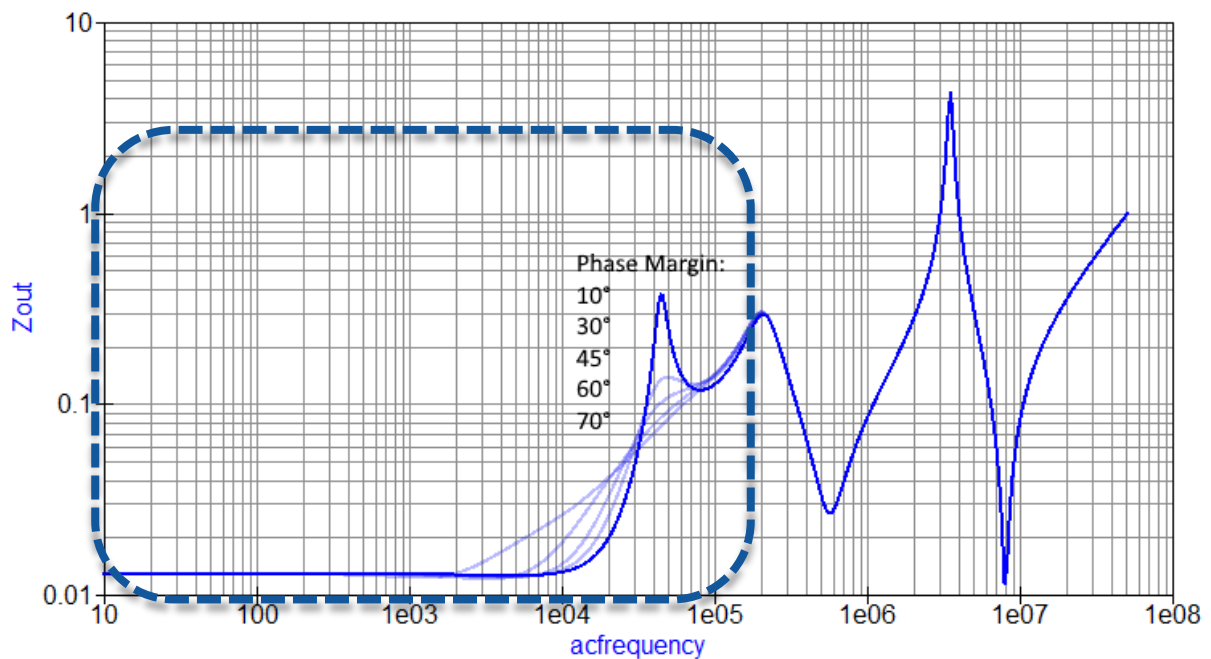


Bode 100 - Application Note

Output Impedance for Stability Analysis



By Florian Hämmerle

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Note: Basic procedures such as setting-up, adjusting and calibrating the Bode 100 are described in the Bode 100 user manual available at:

<https://www.omicron-lab.com/downloads/vector-network-analysis/bode-100/>

Note: All measurements in this application note have been performed using the Bode Analyzer Suite V3.23 Use this version or a newer version to perform the measurements shown in this document. You can download the latest version at

<https://www.omicron-lab.com/downloads/vector-network-analysis/bode-100/>



1 Executive Summary

The output impedance of a linear voltage regulator or switching power supply is an important design parameter that provides information about the control loop stability of the converter as well as information about the decoupling network used to bring the power from the supply to the powered device.

By measuring the output impedance one can estimate the phase margin of the control loop from the resonance peak in the output impedance (Non-Invasive Stability Measurement – NISM). Furthermore, the decoupling network can be analyzed to avoid resonance peaks and provide low impedance over a wide frequency range.

Before starting into the details, I want to express my thanks to Steve Sandler. Steve is the founder of Picotest.com, a guru in the field of power-electronics and a friend. He coined the term “NISM” and did introduce me to the concept already in 2010. I must admit, it took me some time to understand the idea behind NISM. With this document written roughly 10 years after his first explanation, I hope to speed up the learning curve for you as a reader.



Steve Sandler

2 Output Impedance of a Regulated Voltage Source

This section recaps the principal idea of output resistance and output impedance and how it correlates to the control loop of a voltage regulator or switching power supply.

2.1 Unregulated Voltage Source

In theory, a perfect voltage source has zero inner resistance or output resistance R_{out} . This means that the output voltage V_{out} does not depend on the load current I_{out} which is drawn from the voltage source. In every real-life implementation, a voltage source has some non-zero output resistance that will cause the output voltage to drop when the output current rises. Figure 1 shows a DC equivalent circuit model for an ideal (a) and a “real” voltage source (b). The “real” voltage source model uses the non-zero output resistance R_{out} to model the current dependent voltage drop when increasing the load current I_{out} . The output voltage then equals $V_{out} = V_0 - I_{out}R_{out}$.

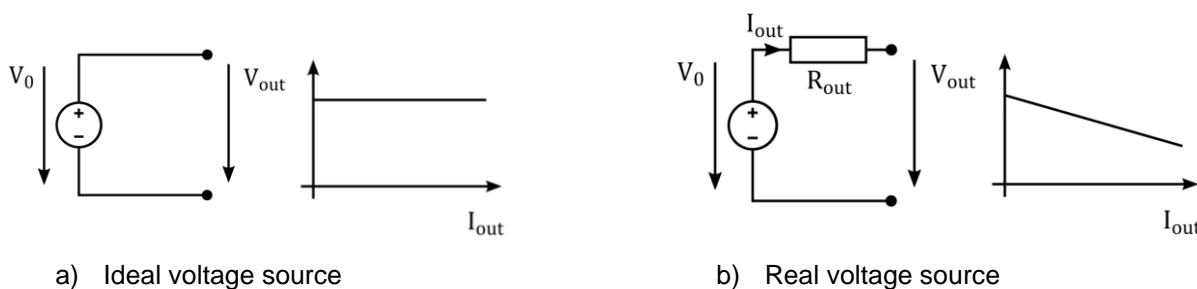


Figure 1: Ideal versus “real” voltage source

The model shown in Figure 1 (b) can describe the voltage drop at DC conditions but it cannot model any dynamic behavior or frequency-dependent behavior. To model frequency-dependent behavior, the output resistance R_{out} can be replaced by a frequency dependent output impedance Z_{out} . In the following, all frequency-dependent parameters will be written as the Laplace transformed term in the s-domain i.e. $Z_{out}(s)$.

2.2 Voltage Feedback Reduces Output Impedance

To compensate for non-ideal behavior such as voltage loss in voltage converting systems, negative feedback is used. A compensator can counteract a voltage loss caused by e.g. a higher load current by changing the duty cycle in a switching converter or by reducing the voltage drop in case of a linear regulator. In both cases, the compensator (or regulator or controller) acts on the power stage to keep the output voltage stable respectively proportional to the reference voltage.

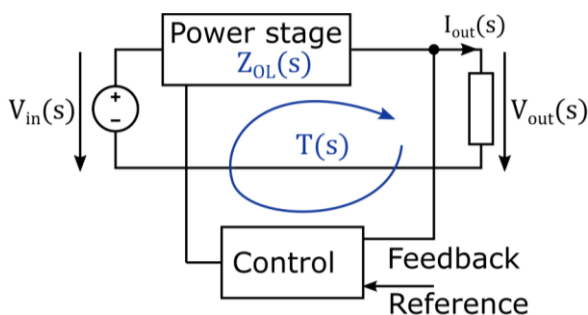


Figure 2: Voltage feedback loop to stabilize the output voltage

Figure 2 shows a feedback system with voltage feedback. The term $T(s)$ is the loop gain of the feedback system (the product of all gains around the loop). Let us call $Z_{OL}(s)$ the open-loop output impedance of the power stage. This means that the power stage is running at a constant operating point meaning the controller signal stays constant (feedback loop not closed). Now, the question arises, how does the output impedance of the system change when we close the loop?

2.3 Output Impedance and Loop Gain

With the open-loop output impedance $Z_{OL}(s)$ and the loop gain $T(s)$, the closed-loop output impedance $Z_{out}(s)$ can be calculated using the following expression (see [1, Ch. 9.2.1]):

$$Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)} \quad (1)$$

From the equation above, the following two cases can easily be analyzed:

- If the loop gain is high ($T(s) \gg 1$), then the closed-loop output impedance $Z_{out}(s)$ will be small respectively much smaller than the open-loop output impedance $Z_{out}(s) \ll Z_{OL}(s)$.
- If the loop gain is low ($T(s) \ll 1$), then the closed loop output impedance $Z_{out}(s)$ equals the open-loop output impedance $Z_{out}(s) = Z_{OL}(s)$ meaning that the feedback or the controller does not affect the output impedance anymore.

From this, we can conclude that high loop gain is required to achieve a low output impedance and that the control loop affects the output impedance below the crossover frequency f_c . Above the crossover frequency where $|T(s)| < 1$ the feedback has little impact on the closed-loop output impedance. In a real-life circuit, the maximum achievable Gain is always limited. Furthermore, the bandwidth of amplifiers is limited. Therefore, the following conclusions can be drawn:

- The loop-gain at DC is not infinite. Therefore, the output resistance R_{out} respectively the low-frequency output impedance Z_{out} is never zero.
- The control loop is not infinitely fast but crosses the 0-dB axis at f_c . Above f_c the feedback has nearly no influence on the output impedance.

2.4 Small-Signal Model of a Voltage-Mode Buck

The relation between $T(s)$ and $Z_{out}(s)$ can be illustrated using a simple simulation example. The following simulation uses the linearized small-signal model of a Buck converter with voltage mode control (Type III compensator). Figure 3 shows the small signal model (closed loop) implemented in Qucs¹. For the open-loop simulation the duty-cycle-ripple was set to zero. The output impedance is measured by applying a 1 A sinusoidal current at the output and measuring the resulting voltage ripple.

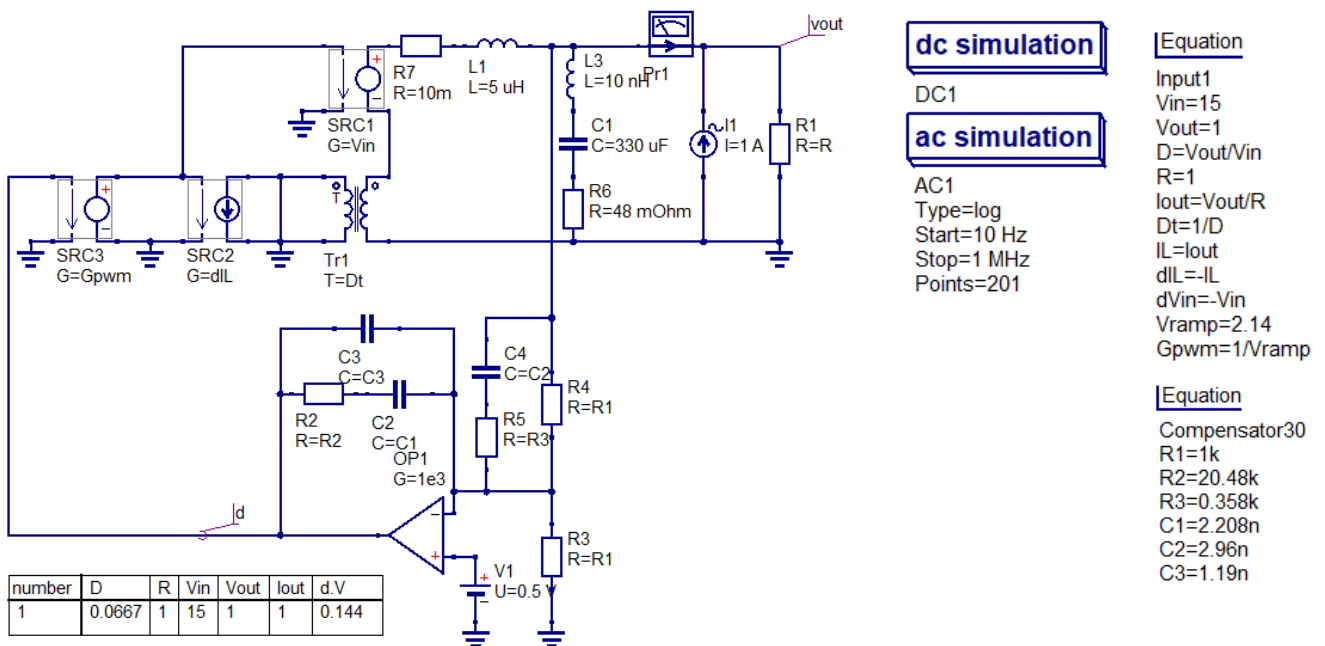


Figure 3: Small-Signal dynamic model of a buck converter

With the shown compensator values (Compensator30), the loop crossover frequency results in $f_c \approx 40 \text{ kHz}$ with a phase margin of $\varphi_m \approx 30^\circ$. The maximum gain of the error amplifier was set to 70 dB.

¹ QUCS stands for Quite Universal Circuit Simulator. Qucs is open source.

The loop gain plot is shown in Figure 4 on the following page. It shows the DC or low-frequency gain of 70 dB and the falling gain over frequency as well as the crossover frequency f_c . Note that this does not show a good compensator design but is for illustration purpose only. The slope at crossover is too high, resulting in a poor phase margin of only 30°.

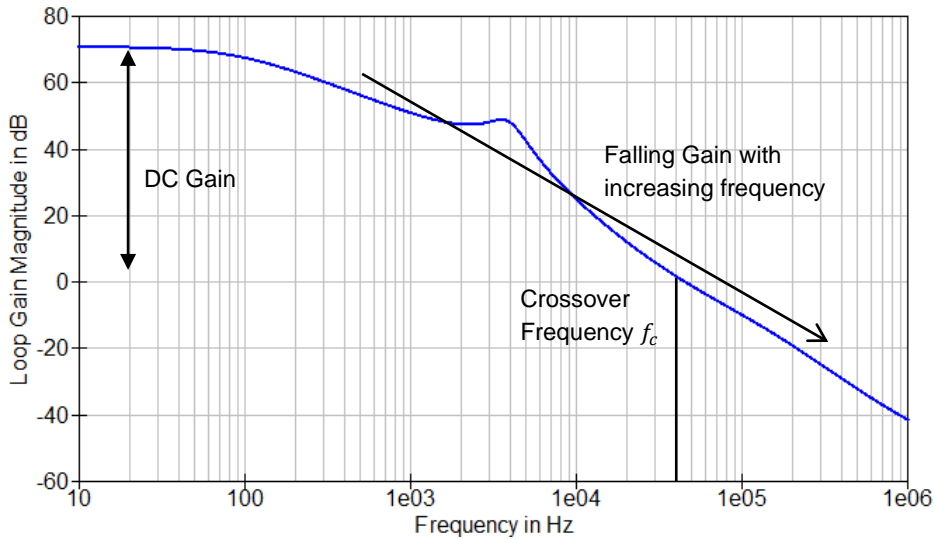


Figure 4: Loop-gain of the buck-converter simulation example

Figure 5 below shows the calculated output impedance in the closed-loop case (blue) and open-loop case (red). When comparing it to Figure 4, one can clearly see that high loop-gain reduces the closed-loop output impedance. As the loop-gain reduces, the difference between the open-loop output impedance (red) and the closed-loop output impedance (blue) gets less and above crossover frequency, the curves overlap since the effect of the feedback becomes negligible.

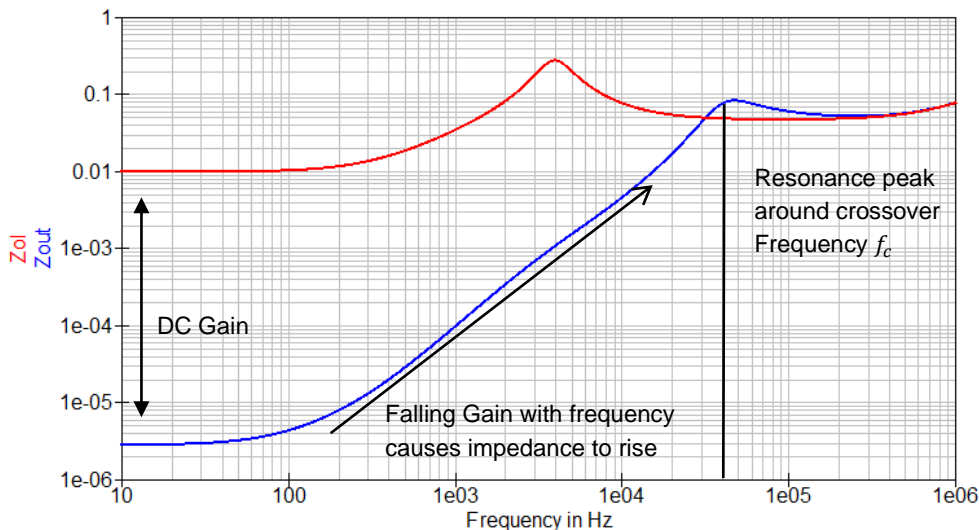


Figure 5: Open-loop and Closed-loop output impedance

Around the loop crossover frequency, the closed-loop output impedance (blue curve in Figure 5) becomes higher than the open-loop output impedance (red curve) showing a peaking at the crossover frequency. This “resonance peak” is caused by the oscillatory behavior of the

closed loop system caused by the low phase margin of the control loop. Lowering the phase margin will cause a higher resonance peak in the closed-loop output impedance whereas a high phase margin causes high damping which will reduce the peaking at resonance.

2.5 The Peak in Output Impedance coheres with Phase Margin

In this section, we will look at the influence of the phase margin on the closed-loop output impedance $Z_{out}(s)$. Figure 6 shows five different compensators that have the same crossover frequency of ≈ 40 kHz, but different phase margin values of 10° , 30° , 45° , 60° and 70° .

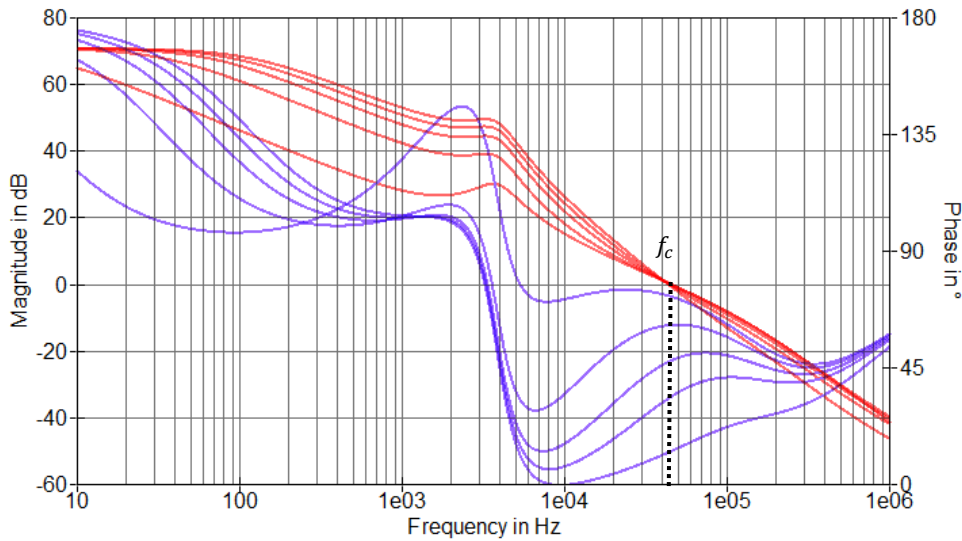


Figure 6: Loop-Gain with different phase margin values

The corresponding output impedance curves are shown in Figure 7 below. The peaking in the output impedance appears at crossover frequency and correlates with the phase margin of the loop. The highest peak appears in the case of 10° phase margin whereas the peaking disappears for phase margin values above 60° .

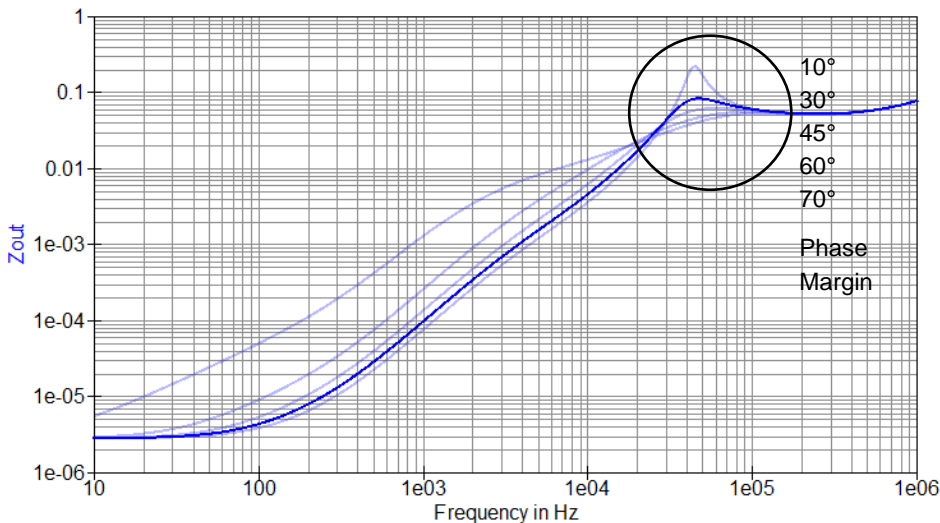


Figure 7: Output impedance Z_{out} for different phase-margin values

3 Non-Invasive Stability Measurement (NISM)

The correlation between phase margin and the impedance-peaking in the closed-loop output impedance can be used to derive the phase margin of the control loop from one closed-loop output impedance measurement (see also [2]).

For a “simple” loop gain curve that crosses the 0 dB axis with a slope of approximately -20 dB per decade and does not have poles and zeros close to the crossover frequency, the following relation between the closed-loop quality factor Q and the phase margin φ_m holds (see [1, Sec. 9.4.2]):

$$Q = \frac{\sqrt{\cos(\varphi_m)}}{\sin(\varphi_m)} \quad (2)$$

This means that by measuring the Q of the closed-loop system one can estimate the phase margin of the control loop. Measuring the Q of the closed-loop system can be done by measuring the Q of the peaking in the output impedance that appears at f_c when the system is insufficiently damped.

3.1 Measuring Closed-Loop Q

A very sensitive way to measure the quality factor Q is measuring it via the phase slope at resonance. The higher the Q , the sharper the phase-turn, respectively the higher the slope of phase at resonance as shown in Figure 8 below.

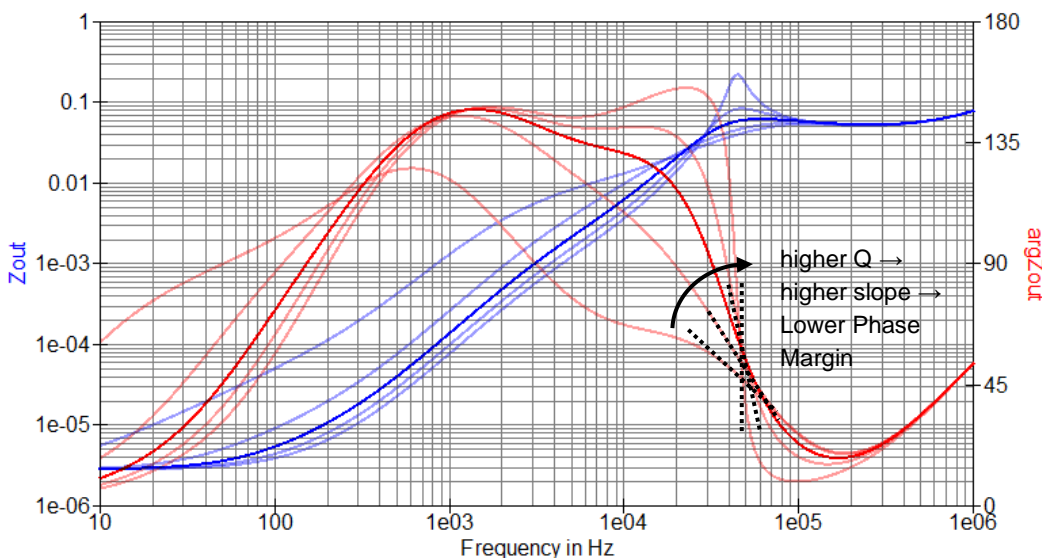


Figure 8: Output impedance with phase for different phase-margin values

The Bode Analyzer Suite uses the group delay $T_g = -\frac{d\varphi}{d\omega}$ for the calculation of Q . The used equation is shown below and can be found in RF literature such as [3, p. 60] or [4, p. 235]:

$$Q(T_g) = |\pi \cdot f \cdot T_g| \quad (3)$$

3.2 Deriving φ_m from Q

The closed-loop Q is used to derive the phase margin by reading the maximum value of the measured $Q(T_g)$ curve around the loop-crossover frequency respectively close to the peak in output impedance. The following Figure 9 shows the $Q(T_g)$ curves (red) for the different phase margin values of the small-signal Buck-simulation:

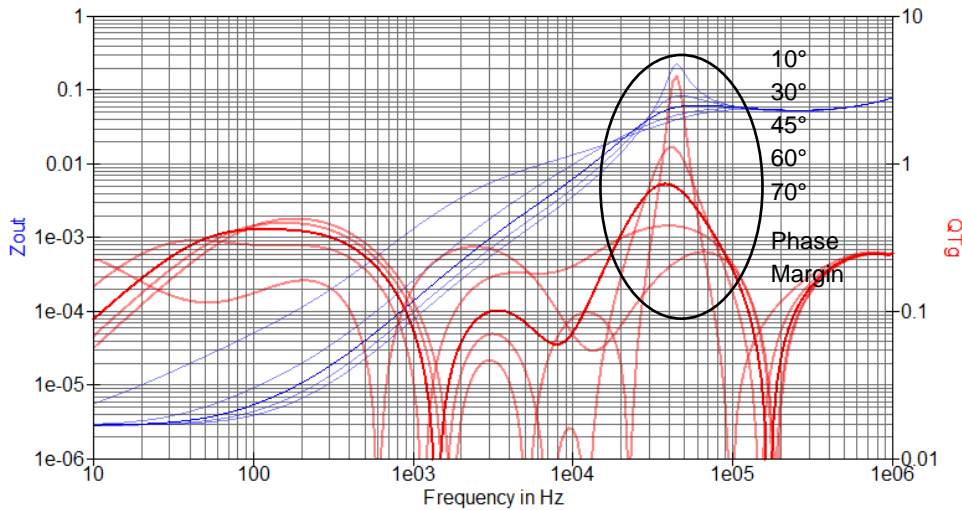


Figure 9: Output impedance with $Q(T_g)$ in low-phase margin cases

The results from the NISM calculation are listed in the table below. The measured phase margin is the reading from the bode-plot of the simulated loop-gain. The closed-loop quality factor is taken from the maximum of the $Q(T_g)$ curve from Figure 9. The phase margin was calculated from the Q using NISM.

Measured φ_m Via Loop Gain	Closed-loop Q maximum value of $Q(T_g)$	Calculated φ_m using NISM
12.4°	4.32	12.9°
33.4°	1.31	37.4°

The two measurements show that NISM provides accurate results for low phase-margin values (12.9° instead of 12.4°) but starts to be less accurate when the phase margin gets higher. Above 30° phase margin, the result will deviate from the loop-gain measurement (e.g. 37.4° instead of 33.4°). For higher phase margin values, the deviation will be higher.

In this case, the algorithm implemented in the Bode Analyzer Suite (Basic Phase Margin Calculation) was used. The Bode Analyzer Suite does also offer an improved algorithm (see [2], [5], [6]) that uses two cursors and provides more accurate results also for higher phase margin values up to around 60°.

Note: The Bode Analyzer Suite implements an improved and proprietary NISM calculation algorithm from Steve Sandler (see [2], [5], [6]) that is not identical to equation (2).

3.3 Conclusion

The NISM method provides a very simple and fast assessment method to identify control-loop stability issues without measuring the loop itself. The lower the phase margin of a voltage regulator, the higher the peaking in the output impedance and the more accurate the results provided by this method.

If no clear peaking appears in an output impedance measurement in a frequency range where the control-loop bandwidth is expected, the phase margin will be approximately 45° or higher and therefore the system is not subject to excessive overshoot and ringing from low phase margin.

In the next section, we will have a look at a real-life output impedance measurement example demonstrated on a SEPIC converter.

4 Experimental Verification of NISM

To demonstrate that NISM does not only work in simulation or for linear regulators, the following measurements were made on a SEPIC converter. This SEPIC provides a wide input range which makes it simple to measure high-phase margin operating points as well as low-phase margin conditions on the same device under test.

4.1 DC/DC Converter Under Test

The measurements outlined in this section were performed on the Analog (Linear) demo circuit 1342B, a SEPIC converter with 18 V to 72 V input voltage and a fixed 24 V output voltage with a maximum load current of 1 A and a switching frequency of 300 kHz.

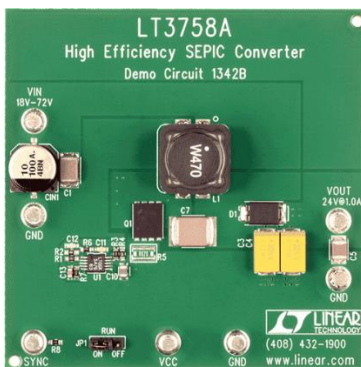


Figure 10: Converter Under Test

The following figure shows the circuit diagram or schematic of the converter including the component values and the compensation network consisting of C12, R6 and C11.

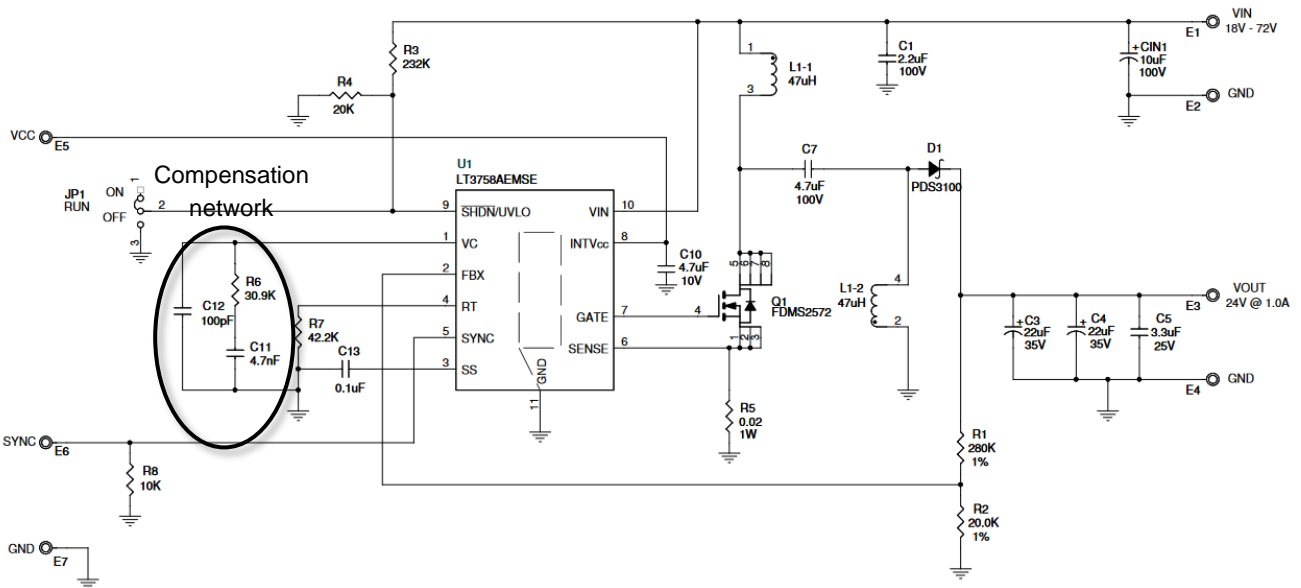


Figure 11: Converter schematics from the manufacturer’s demo-manual

4.2 Reducing Control-Loop Stability

The demo circuit provides a very high phase margin over all operating conditions. This means that no peak in the output impedance will appear and no phase margin values can be derived using NISM.

For demonstration purpose, the compensator network was changed to have less phase margin. This will end up in a peak in the output impedance that allows applying NISM. To quickly change the compensation network, the circuit was simulated using the power supply design software WDS from Biricha. For more details on WDS, please check out www.biricha.com.

The following table lists the original and the modified type-II transconductance compensator as it was used for the measurements shown in this document:

Parameter	Original high phase margin	Modified lower phase margin
C12	100 pF	100 pF
R6	30.9 kΩ	100 kΩ
C11	4.7 nF	1 nF
Pole at origin	≈ 500 Hz	≈ 2 kHz
Pole	≈ 52.6 kHz	≈ 17.5 kHz
Zero	≈ 1.1 kHz	≈ 1.6 kHz

Increasing the pole at origin increases the loop crossover frequency. At the same time the pole was lowered to reduce the phase margin even further. This leads to a faster but less stable system in

some operating points. To check how the loop performs in detail, a loop-gain measurement was performed using the voltage-injection method.

4.3 Loop Gain Measurement

Figure 12 below shows the measurement setup including the 10 Ω injection resistor placed above the feedback divider. The B-WIT 100 is used to inject the disturbance signal (isolate the Bode 100 output source) whereas the input channels measure the loop-gain. For more information on the loop-gain measurement method, please refer to our webinar recordings or application notes on www.omicron-lab.com.

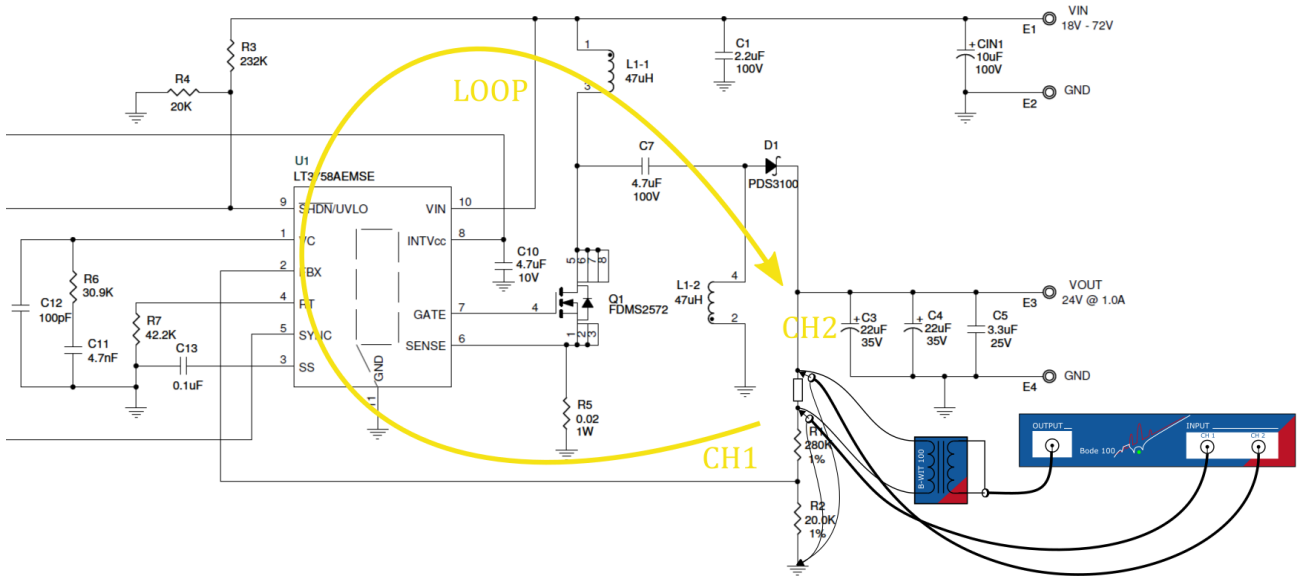


Figure 12: Loop-Gain measurement setup with 10Ω injection resistor in the feedback path

The following table lists the measured phase margin and crossover frequency derived from the measurement results shown in Figure 12 on the next page:

Operating Point V_{in}, I_{out}		Crossover Frequency f_c	Phase Margin φ_m
50 V	0.3 A	17.29 kHz	44.2°
50 V	1 A	22.93 kHz	26.7°
30 V	1 A	20.6 kHz	18.3°
18 V	0.6 A	17.3 kHz	12.3°
18 V	1 A	17.75 kHz	3.5°

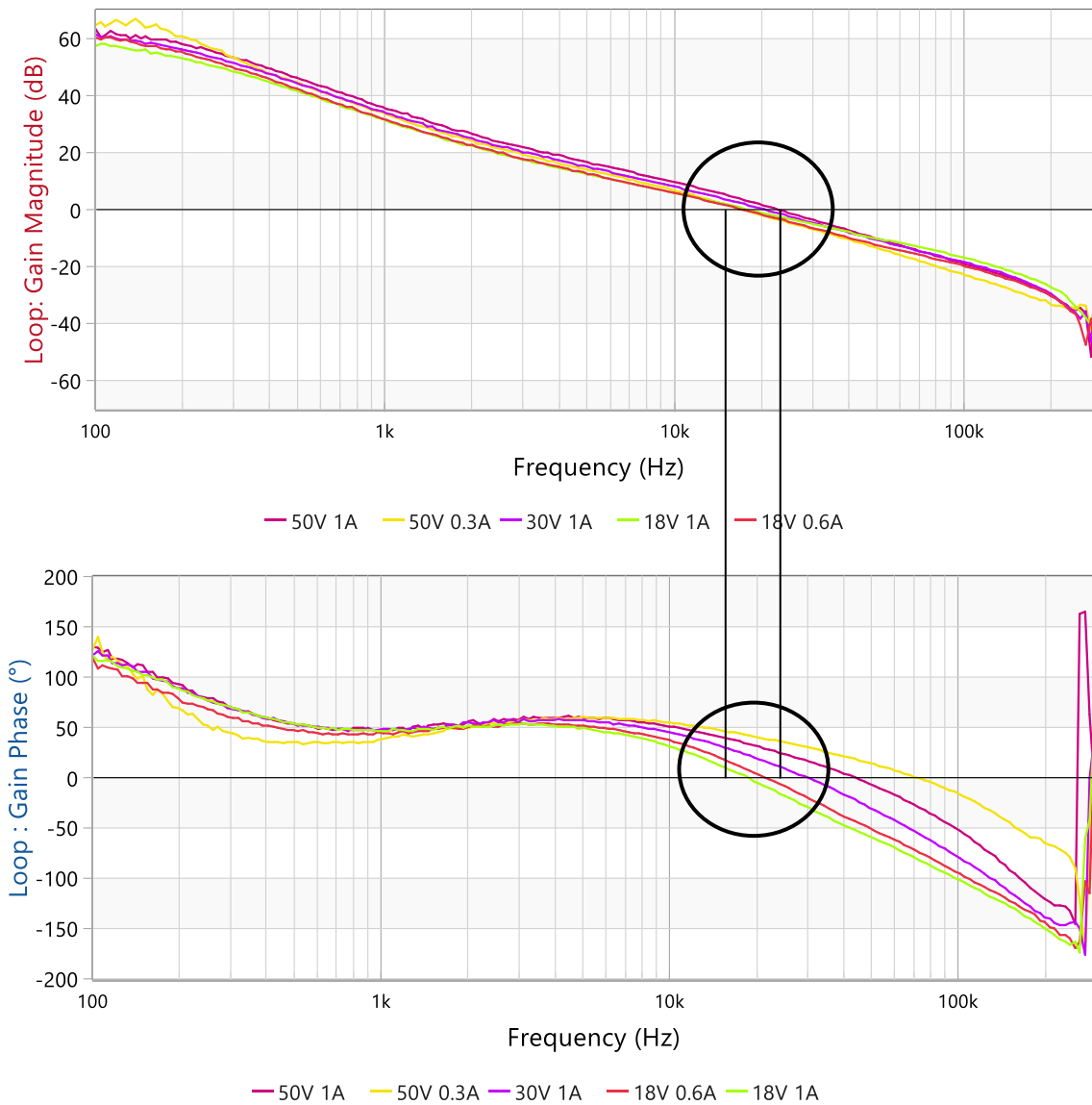


Figure 13: Measured loop-gain curves at different operating points

The measurement shows that the crossover frequency is between 17.2 kHz and 22.9 kHz with phase margin values between 3.5° and 45°. In some operating points the system will work “fine” when having a phase margin of 45° but as soon as the phase margin is coming close to 20° and even lower, the overshoot and ringing will be clearly visible. As a next step, the output impedance is measured and NISM is used to derive the phase margin from the output impedance measurement alone.

4.4 Output Impedance Measurement

There are several possibilities to measure the output impedance of a converter or voltage regulator. Please refer to the OMICRON Lab webinars or application notes on how to select the most suitable method for your application. In this case, the J2111A from Picotest was used to perform an output impedance measurement.

4.4.1 Measurement Setup

The J2111A is connected to the output of the SEPIC converter as shown in Figure 14. The Bode 100 output drives the current modulation input of the J2111A and CH1 measures the output current whilst CH2 measures the output voltage. Since only the AC portion of the signals are measured, this results in the output impedance when using the Voltage/Current method from the Bode Analyzer Suite.

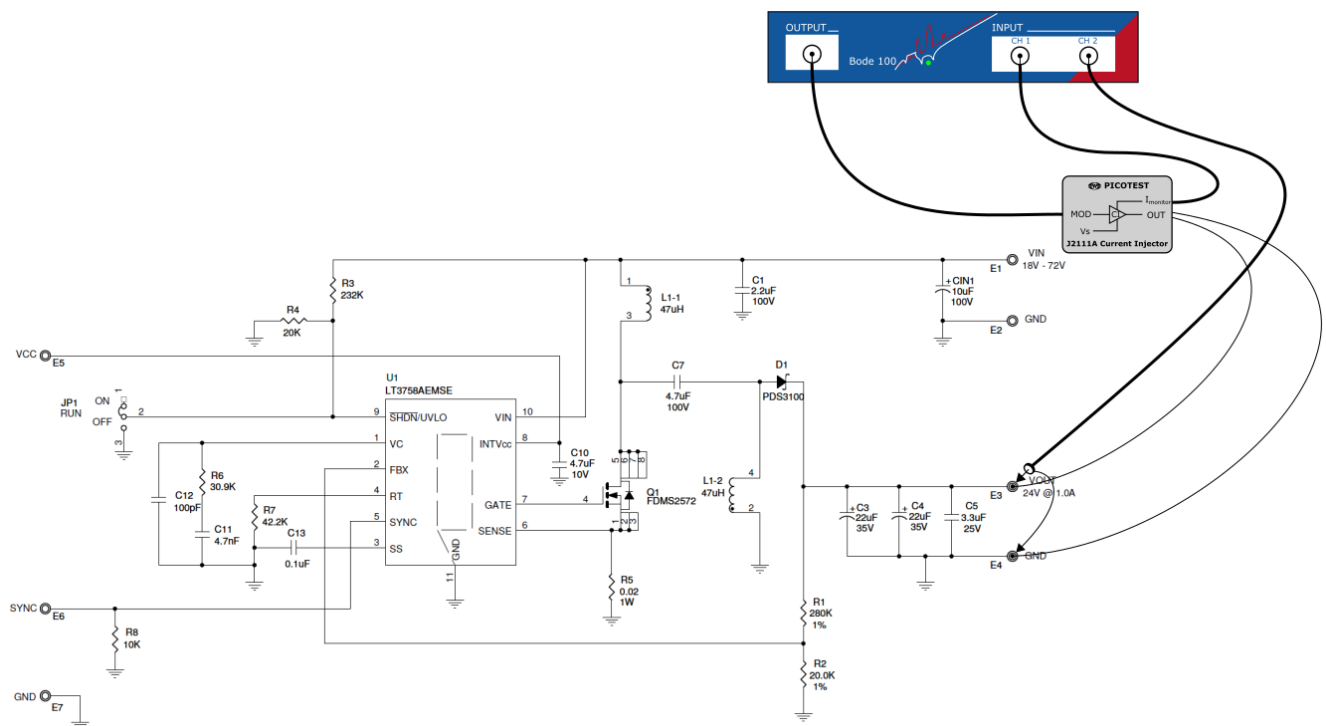


Figure 14: Output impedance measurement setup

More details on the measurement method can be found in [7] or in OMICRON Lab webinars.

Note that this method applies a 25 mA DC load to the output. This could be critical in case of low-power applications or voltage references. On top of this 25 mA DC, a small AC current signal is drawn from the DUT.

4.5 Measurement Results

Figure 15 below shows the output impedance of the SEPIC converter at different input voltages and load-currents. In the frequency range from 10 kHz to 30 kHz, the output impedance peaks depending on the phase margin of the control loop.

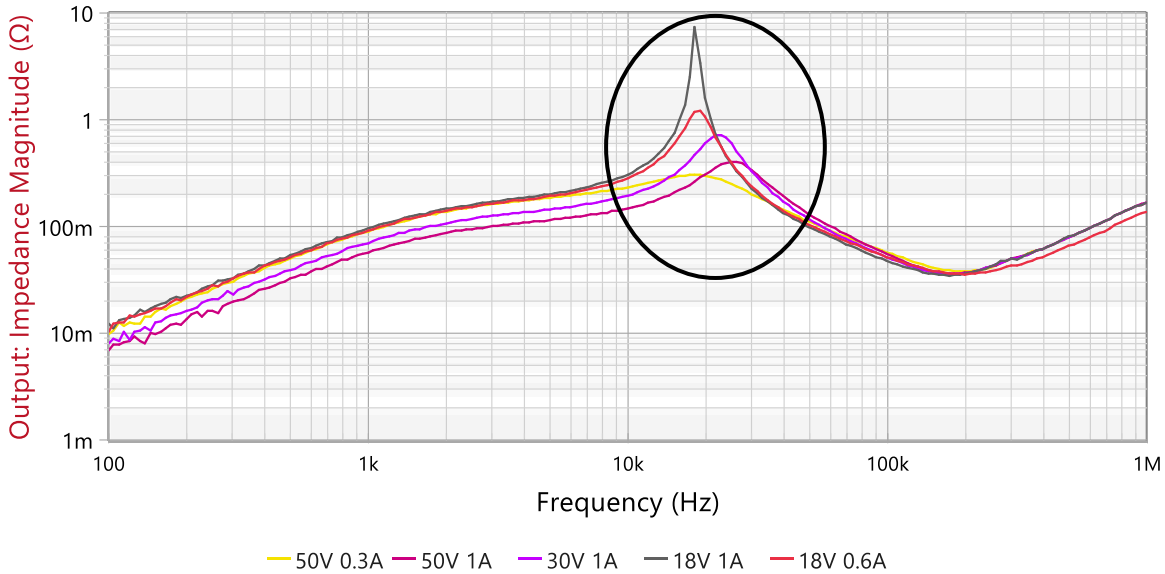


Figure 15: Output impedance curves of the SEPIC

Note that the peaking in impedance can be quite significant. The maximum output impedance rises from roughly 300 mΩ in the well-damped case to 7 Ω at resonance in the undamped case. This could even cause an issue with the input impedance of a following converter if its input impedance is not significantly higher than 7 Ω.

The peaks in the output impedance appear at the same frequency as the $Q(T_g)$ peaks as shown in Figure 16 below. From the height of the peak in $Q(T_g)$ the phase margin is calculated.

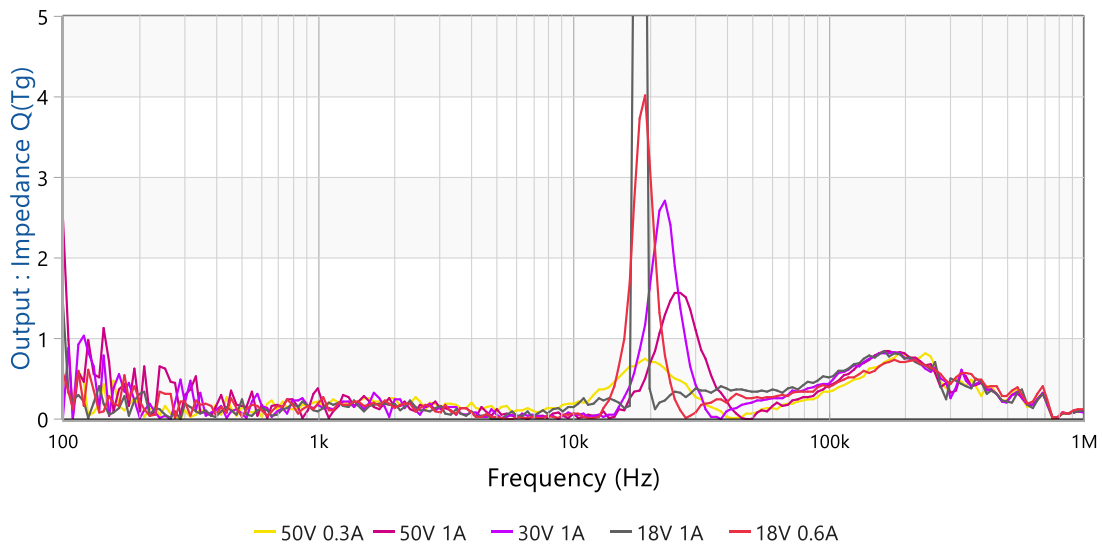


Figure 16: $Q(T_g)$ peaks correspond to impedance peaks

The following table lists the measured resonance frequency of the peak in impedance as well as the height of the $Q(T_g)$ -peak and the calculated phase-margin result from the Bode Analyzer Suite.

Operating Point V_{in}, I_{out}		Resonance Frequency f_r	Maximum peak of $Q(T_g)$	NISM Phase Margin φ_m
50 V	0.3 A	20.1 kHz	0.74	57.8°
50 V	1 A	25.8 kHz	1.57	32.3°
30 V	1 A	22.9 kHz	2.72	20°
18 V	0.6 A	18.9 kHz	3.96	14.1°
18 V	1 A	18.2 kHz	15	3.8°

Let's now compare the results from NISM with the results from the loop-gain measurement.

4.6 Comparing Loop Gain & NISM Results

Phase margin results of the loop-gain measurement are compared to the result of the NISM calculation in the table below. It can be clearly seen that for low phase margin values, the loop-gain results and the NISM results do match well. The higher the phase margin, the better the damping of the closed-loop system, the less clearly a resonance can be identified and the lower the agreement between the two methods.

However, critical low-phase-margin cases can be identified easily and can be qualified accurately.

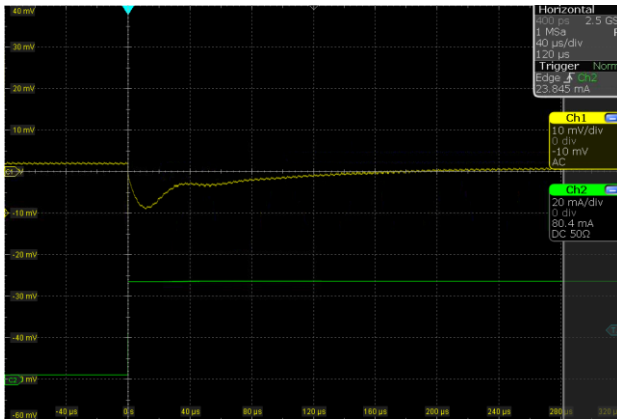
Operating Point V_{in}, I_{out}		Loop Gain Phase Margin	NISM Phase Margin
18V	1 A	3.5°	3.8°
18 V	0.6 A	12.2°	14°
30 V	1 A	18°	20°
50 V	1 A	27°	32°
50 V	0.3 A	44°	58°

But why is a high phase margin important? In the next section, the transient response of the converter is analyzed for the different phase-margin cases.

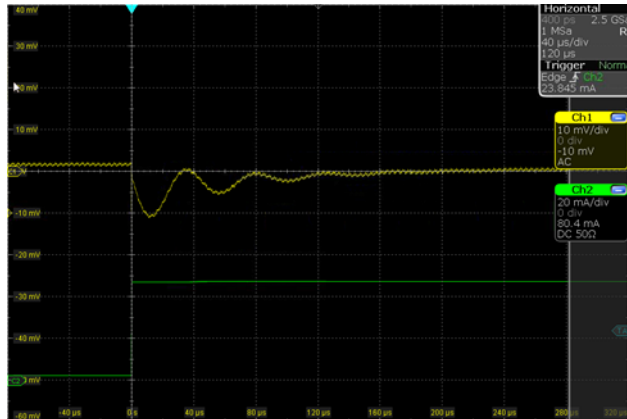
4.7 Transient Response

The following figures show the transient response of the system for different operating points. The transient response was captured using repetitive 25 mA load steps generated by the J2111A and an AWG. Averaging was used to remove the switching ripple / noise.

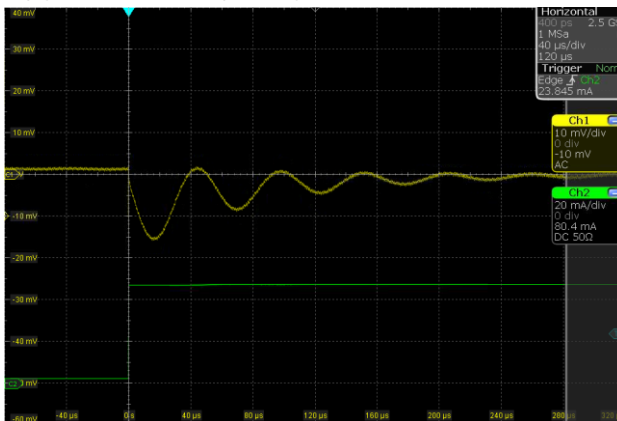
(a) 50 V, 0.3 A ($\approx 45^\circ$)



(b) 30 V, 1 A ($\approx 20^\circ$)



(c) 18 V, 0.6 A ($\approx 13^\circ$)



(d) 18 V, 1 A ($\approx 4^\circ$)

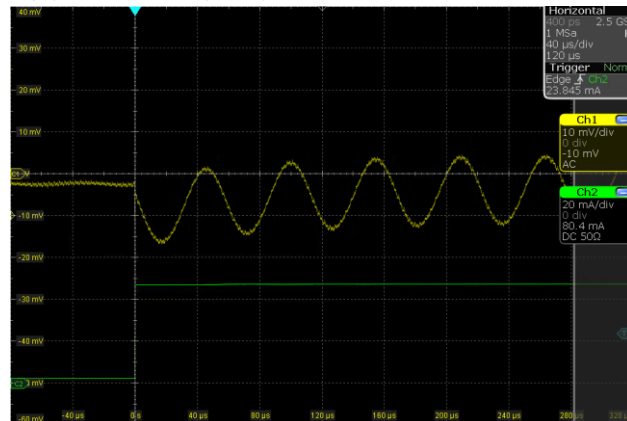


Figure 17: Transient response for different phase margin values

The transient response in Figure 17 clearly shows the difference between the different operating points. Figure 17 (a) shows a well-damped case with 45° of phase margin. Only slight ringing is visible. In Figure 17 (b) the ringing starts to be clearly visible. Due to the low phase margin of 20° , the system is not sufficiently damped, and it takes roughly $200 \mu\text{s}$ until the ringing disappears. In the last picture (d) there is practically no damping and the ringing goes on for a long time. This will certainly cause a clear disturbance signal at the crossover frequency of 18 kHz, which can couple into other circuits and will certainly degrade system performance.

5 Summary

Performing an output impedance measurement over frequency provides an insight into the control-loop stability of a power converter or voltage regulator. The great advantage of this method is that the loop must not be opened, and no signal must be injected into the feedback loop. The output ports or output capacitors of a converter or regulator are always accessible, which means that an output impedance measurement is practically always possible.

Besides information about the control loop, the output impedance measurement can also reveal improperly damped decoupling or output filtering.

The measurement setup of course depends on the voltage level and power level.

Please refer to our Output Impedance [webinar](#) for more details on how to choose the right measurement method and how to reveal issues in the decoupling network.

6 References

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