FH Vorarlberg
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Dc Biased Equivalent Series Resistance Measurement and Loss Estimation in Ferroelectric Ceramic Capacitors

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Kurzreferat

Messung des äquivalenten Serienwiderstandes und Verlustbestimmung von ferroelektrischen Keramikkondensatoren unter anliegender Gleichspannung

In dieser Arbeit wird der Effekt von Gleichspannung auf den äquivalenten Serienwiderstand (ESR) von Kondensatoren und im speziellen von ferroelektrischen Keramikkondensatoren (FDCC) untersucht. Weiters wird der Einfluss des ESR unter Gleichspannung auf die Verluste in den Kondensatoren untersucht. Piezoelektrische Resonanzen (PR) welche in FDCCs mit anliegender Gleichspannung auftreten werden analysiert und deren Einfluss auf die Verluste inspiziert.

Für diese Untersuchungen wird eine Messschaltung entwickelt um die Impedanz bwz. den ESR von Kondensatoren in Kombination mit einem vektoriellen Netzwerkanalysator mit anliegender Gleichspannung zu messen. Die Schaltung wird verwendet um den ESR von Kondensatoren unterschiedlicher Technologie zu messen und deren Verhalten in Bezug auf Gleichspannung zu evaluieren. Die Verluste eines FDCCs werden in einer leistungselektronischen Schaltung mit einem kalorimetrischen Messsystem gemessen. Der Einfluss der PR auf die Verluste wird gemessen indem die Schaltfrequenz der leistungselektronischen Schaltung genau der PR Frequenz entsprechend eingestellt wird. Somit entspricht auch die Frequenz des Kondensatorstromes der Frequenz der PR. Die gemessenen Verluste werden mit einer Berechnung verglichen, die die Fourier Koeffizienten des Stromes, sowie den entsprechenden ESR verwendet.

The Messungen zeigen einen zunehmenden ESR mit Gleichspannung für die gemessenen FDCCs. Die Verlustmessungen zeigen eine signifikante Zunahme der Verluste in einem FDCC wenn der Strom genau einer PR entspricht. Folglich ist auch eine Abnahme des Gesamtwirkungsgrades der Schaltung an diesem Punkt zu beobachten. Die Verlustberechnungen stimmen nicht exakt mit den Messungen überein, aber die Abweichungen liegen für alle Messungen in der gleichen Größenordung und Richtung.

Abstract

Dc Biased Equivalent Series Resistance Measurement and Loss Estimation in Ferroelectric Ceramic Capacitors

In this thesis the effect of dc voltage bias on the equivalent series resistance (ESR) of capacitors and especially ferroelectric dielectric ceramic capacitors (FDCC) is analysed. Further the influence of the dc biased ESR on the losses of capacitors is investigated. Also piezoelectric resonances (PR) occurring in FDCCs with applied dc bias and their influence on the losses are analysed.

Therefore a measurement circuit to measure the impedance and thus the ESR of capacitors in combination with a vector network analyser (VNA) is developed. Using the developed circuit the ESR of capacitors of different technologies is measured and their behaviour with dc bias is evaluated. The losses of an FDCC are measured in a power electronic (PE) circuit with a developed calorimetric measurement system (CMS). The influence of the PR is investigated by tuning the switching frequency of the PE system and thus the frequency of the capacitor current exactly into the PR. The measured losses are then compared to a calculation based on the capacitor current harmonics and the respective ESR.

The measurements show an increase of the ESR with dc bias for all measured FDCCs. The loss measurements show a significant increase of the losses in an FDCC if the current frequency matches the PR frequency. Consequently a decrease of the PE system's efficiency is measured. The loss calculations do not exactly match the measurements but there is a systematic deviation of the same order for all measurements.

Acknowledgement

I want to thank these people who were actively or passively involved in the realisation of this thesis.

- My supervisor André Mitterbacher
- My mother, my brothers and my friends
- The Omicron Lab Team

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List of Abbreviations and Symbols

dc Direct Current

ac Alternating Current

ESR Equivalent Series Resistance

FDCC Ferroelectric Dielectric Ceramic Capacitor

PR Piezoelectric Resonances

VNA Vector Network Analyzer

PE Power Electronics

CMS Calorimetric Measurement System

ESL Equivalent Series Inductance

CC Ceramic Capacitor

RMS Root Mean Square

OSL Open-Short-Load

DUT Device Under Test

ABB Auto-Balancing Bridge

OA Operational Amplifier

LISN Line Impedance Stabilisation Network

TCM Two Capacitor Measurement

E-cap Electrolytic Capacitor

Mosfet Metal Oxide Semiconductor Field Effect Transistor

FFT Fast Fourier Transform

1 Introduction

FDCCs are widely used in PE today. FDCCs can exhibit several advantages like high capacity density, low ESR and especially compared to electrolytic capacitors an increased lifetime. Negative attributes of FDCCs are temperature and voltage dependence of the capacitance, dielectric losses and sound emissions due to the inverse piezoelectric effect, among others. Current investigations show also peaks in the ESR, in component specific frequencies when dc bias[1] is applied. Their cause is not fully determined, but assumed to be resonances due to mechanical oscillations caused by the inverse piezoelectric effect [TB16] [Nov+11]. The decrease of capacitance with dc bias is generally known and has been focus in many investigations in the past[2] [Nov+11] [BLD00]. However the behaviour of the ESR with dc bias is not fully analysed and a general trend is to the knowledge of the author not documented yet.

The losses in capacitors are related to the ESR and the current through the capacitor, as e.g. shown in [TB16] and [Has+16]. This leads to the question how the losses in capacitors are influenced by the dc bias and how the losses can be predicted knowing the ESR at the respective dc voltage level and frequency.

1.1 Focus of this Thesis

In this thesis the research question is discussed how the ESR of FDCCs can be measured with dc bias and how the dc bias influences the losses of FDCCs in PE applications.

First a suitable measurement circuit is developed to measure the ESR over frequency with applied dc bias. With this circuit the effect of dc bias on the ESR and further on the losses is investigated. A determined FDCC is then embedded into a typical PE application and analysed for the losses. The losses are measured in a specific frequency, where the FDCC is tuned into an ESR peak, which is assumed to be a mechanical resonance caused by the inverse piezoelectric effect. This peaks are further referred as PR. The loss measurement is done using a self-developed CMS. The measured losses are then compared to loss calculations using the ESR at the specific frequency and dc bias. Further loss calculations are performed using the Fourier coefficients of the current with the respective ESR values, because the current in the PE system is not sinusoidal. The losses are then set in relation to the overall losses of the PE system to obtain the change in the system's efficiency.

[1] In this work dc bias always refers to dc voltage bias

[2] The capacitance can in some cases also increase with dc bias, like e.g. in TDK's cera-link capacitors[TDK19]

1.2 Capacitor Equivalent Circuit and ESR

The real capacitor as component is usually modelled with three ideal components: an ideal capacitance, an ESR and an equivalent series inductance (ESL). The ESR is frequency dependent, especially in FDCCs. It models the influences of the ohmic connection resistances and also the dielectric losses. In the equivalent circuit shown in figure 1.1 also a resistor R_p is included in parallel to the capacitance C. This resistor models the finite insulation resistance of the capacitor's dielectric. The R_p is often neglected, or calculated into the ESR. This is also the case in this thesis.

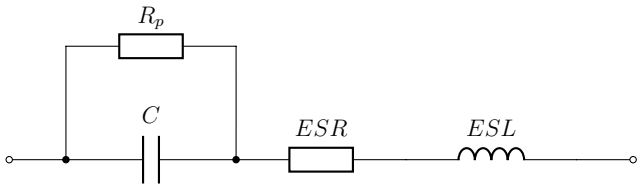

Figure 1.1: Equivalent circuit of a real capacitor

Figure 1.2 shows the impedance Z of a capacitor in the complex plane. In resonance the reactances of the capacitor and the ESL have the same length and cancel out due to the opposite direction of the vectors.

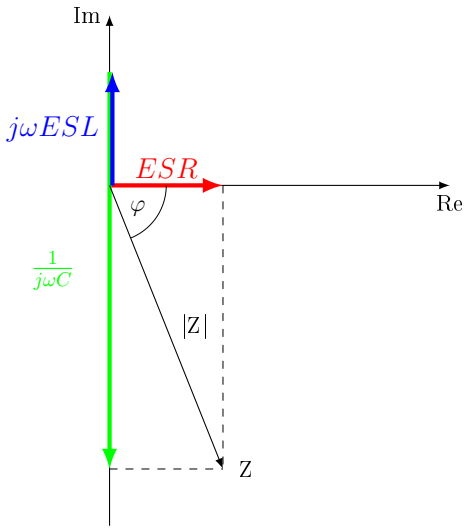

Figure 1.2: Impedance of a real capacitor in the complex plane

Figure 1.3 shows the magnitude and the phase of a capacitor over a specific frequency range. Below circa 1 MHz in this example the magnitude is monotonically decreasing and the phase is close to $-90\,°$, the capacitive part is dominant. Above 1 MHz the magnitude is monotonically increasing and the phase is close to $+90\,°$, the inductive part is dominant. In the transition from capacitive to inductive the imaginary parts cancel out and only the real part, the ESR, is remaining. At the resonance point the

phase equals 0 °. The plot shown in the figure is called Bode plot. A Bode plot contains usually a plot of the magnitude versus frequency and one of the phase versus frequency. A Bode plot can be measured using a VNA, or a frequency response analyzer. The plot in figure 1.3 is measured with the Bode 100 VNA from Omicron Lab.

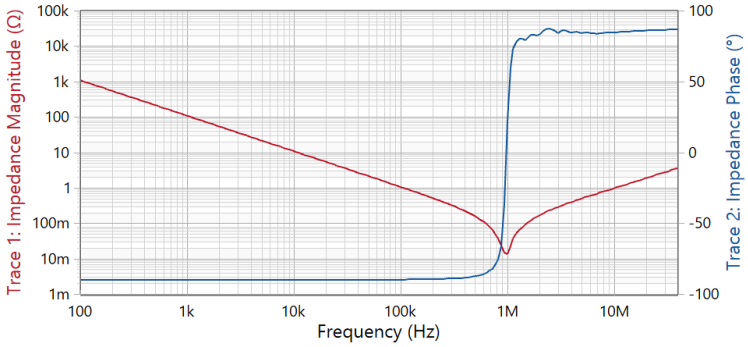

Figure 1.3: Bode plot of a capacitor. Red: magnitude; blue: phase

1.3 Small Signal and Large Signal Capacitance

The general relationship between charge and voltage

$$Q = CV \tag{1.1}$$

and

$$C = \frac{Q}{V} \tag{1.2}$$

respectively, does not apply if the capacitance is non-linear as it is the case in FDCCs. Here it has to be differentiated between the small signal capacitance and the large signal capacitance. In figure 1.4 the difference between these two capacitances is illustrated. The slope of the curve is proportional to the capacitance. The difference between the two capacitances is clearly visible. The small signal capacitance is calculated with

$$C_{ss} = \frac{dQ}{dV} \tag{1.3}$$

while the large signal capacitance is calculated with

$$C_{ls} = \frac{\Delta Q}{\Delta V} \tag{1.4}$$

The small signal capacitance can be obtained practically by decreasing the amplitude of the applied ac voltage until the approximated value fits sufficiently.

In this thesis capacitance always means small signal capacitance. Furthermore it is assumed that the measurement signal is always sufficiently small to get the small signal capacitance. Otherwise it is distinguished.

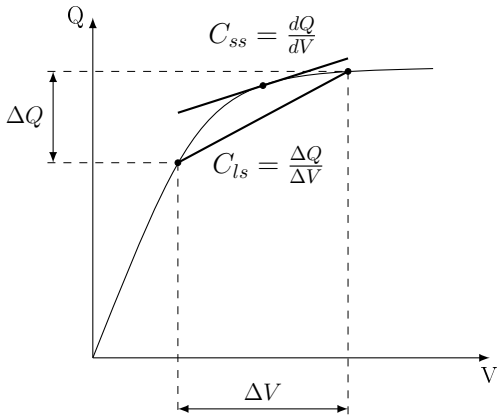

Figure 1.4: Difference between small signal and large signal capacitance

1.4 Ferroelectric Ceramic Capacitors

FDCCs are ceramic capacitors (CC) with a high dielectric constant compared to non-ferroelectric CCs. CCs are categorised in two classes, where class 1 are non-ferroelectric CCs and class 2 are FDCCs. FDCCs show temperature and dc and ac voltage dependence, respectively. FDCCs are also piezoelectric thus noise pollution and resonances in mechanical oscillations can occur like described in [TB16]. Commonly used Class 2 CCs are e.g. X7R, X7S, Z5U, etc. and class 1 CC are e.g. C0G (also referred to as NP0). The three character codes describe the temperature behaviour of the respective CCs.

In contrast to the equivalent series circuit described in the previous section 1.2 [Ben18] proposes a parallel circuit for the description of the losses of FDCCs like shown in figure 1.5. This method assumes that the ESR of FDCCs can be approximated with an equation of the form

$$ESR_{FDCC} = \frac{k_s}{f} + ESR_0 \tag{1.5}$$

where k_s is a constant with the unit ΩHz and ESR_0 is the minimal value of the ESR.

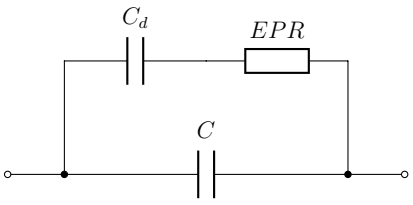

Figure 1.5: Parallel equivalent circuit model of an FDCC

The circuit in figure 1.5 consists of the ideal capacitance C, a frequency dependent parallel resistor EPR and a dc block capacitor C_d which prevents a dc current from flowing through the EPR.

The EPR can be calculated with

$$EPR = \frac{1}{(2\pi fC)^2 \left(\frac{k_s}{f} + ESR_0\right)} \tag{1.6}$$

The associated power loss can further be obtained with an equation similar to the Steinmetz equation, which describes the losses in ferromagnetic materials [Ste92].

$$P_{loss} = k_p f V_C^2 \tag{1.7}$$

where

$$k_p = (2\pi C)^2 k_s \tag{1.8}$$

This analogy is not coincidentally, hence both mechanisms exhibit losses due to hysteresis effects. The amount of hysteresis loss per cycle seems not to change with frequency thus the dielectric losses are stated to be directly proportional to the frequency and the square of the applied voltage according to [Ben18]. Losses in FDCCs are still a topic of research; which effects are contributing to the losses is not fully clarified yet.

1.5 Loss Calculation in Capacitors using ESR

The losses in capacitors are often calculated by the equation

$$P = I^2 \cdot ESR \tag{1.9}$$

like e.g. in [TB16], or [CBP18]. I is the root mean square (RMS) current.

Some sources use the Fourier transform to get a better suited approximation for the losses in PE systems, when the current is not sinusoidal.

$$P_{tot} = \sum_{n=1}^{\infty} I_n^2 \cdot ESR_n \tag{1.10}$$

with the ESR evaluated at the specific frequency of each harmonic. [Has+16] shows that the results of the calculations fit well with the measured losses for an electrolytic capacitor. [NHS16] uses the Fourier analysis also for FDCCs with accurate results, although the Fourier transform applies only to linear systems and the behaviour of FDCCs is non-linear. However this is assumed to be not a problem because the voltage amplitude is kept small enough that the capacitance can be assumed to be linear.

2 State of the Art

In this chapter three possible measurement circuits are introduced to measure the impedance and hence the ESR of a dc biased capacitor. But first the open-short-load (OSL) calibration is introduced which is essential for most of the measurement circuits.

2.1 Open-Short-Load Calibration

The OSL calibration[1] can be used to mathematically remove systematic measurement errors. Hence a custom network to connect the device under test (DUT) to the VNA (or an other impedance measurement device) as well as parasitic resistances, inductances and capacitances can be removed by calculation.

A simplified schematic of a measurement with a connection network is shown in figure 2.1. The connection network to connect the DUT to the measurement device is modelled with a respective chain matrix. The matrix coefficients can be obtained by measuring known impedances. In the OSL calibration the DUT is replaced consecutively by an open circuit, a short circuit and a known load device e.g. a $50\,\Omega$ resistor. Each time the impedance is measured and together with the expected impedances (0 for short, ∞ for open and $50\,\Omega$ for load) it can be resolved for the chain matrix coefficients. The OSL calibration is performed individually at each frequency point to get a calibration over the whole frequency range. The calibration process described in this section is taken out of [Tec16].

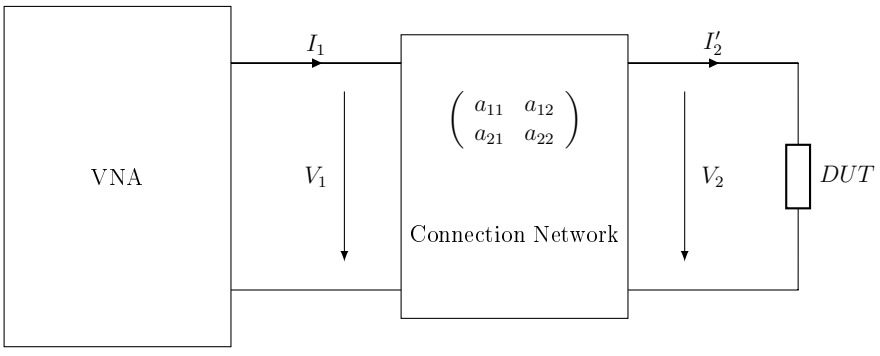

Figure 2.1: Impedance measurement circuit with an arbitrary connection network

The correlation between the input and output voltages of the connection network

[1] Also referred to as OSL correction or OSL compensation

shown in figure 2.1 is given by the equation

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_2 \\ I_2' \end{pmatrix} \tag{2.1}$$

where a_{11}, a_{12}, a_{21} and a_{22} are the coefficients of the chain matrix. V_1, V_2, I_1 and I_2' are the voltages and currents according to figure 2.1.

Using the calibration process the impedance of the DUT can be obtained for each frequency individually by applying the equation

$$Z_{dut} = \frac{(Z_s - Z_{xm})(Z_{sm} - Z_o)}{(Z_{xm} - Z_o)(Z_s - Z_{sm})} Z_{std} \tag{2.2}$$

where

Z_{dut} ... Corrected impedance of the DUT
Z_{xm} ... Measured impedance of the DUT
Z_o ... Measured impedance when the measurement terminals are open
Z_s ... Measured impedance when the measurement terminals are shorted
Z_{sm} ... Measured impedance of the load device
Z_{std} ... True value of the load device

The derivation of equation 2.2 is carried out in appendix A.

2.2 Series Circuit of Ac and Dc Source

[Tec16] describes a dc biased impedance measurement circuit using a series circuit of a dc voltage source and an ac voltage source as depicted in figure 2.2. The dc source is bypassed by a blocking capacitor, which blocks the dc voltage. Two coupled inductors prevent the ac current from flowing through the dc source. The current is measured with a circuit referred to as auto-balancing bridge (ABB) consisting of an operational amplifier (OA) and the resistor R_1. The ABB provides a so called virtual ground at the DUT, i.e. the potential is held at ground potential by the OA. The inputs of the OA are high-ohmic thus the current through the resistor R_1 has to be the same than the current through the DUT. The current can be calculated using R_1 and the voltage at the voltage probe. The impedance of the DUT can be calculated by the input voltage and the measured current if the voltage across C_{block} is either negligible small or the influence of C_{block} is removed by OSL calibration. Otherwise the voltage across the DUT has to be measured with an additional voltage probe.

[Tec16] states the maximum frequency of this simple ABB circuit consisting of an OA and a resistor is in the order of 100 kHz. Higher frequencies demand a more complex circuit.

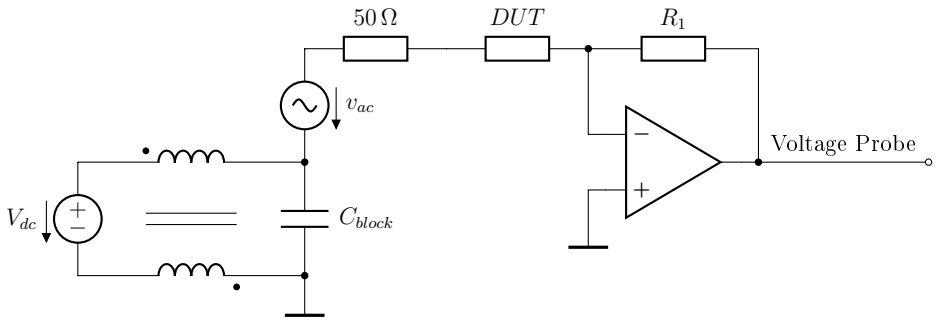

Figure 2.2: Series circuit of an ac and a dc voltage source and current measurement with an ABB

2.3 Measurement with Inductive Coupling

The measurement channels and especially the output of a VNA can be harmed when high voltage is attached. To overcome the destruction of the VNA by the high dc voltage the ac signal is injected inductively into the dc circuit as shown in figure 2.3.

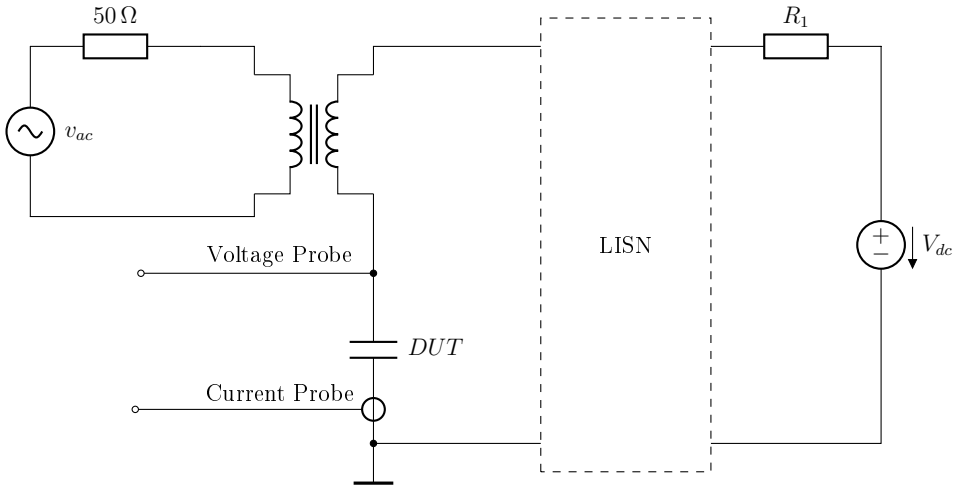

Figure 2.3: Dc biased impedance measurement circuit with inductive decoupling of the ac source

[Ham+14] proposes a measurement circuit similar to the circuit shown in figure 2.3. The circuit in the paper does not use the voltage probe though. The method is used with an line impedance stabilization network (LISN) to keep the impedance of the network including the dc voltage source constant. By using the voltage probe the error of the dc voltage source can be removed because the true current through the DUT and the true voltage at the DUT are measured. Depending on the voltage level at the DUT the voltage probe should provide resistive or capacitive decoupling.

The LISN should not only provide a constant impedance at the dc source, it should also prevent the ac signal to sink into the dc source and provide a low-ohmic path for

the ac signal. Thus the signal level is not damped to much by R_1. Maybe some kind of LC filter should be suited as a proper LISN.

In the paper also the error of the measurement circuit is discussed. Below 200 kHz and above about 8 MHz the error is relatively high, i.e. more than 10 %.

2.4 Two Capacitor Measurement

In the two capacitor measurement (TCM) the impedance of capacitors can be measured with dc bias using the circuit shown in figure 2.4. Two equal DUTs are connected in series. The capacitors are charged with a dc voltage source which is attached to the DUTs over a high-ohmic resistor. If the resistance of R is very high compared to the impedance of the series circuit, the measurement is not significantly affected.

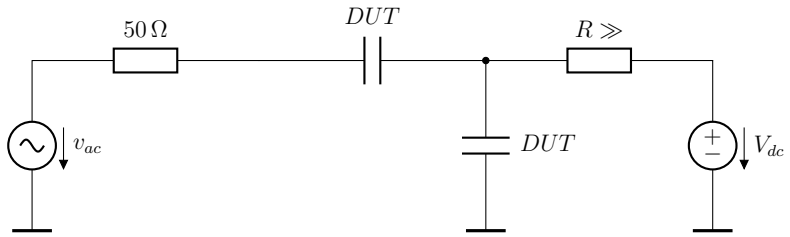

Figure 2.4: Dc biased impedance measurement circuit using two equal capacitors

A series circuit of two capacitors, each modelled as the classical equivalent circuit neglecting the ESLs is shown in figure 2.5. The total ESR and the total capacitance of the circuit can be calculated with the equations

$$ESR_{tot} = ESR_1 + ESR_2 \tag{2.3}$$

$$C_{tot} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}} \tag{2.4}$$

If both ESRs are equal the resulting total ESR, ESR_{tot}, is two times the ESR. If both capacitances are equal the resulting total capacitance C_{tot} is the half of each capacitance.

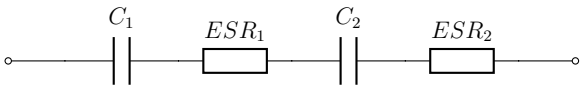

Figure 2.5: Series circuit of two real capacitors

So the capacitance of each DUT measured with the TCM is twice the measured capacitance. The ESR of each DUT is the half of the measured ESR.

Considering the three introduced measuring proposals an appropriate concept is derived in the next chapter.

3 Measurement Concepts

Based on the circuits described in the previous chapter a suitable measurement circuit for measuring the ESR of capacitors is developed in this chapter.

The circuit should be suited to be operated under the following conditions, as specified by the Company Omicron: The frequency range shall be at least 50 Hz to 50 MHz, thus also capacitors in mains applications can be measured. The measurable impedances shall lie in a range between 10 mΩ up to 100 kΩ. Dc bias up to 1000 V shall be able to be applied. The system has to be able to be operated with Omicron Lab's Bode 100 VNA.

The concept described in section 2.2 is difficult to realise since either the ac or the dc voltage source has to be floating. Also the simple ABB consisting of an OA and a resistor is described to be not suited for frequencies above about 100 kHz and is assumed to be complex in development otherwise. For these reasons this circuit is not further analysed.

In section 2.3 a measurement circuit with inductive decoupling of the ac source is described. A unknown network for decoupling the dc source from the DUT is used. The impedance can be measured using a current probe and optionally an additional voltage probe. The error becomes relatively high below about 200 kHz and above circa 8 MHz. Due to the error aspect and the relatively high complexity with transformer, current probe and impedance matching network the approach is not considered further.

3.1 Two Capacitor Measurement

The TCM described in section 2.4 circuit is very simple to build up. There are uncertainties how much the dc voltage source actually influences the measurement results though. Thus the circuit is simulated via ac simulation in the simulation program Qucs.

For the simulation the output impedance of the dc source[1] used for further measurements is modelled. Therefore the output impedance is measured at 0 V and at 1000 V, the highest voltage. The output impedance is measured according to the setup shown in figure 3.1. The dc voltage is blocked with a linear 7 µF polypropylene capacitor. The VNA measures the impedance via the voltage drop across the 50 Ω output resistor and the known ac voltage level. The impedance of the 7 µF capacitor is mathematically removed using the OSL calibration.

Figure 3.2 shows the output impedance of the voltage source at 50 V (green) and 1000 V (grey). The impedance curve exhibits a relatively flat impedance at lower frequencies. Then the output capacitor lets the curve decrease until the inductance of the

[1] The voltage source is a SPS-24-1000P-30 source from Dean Technology

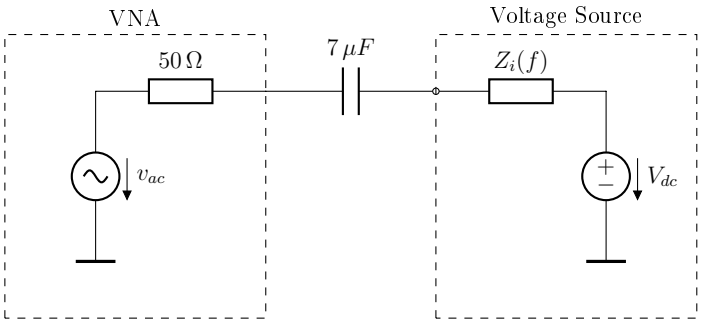

Figure 3.1: Measurement setup for the output impedance measurement of a voltage source

measurement path increases the impedance. The impedance drops at low frequencies when the voltage is increased. Also the output capacitance decreases with increasing voltage. This may be caused by the voltage dependence of used FDCCs.

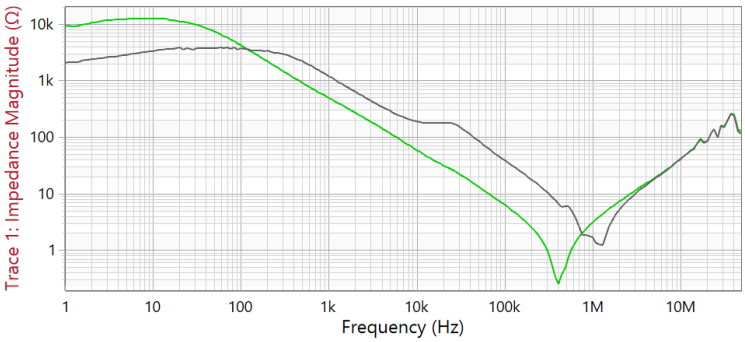

Figure 3.2: Output impedance of the used voltage source at 50 V (green) and 1000 V (grey)

The output impedance is modelled with the circuit shown in figure 3.3. The model is designed to fit the grey curve at 1000 V.

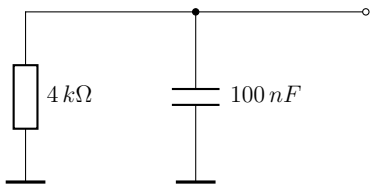

Figure 3.3: Output impedance model of the used voltage source

The impedance model of the voltage source is inserted into the simulation. The simulation schematic is depicted in figure 3.4. The two DUTs are modelled with a capacitance and an ESR each time.

Figure 3.5 shows the simulation of the measured capacitance. The red curve shows the simulation including the dc source. The blue curve shows the ideal measurement

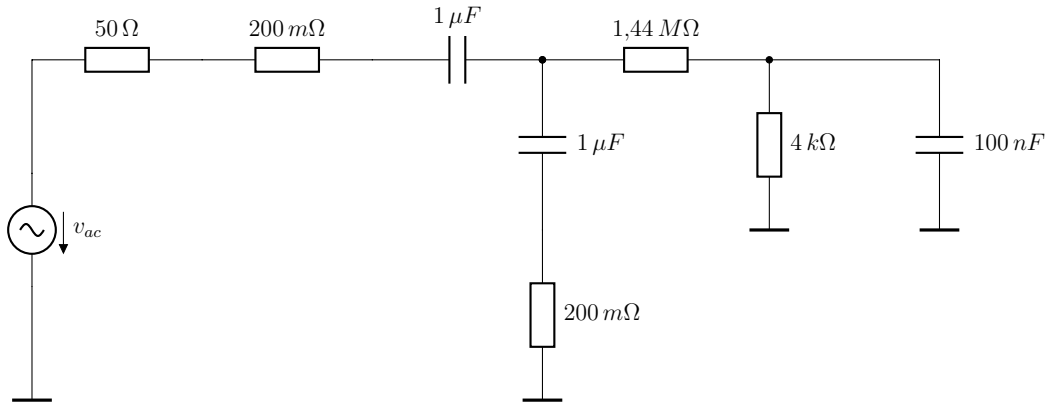

Figure 3.4: Schematic of the error simulation of the TCM

results without the influence of the dc source. The error of the capacitance measurement is below 1 % over the whole simulated frequency range.

Figure 3.6 shows the simulation of the ESR measurement. The red curve is again the simulation including the dc source and the blue curve is the true value. It can be seen that the ESR deviates below about 1 kHz for this specific parameters. The dc source leads to an error in the ESR which is decreasing with a factor $^1/_{100}$, or −40 dB, respectively per decade. In section 1.4 the ESR of FDCCs is described as falling with a factor $^1/_{10}$, or −20 dB, respectively per decade for lower frequencies. Thus a stronger decrease of the ESR than $^1/_{10}$, or −20 dB per decade in a measurement is an indication for a measurement error induced by the dc source.

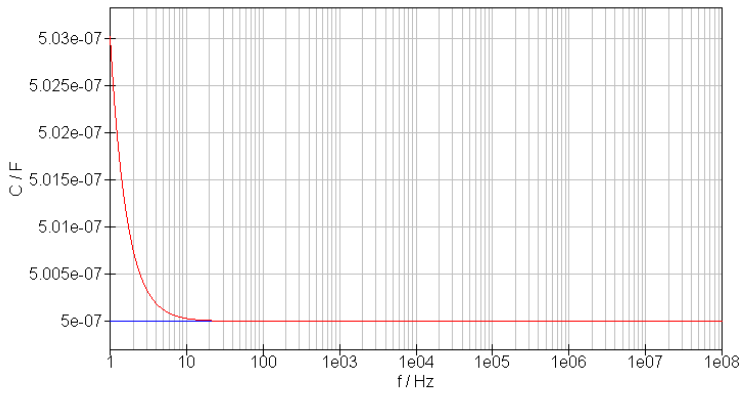

Figure 3.5: Simulated capacitance of the TCM. Red: simulation of the measured capacitance; blue: ideal capacitance

This simulations show that the TCM is suited for the measurement of the capacitance rather than the measurement of the ESR in the desired frequency range. However the capacitance measurement works very well thus the circuit is used for further verifications of developed measurement circuits.

As an improvement of the measurement circuit one of the DUTs can be replaced by a

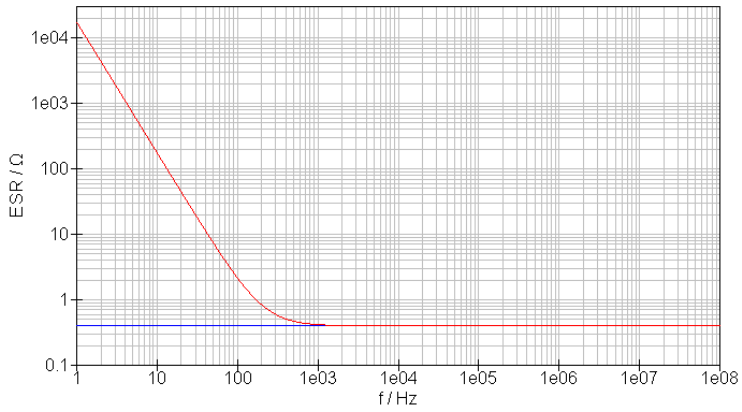

Figure 3.6: Simulated ESR of the TCM. Red: simulation of the measured ESR; blue: ideal ESR

linear capacitor, e.g. a film, or a C0G capacitor which does not change its capacitance with dc bias. Then the other DUT can then be measured individually. Based on this thought a measurement bridge is developed in the next section.

3.2 Measurement Bridge

Figure 3.7 shows an adapted circuit of the TCM introduced in the previous section. In contrast to the TCM one DUT is interchanged with a linear capacitor C_1. Again the dc voltage source is decoupled with a high-ohmic resistor R_5. A shunt resistor R_3 is inserted to measure the current flow through the DUT and a voltage divider (R_1 and R_2) to measure the voltage drop over C_1, the DUT and R_3 if the resistor R_5 is very high. The voltage over the DUT can be calculated using the OSL calibration. The resistor R_4 is inserted for termination for high frequency signals.

A changing output impedance of the dc voltage source after OSL calibration, e.g. with dc voltage (like e.g. shown in the measurement depicted in figure 3.2 on page 21) could possibly corrupt the measurement. Thus an adapted circuit is shown in figure 3.8. In this circuit the voltage over the DUT and R_3 is measured by the voltage divider. Assuming all resistors and capacitors (except the DUT) to be constant over dc voltage a changing output impedance of the dc source would not affect the measurement of the DUT. The voltage at the voltage divider still represents the voltage drop over the DUT and the voltage at the shunt R_3 still represents the current through the DUT.

The measurement bridge circuit is further developed and investigated in the next chapter.

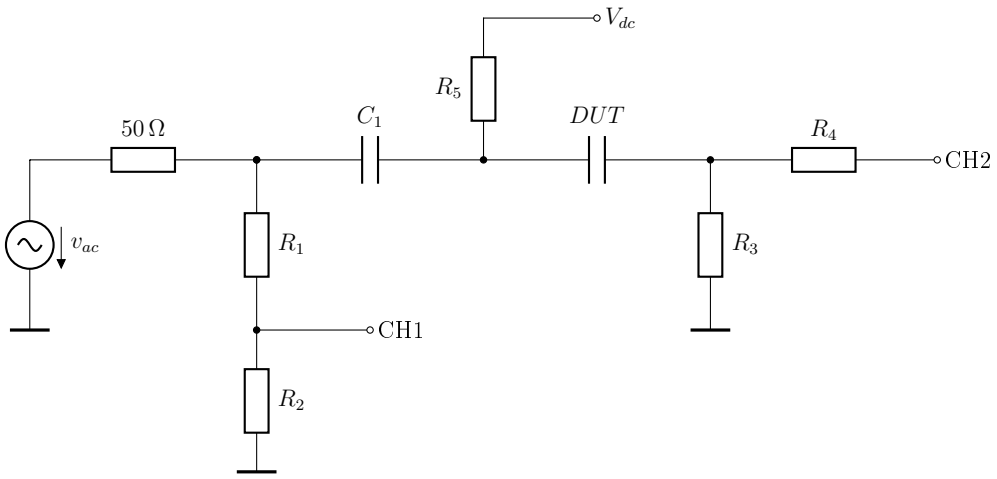

Figure 3.7: Circuit of a possible impedance measurement bridge

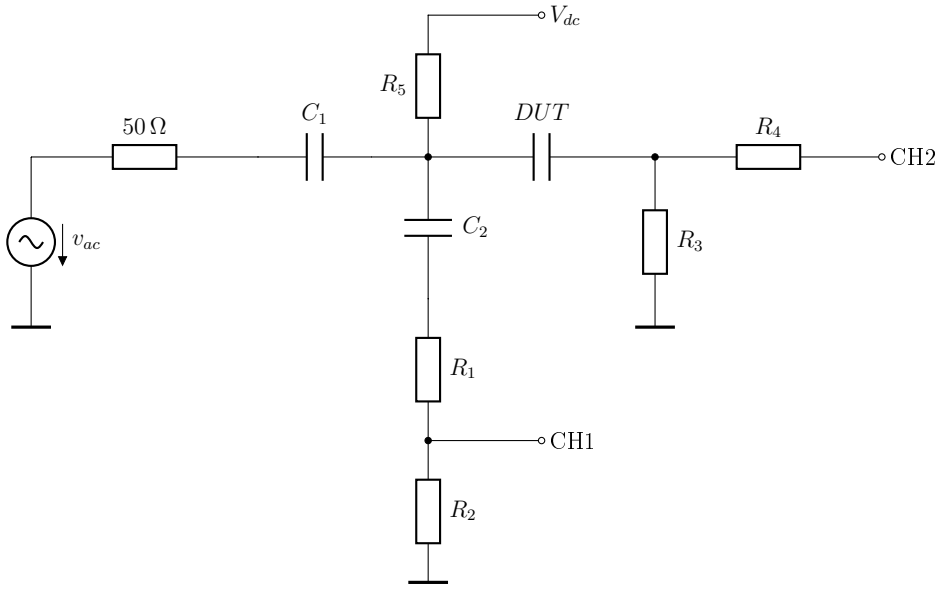

Figure 3.8: Circuit of the improved impedance measurement bridge

4 Measurement Bridge

The in the previous chapter 3.2 presented measurement circuit is now investigated more detailed to figure out if it is suitable.

4.1 General Design

The capacitors C_1 and C_2 need a high capacitance to not attenuate the signal level to much at lower frequencies. The capacitor C_1 needs a high capacitance to pass much signal, while there is no special need for linearity. The impedance is calculated only using the signals at CH1 and CH2; distortions due to an un-linearity of C_1 are removed by input filters of the VNA's measurement channels. The capacitor C_2 needs to be very linear, as further investigations in the section 4.3 show. However for this design the capacitors C_1 and C_2 are both chosen to be polypropylene film capacitors with a capacitance of $7\,\mu$F and a rated voltage of 1100 V. A list of all used and measured capacitors can be found in Appendix B.

The resistors R_1 and R_2 are designed to step down the voltage by a factor of about $1/20$, while the resistor R_2 acts as a termination and is $50\,\Omega$. Thus R_1 is $1\,\text{k}\Omega$. R_3 is a shunt resistor for current measurement and is designed to be $2{,}35\,\Omega$. R_4 is also for termination and equals $50\,\Omega$. R_5 provides an ohmic decoupling of the dc source and limits the charging current of the capacitors. It is designed to be $40\,\text{k}\Omega$.

4.2 Parameter Sweep Simulation

The purpose of this simulation is to obtain the voltage levels at the measurement channels 1 and 2 with varying frequency and impedance. Thus the frequency and impedance range can be estimated in which the circuit can be operated. Therefore the resistance of the DUT is swept from $1\,\text{m}\Omega$ to $1\,\text{M}\Omega$. Also to frequency is swept from 1 Hz to 10 MHz in steps of one per decade. Figure 4.1 shows the schematic of the simulation. The input is a dc voltage source with an output voltage of 2 V. The impedance of the reactances X_C is calculated with $X_C = 1/2\pi fC$, where $C = 7\,\mu$F.

Figure 4.2 shows the simulation result of the parameter sweep measurement. The blue curves show the levels of the voltage at channel 1 at the respective frequency, the red curves the levels at channel 2. The direction of increasing frequency is denoted.

The lowest voltage levels to measure occur at the combination of low impedances and low frequencies (at channel 1) and generally at high frequencies at channel 2. The Bode 100 VNA is able to measure voltages as small as $1\,\mu$V. Only the curve representing 1 Hz is partially below this level. All others are above and thus measurable.

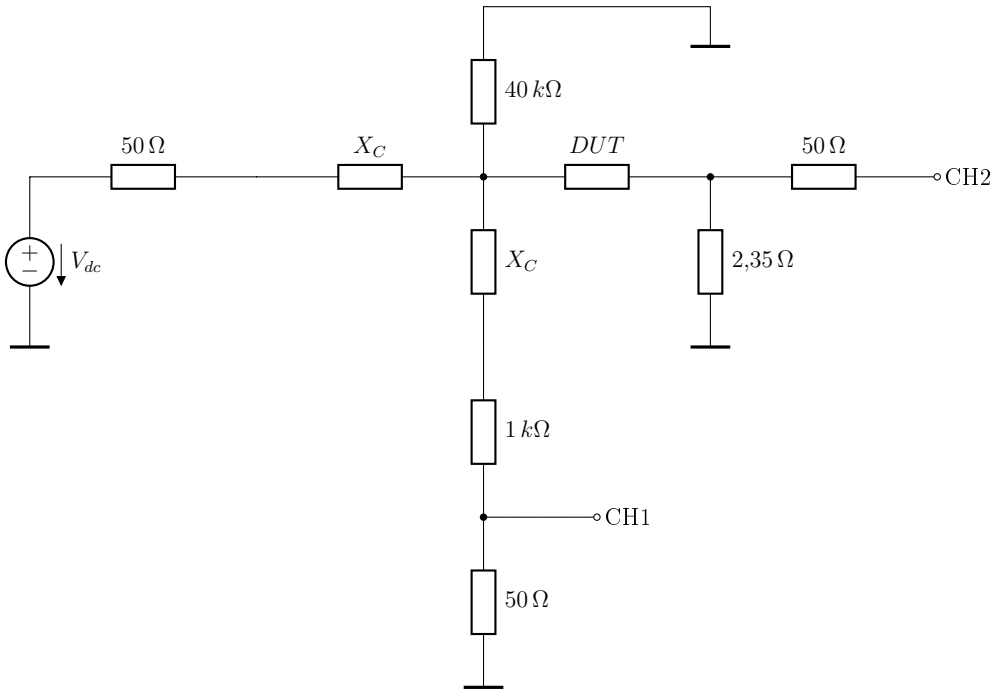

Figure 4.1: Schematic of the parameter sweep simulation

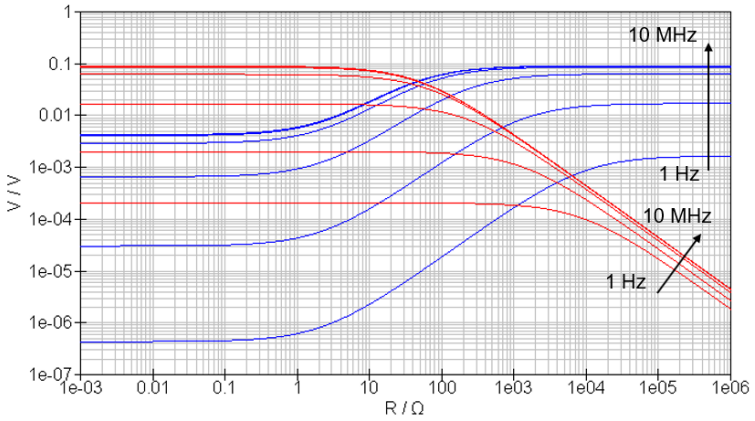

Figure 4.2: Simulation of the voltage against the impedance of CH1 (blue) and CH2 (red)

4.3 Influence of Capacitance Change

The simulations and calculations do only apply if all used components are linear and do not change their behaviours over dc bias. It is assumed that all resistors remain stable over the whole dc voltage range but the capacitors not necessarily. A TCM as introduced in section 2.4 of the further used 7 μF polypropylene capacitor is shown in figure 4.3. The figure shows the capacitance (blue) and the temperature (red) versus the time. The measurement starts at 0 V bias and every six hours the bias voltage is

increased by 100 V up to 1000 V.

The capacitor changes its capacitance with applied dc voltage from 3,434 μF to 3,446 μF, i.e. a change of about 0,35 % when changing the dc voltage form 0 V to 1000 V. A relatively linear correlation between voltage and capacitance is observed. Comparing the capacitance and the temperature it can be seen that the capacitance drifts rather because of the temperature than because of the time. During a time interval of constant voltage the capacitance does not change when the temperature is constant (e.g. between hour 60 and hour 66).

How a change of the capacitor C_2 influences the impedance measurement has to be investigated.

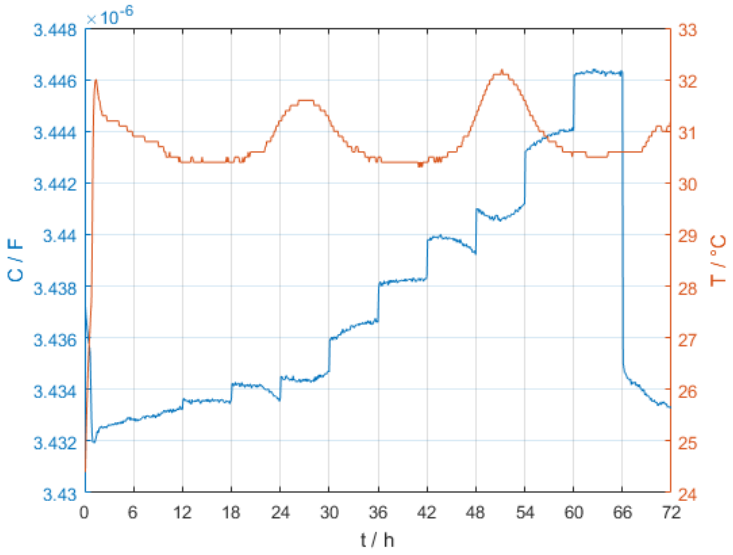

Figure 4.3: Capacitance change over voltage and time. Blue: capacitance; red: ambient temperature

4.3.1 Error Simulation

The error due to a change in the capacitance of C_2 is simulated with the circuit shown in figure 4.4. The circuit is OSL calibrated (by using a short, an 100 Ω resistor and an open circuit, respectively) according to section 2.1. After the calibration the capacitor C_2 is changed by 0,35 % from 7 μF to 7,025 μF and the error is simulated.

The simulated relative errors are calculated using the equations

$$\varepsilon_{\varphi_{rel}} = \left| \frac{\varphi_2 - \varphi_1}{\varphi_1} \right| \cdot 100\,\% \tag{4.1}$$

$$\epsilon_{Z_{rel}} = \left| \frac{|Z_2| - |Z_1|}{|Z_1|} \right| \cdot 100\,\% \tag{4.2}$$

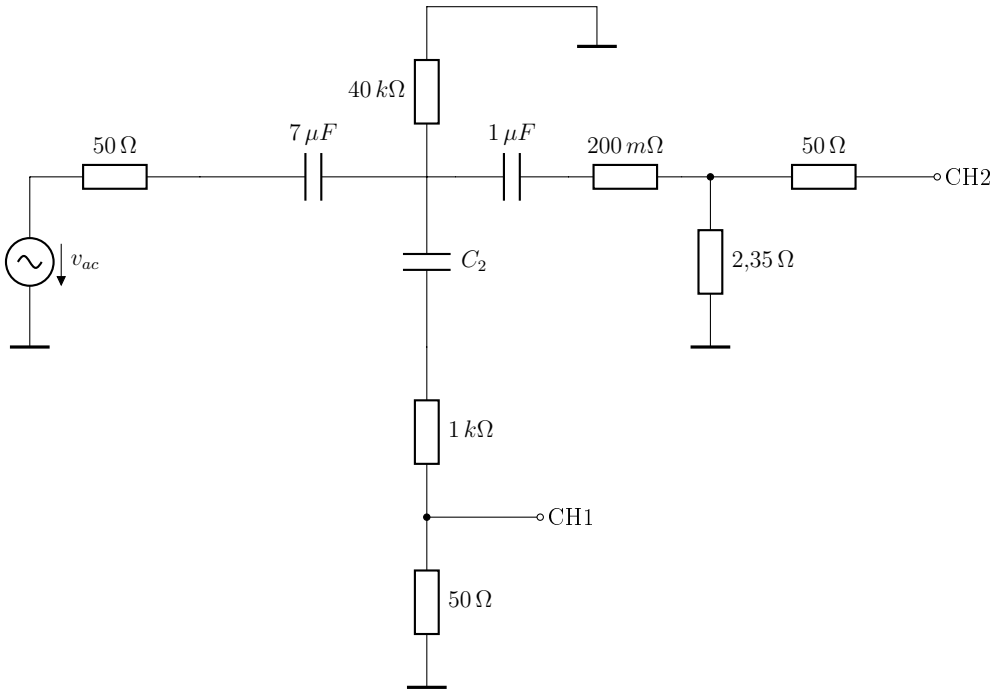

Figure 4.4: Schematic of the error simulations

$$\varepsilon_{C_{rel}} = \left| \frac{C_2 - C_1}{C_1} \right| \cdot 100\,\% \tag{4.3}$$

$$\varepsilon_{ESR_{rel}} = \left| \frac{ESR_2 - ESR_1}{ESR_1} \right| \cdot 100\,\% \tag{4.4}$$

Figure 4.5 shows the modulus of the relative error of phase (blue) and magnitude (red). These are calculated with the equations 4.1 and 4.2. The magnitude error is at max approximately 0,35 %. The phase error reaches its maximum at approximately 20 Hz, where it is about 0,11 %.

Figure 4.6 shows the relative error of the capacitance (blue) and the ESR (red). The relative errors are calculated with the equations 4.3 and 4.4. While the capacitance error remains below 1 % over the whole frequency range the ESR error increases up to over 10.000 % at low frequencies.

The in section 1.4 introduced approximation for the ESR of an FDCC is applied on a measured FDCC. Figure 4.7 shows the measurement (blue) and the approximation (red). The ESR is approximated with the once again written equation

$$ESR_{FDCC} = \frac{k_s}{f} + ESR_0 \tag{4.5}$$

The ESR_0 is the smallest ESR value and is measured to be 27,5 mΩ at a frequency of 1,26 MHz. The value k_s is evaluated at a frequency of 6897 Hz where the ESR is 700 mΩ

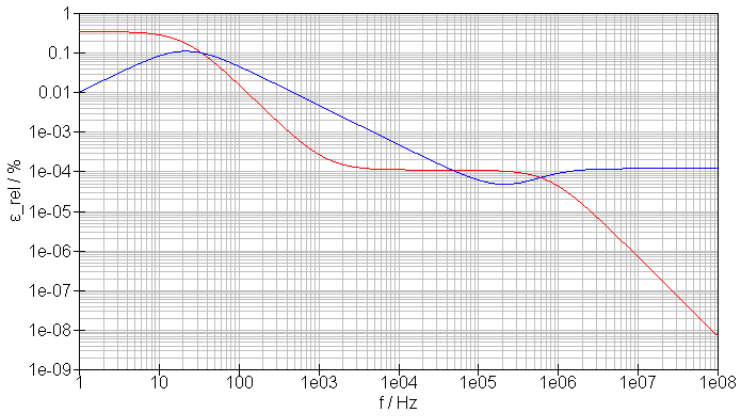

Figure 4.5: Simulation of the relative magnitude error (red) and the relative phase error (blue)

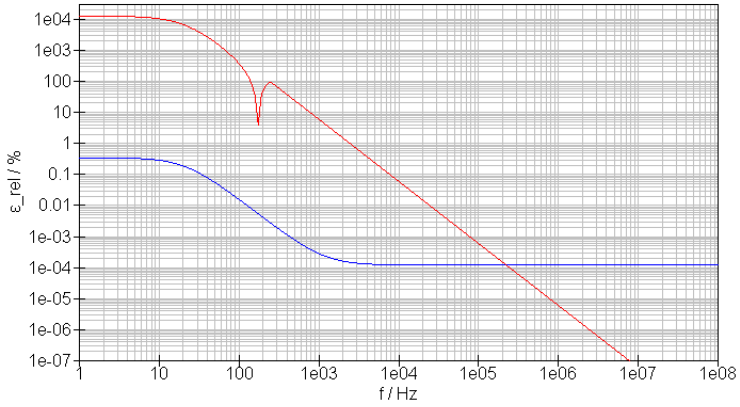

Figure 4.6: Simulation of the relative ESR error (red) and the relative capacitance error (blue)

and is calculated with

$$k_s = (ESR_{FDCC} - ESR_0)\, f = 4636\,\Omega Hz \tag{4.6}$$

The ESR model described in equation 4.5 is inserted into the simulation. The circuit and the OSL calibration process remain the same as in shown in figure 4.4, only the 200 mΩ resistor is replaced by the frequency dependent model. The capacitance is changed to 330 nF to get the right results for this specific capacitor.

Figure 4.8 shows the relative error of both, the ESR (red) and the capacitance (blue). Comparing this figure with figure 4.6 it is seen that the error of the capacitance is still the same while the ESR error is reduced significantly.

Figure 4.9 shows the capacitance error like shown in figure 4.8. This time the capacitance of the DUT is swept logarithmically from 1 nF to 100 μF with one curve per decade.

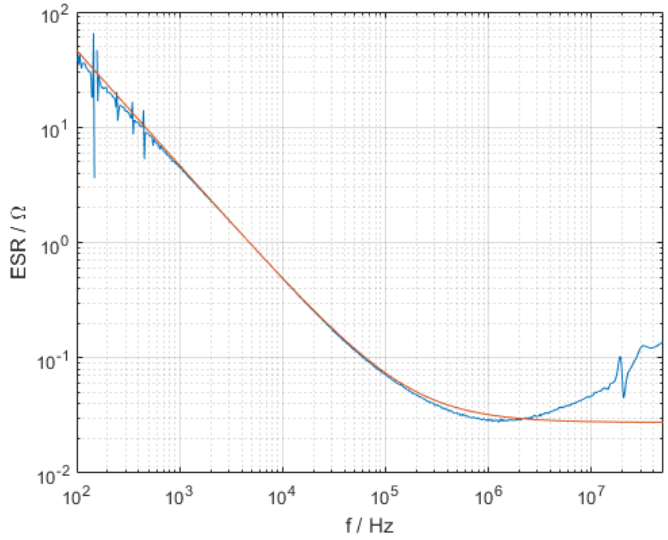

Figure 4.7: Measured and modelled ESR of an FDCC. Blue: measured ESR; red: modelled ESR

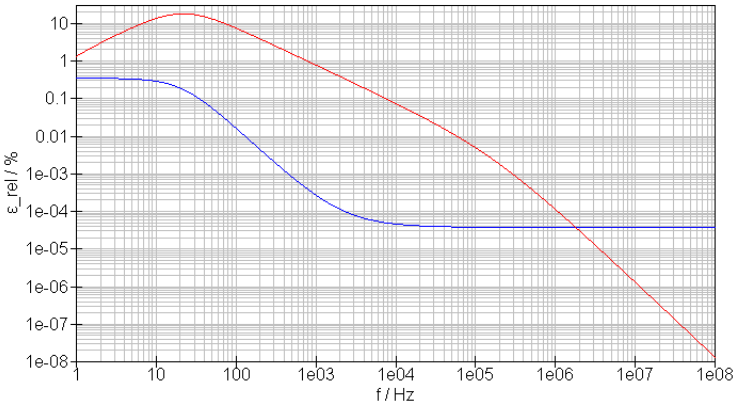

Figure 4.8: Simulation of the relative ESR error (red) and the relative capacitance error (blue) of an FDCC

The simulation shows that the relative error remains below 1 % for all capacitances over the whole frequency range. The relative ESR error is not included in the simulation. While the capacitance can be assumed to be constant over frequency for most capacitors, the ESR model is more complex and its behaviour is depending on more parameters (dimensions, dielectric, etc.). Thus an ESR error simulation is much more complex and is more meaningful when performing in each case individually if necessary.

This simulations show that the circuit is suited for the ESR measurement of capacitors with an ESR behaviour as described in equation 4.5. For capacitors with an other ESR behaviour the error could be significantly higher. A drastically increasing, or decreasing ESR with changing dc bias should hence be brought into question.

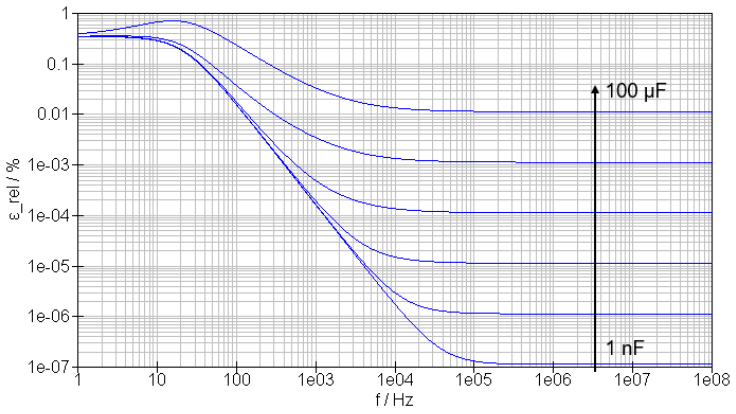

Figure 4.9: Simulation of the relative capacitance error over frequency and capacitance

The ESR error remains below 20 % for FDCCs which is acceptable for further measurements. Nevertheless a possible solution for a high voltage OSL calibration is introduced shortly in the next section.

4.3.2 Possible Circuit for Error Removal

The error introduced in section 4.3.1 can be removed when the OSL calibration is performed when the capacitor C_2 is dc biased. If the capacitance of C_2 does not change after calibration there is also no additional error due to capacitance change. Figure 4.3 on page 27 shows changes in capacitance only with voltage and temperature. If the temperature and the voltage are assumed to be constant no capacitance change is expected.

A small change in the measurement circuit can enable the calibration with applied dc bias an is shown in figure 4.10. The capacitor C_2 is split into two capacitors C_2 and C_3. During the calibration process the half of the voltage V_{dc} is applied in between them. During short and load calibration the voltage at the point between C_1, C_2 and R_5 is approximately 0 V[1]. During the open calibration and the measurement with the DUT the voltage at the same point is V_{dc}, when all capacitors are fully charged. Thus the voltage at C_2 is either $V_{dc} - {}^{V_{dc}}/_2 = {}^{V_{dc}}/_2$ or ${}^{V_{dc}}/_2 - 0\,\mathrm{V} = {}^{V_{dc}}/_2$. If the voltage change in the film capacitor is not dependent on the polarity, the OSL calibration can indeed be done at the specific dc bias point.

The relatively complex calibration process and the high amount of error sources during calibration makes this concept very unhandy. Since in the previous section the error is stated to be low with FDCCs and the focus of the thesis is in FDCCs the original measurement bridge without the high voltage calibration variant is used for further measurements.

[1] If the resistor for the load calibration is very much smaller than R_5

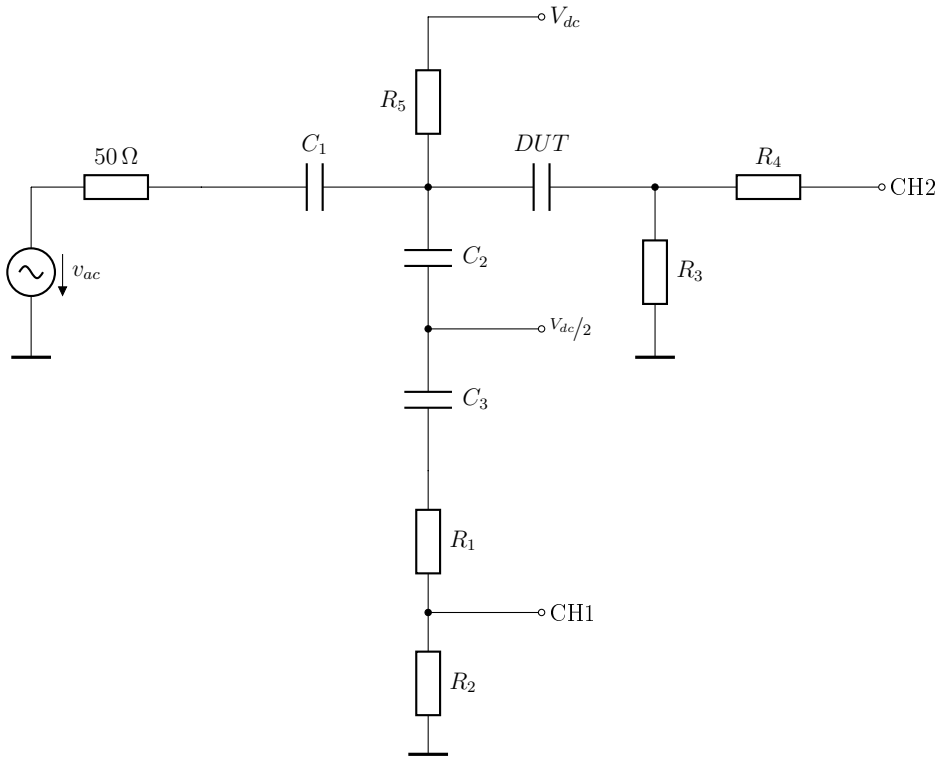

Figure 4.10: Possible circuit for a dc biased OSL calibration

4.4 Measurement Verification

The measurement bridge is verified with the measurement of a well known and stable element. Thus a 68 nF C0G capacitor is measured at 0 V, then at 1000 V and again at 0 V over 8 h for each plateau. The measurement is done one time using the TCM described in section 2.4 and one time using the developed measurement bridge. The measurements are then compared. The measurements are performed at 998,9 Hz every five minutes.

Figure 4.11 shows the magnitude of the capacitor measurement with the measurement bridge (blue) and the TCM method (red). The magnitude of the TCM is divided by two since the measurement of two capacitors results in twice the magnitude. The yellow curve is the magnitude of the ideal 68 nF capacitor. Naturally the blue and the red curves do not exhibit the same magnitude since real components have a specific capacitance tolerance, in this case $\pm 5\,\%$. The trend of both measurements is the same when 1000 V is applied. Also both measurement do not exhibit drift over time.

Figure 4.12 shows the phase of the two measurements. The phase does not change when two capacitors are measured in series. Thus both phases are the real measured phases. The blue curve again belongs to the measurement with the measurement bridge and the red curve belongs to the TCM. Both measurements exhibit noise of the same order. No systematic phase change is visible at the transition between 0 V and 1000 V. The blue curve does not exhibit drift during time and the red one shows only a minor

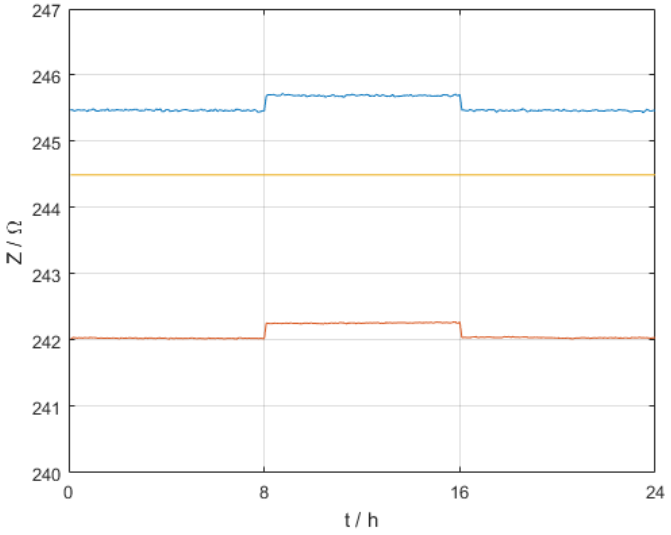

Figure 4.11: Magnitude of the C0G capacitor over time. Blue: measurement bridge; red: TCM divided by two; yellow: ideal

drift which is most likely caused by temperature changes.

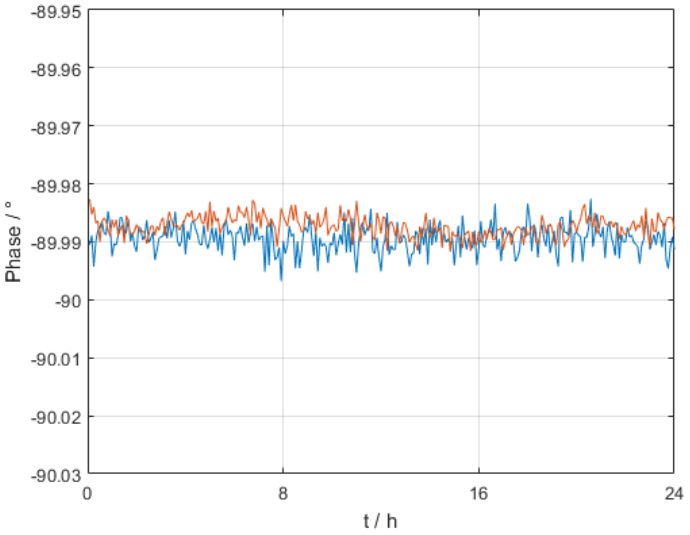

Figure 4.12: Phase of the C0G capacitor over time. Blue: measurement bridge; red: TCM

This measurements show that neither the magnitude nor the phase measurement with the measurement bridge exhibits different behaviour than the measurement with the TCM. Also in terms of time dependence the circuits behave the same. Thus the measurement with the measurement bridge is assumed to be suited for further measurements.

5 Dc Biased ESR Measurement

The measurement circuit introduced in chapter 4 is now used to measure the ESR and also the capacitance of different capacitors. The results are then compared.

5.1 Capacitor Comparison

The ESR and the capacitance of different capacitors of different technologies is measured over frequency and dc bias. The capacitors are one electrolytic capacitor (e-cap), one film capacitor, one non-ferroelectric CC (C0G) and two FDCCs. The two FDCCs are one X7R capacitor and one CeraLink capacitor. The dc voltage is varied over the respective rated voltage range of each capacitor[1]. The parameters are measured 10 minutes after the voltage is adjusted to overcome initial capacitance and ESR changes, respectively, which are described in [Nov+11].

The measured capacitors are listed in table 5.1. More precise information about the capacitors can be found in appendix B.

Table 5.1: Capacitors of the further measurements with rated capacitance, rated voltage and respective colour used in the plots

Capacitor	C_{rated} in μF	V_{rated} in V	Colour
CeraLink	1	500	blue
E-cap	1	450	red
X7R	0,33	630	yellow
Film	0,33	400	violet
C0G	0,068	1000	green

The applied voltage at the DUT is not constant over the frequency since the impedance of the DUT varies over frequency. Also due to impedance changes caused by capacitance changes the applied voltage at the DUT is not constant over dc voltage. A varying voltage level on the DUT can possibly lead to a measurement error, as described in section1.3. Due to the very high rated voltages of all measured capacitors this effect is neglected.

Figure 5.1 shows the capacitance of the five capacitors versus frequency. The measurements are done without dc bias. The colour convention for the capacitors is as listed in table 5.1. This convention is valid for all measurements in this section except the last one. All capacitors exhibit a constant capacitance over the frequency except the e-cap.

[1]Except for the X7R, where the dc bias is varied up to 600 V and the rated voltage is 630 V

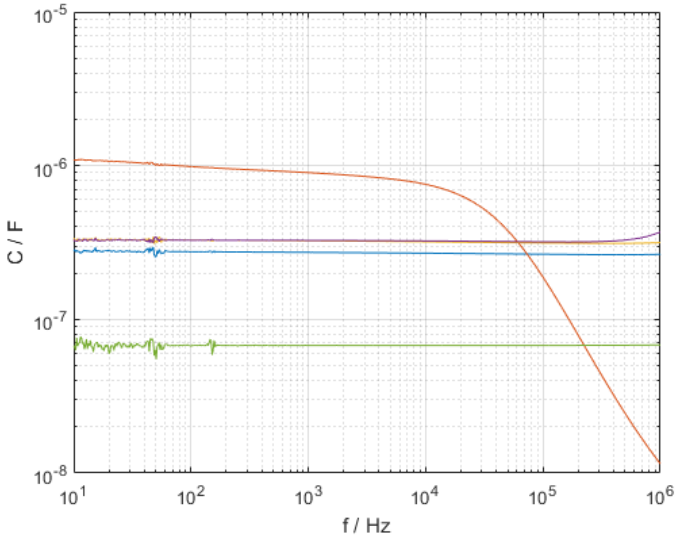

Figure 5.1: Capacitance of capacitors versus frequency without dc bias. Blue: CeraLink; red: e-cap; yellow: X7R; violet: film; green: C0G

Figure 5.2 shows the ESR of the measured capacitors versus frequency without dc bias. The colours are again the same. The ESR of the film, X7R and CeraLink capacitors have a similar behaviour. The ESR of the C0G is plotted from 1 kHz on since it is too noisy below. The ESR of the e-cap is significantly higher.

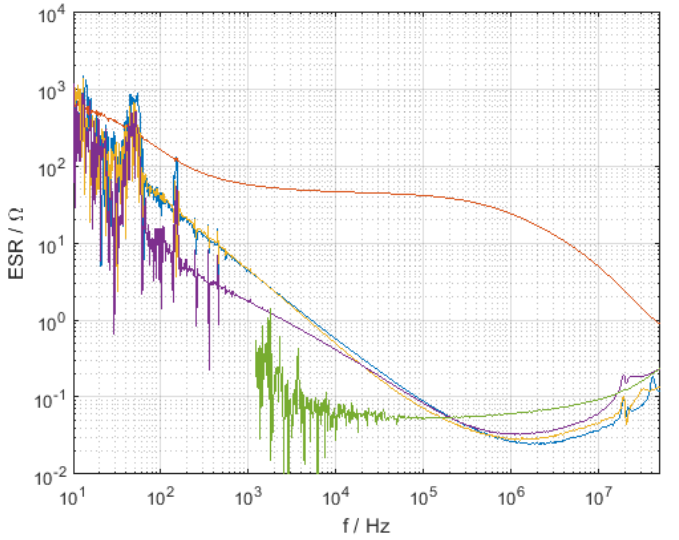

Figure 5.2: ESR of capacitors versus frequency without dc bias. Blue: CeraLink; red: e-cap; yellow: X7R; violet: film; green: C0G

Figure 5.3 shows the relative capacitance change of the capacitors referred to the capacitance at 0 V. The capacitances are measured at 1022 Hz. The capacitance of

the e-cap, the film and the C0G are constant over the whole voltage range. While the capacitance of the X7R capacitor decreases with dc voltage, the capacitance of the CeraLink increases and then decreases again.

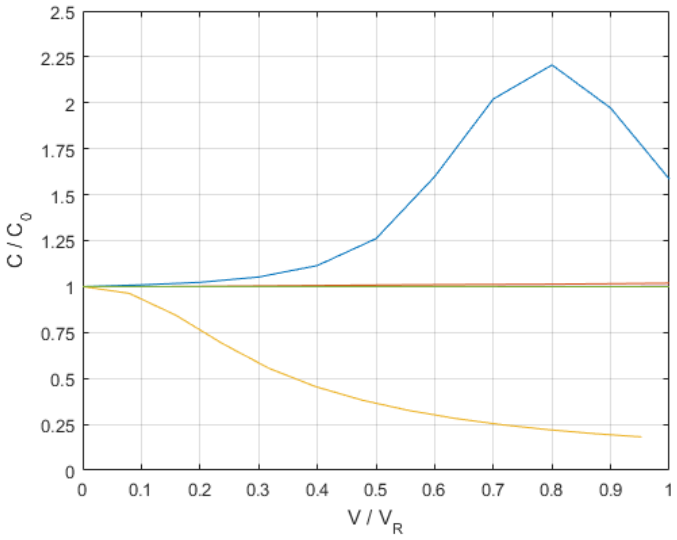

Figure 5.3: Relative capacitance change of capacitors with dc bias. The capacitance is referred to the capacitance without dc bias. The voltage is referred to the rated voltage. Blue: CeraLink; red: e-cap; yellow: X7R; violet: film; green: C0G

Figure 5.4 shows the relative ESR change of the capacitors referred to the ESR at 0 V. The ESRs are measured at 1022 Hz, except of the C0G capacitor which ESR is measured at 100,6 kHz. The ESR of the film and the e-cap are constant over the frequency. The ESR of the X7R increases while the ESR of the C0G decreases. The ESR of the CeraLink capacitor increases and decreases with a similar slope than the capacitance. ESR measurement errors like discussed in section 4.3 should not influence these measurements because of the following reasons:

- The X7R and the Cera Link capacitor are both FDCCs and show a typical FDCC ESR behaviour as seen in figure 5.2. This behaviour is stated in section 4.3.1 to exhibit a small error.
- The ESR of the film capacitor is similar to the ESR of the FDCCs thus a similar behaviour of the error is expected. Also the ESRs of the e-cap and the film capacitor do not change essentially over the rated voltage. A changing ESR with dc bias and a measurement error which removes the change again would be very unlikely.
- The ESR of the C0G is evaluated at a very high frequency where the error is anyway negligible small.

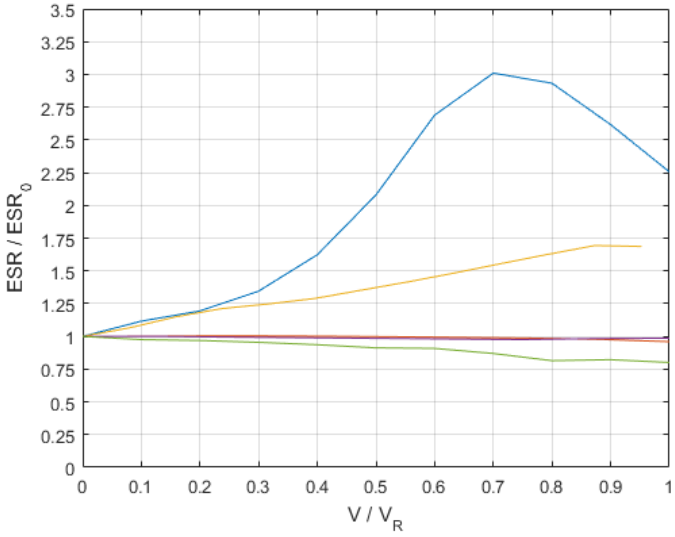

Figure 5.4: Relative ESR change of capacitors with dc bias. The ESR is referred to the ESR without dc bias. The voltage is referred to the rated voltage. Blue: CeraLink; red: e-cap; yellow: X7R; violet: film; green: C0G

Figure 5.5 shows the ESR of the X7R capacitor over frequency. The colours refer now to: blue (0 V), red (150 V), yellow (300 V), violet (450 V) and green (600 V). It can be seen that the PR increase in amplitude with applied dc bias.

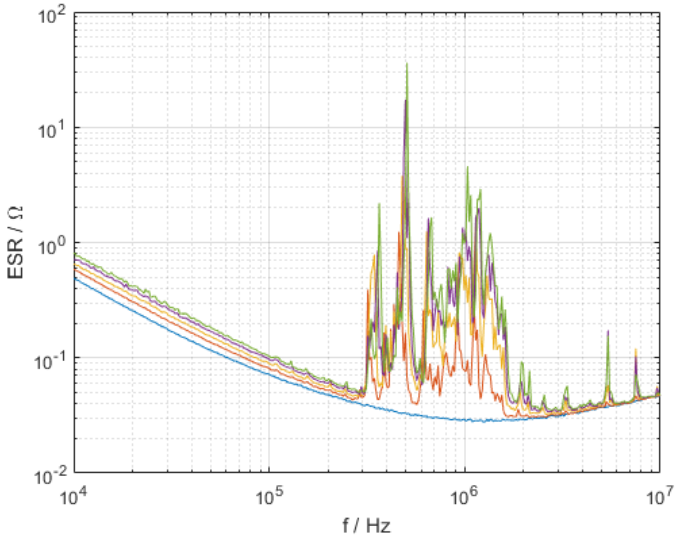

Figure 5.5: ESR versus frequency with dc bias. Blue: 0 V dc bias; red: 150 V; yellow: 300 V; violet: 450 V; green 600 V

The time dependence of the PR is investigated in the next section.

5.2 Piezoelectric Resonance Drift over Time

A measurement of the ESR of an 22 μF FDCC over 12 hours is performed to investigate if the PR remain at the same frequency over time. Figure 5.6 shows the ESR with a PR versus frequency. The blue curve shows the initial ESR after attaching 50 V. The red curve shows the ESR after six hours and the yellow curve shows the ESR after 12 hours. The PR changes in frequency over time.

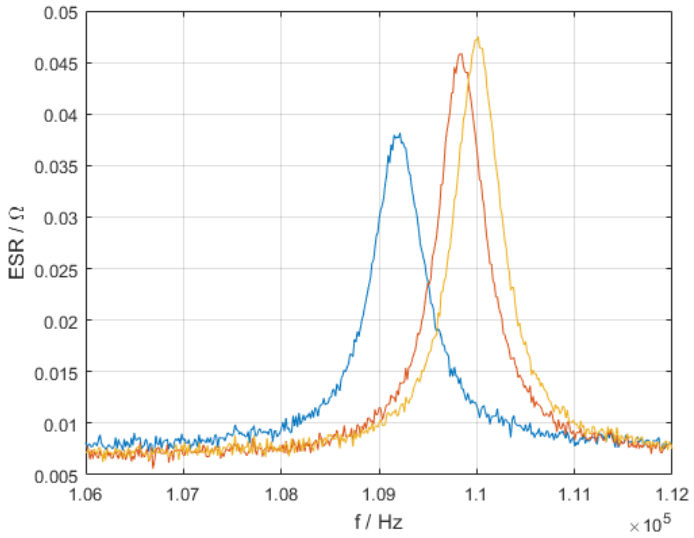

Figure 5.6: PR frequency after attaching dc bias. Blue: initial; red: after 6 hours; yellow: after 12 hours

Figure 5.7 shows the frequency of the PR over time in blue. The PR frequency increases over time. The red curve shows the ambient temperature over the same time.

Figure 5.8 shows again the frequency of the PR over time. In this case also the capacitance is depicted in red. It seems to be a correlation of the increase of resonance frequency and decrease of capacitance. It is not clarified if one of these two parameters depends on the other, or they both depend on a third parameter (e.g. component temperature).

The behaviour of the PR is not further investigated since it would be beyond the resources of this thesis. However this analysis shows that in further loss measurements at the PR the frequency of the peak has to be measured simultaneously.

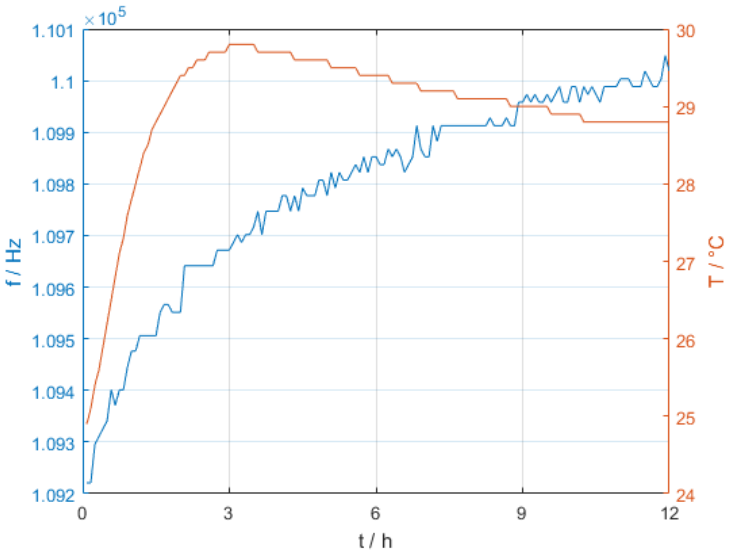

Figure 5.7: PR frequency (blue) and ambient temperature (red) over time after attaching dc bias

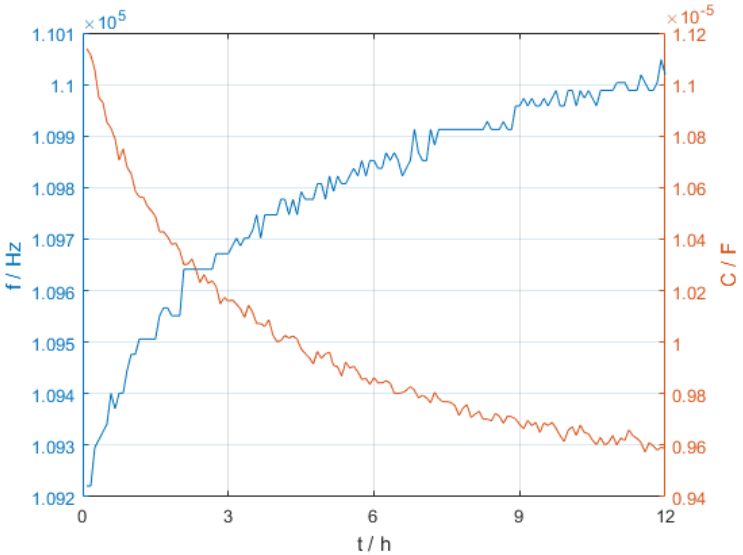

Figure 5.8: PR frequency (blue) and capacitance (red) over time after attaching dc bias

6 Loss Measurement in Power Electronics Application

The power loss is measured in a typical PE application to verify the influence of the ESR and especially the PR on the losses. The losses are measured with a CMS.

6.1 Calorimetric Loss Measurement

A CMS is built up according to figure 6.1. The setup includes a container filled with transformer oil surrounded by polystyrene. Three elements are immersed in the oil: the DUT, a Pt100 temperature sensor for measuring the internal temperature and a resistor. The resistor is used to determine the thermal resistance between the oil and the ambient air. An additional Pt100 temperature sensor is used to measure the ambient temperature to further calculate the temperature difference between the oil and the ambient air.

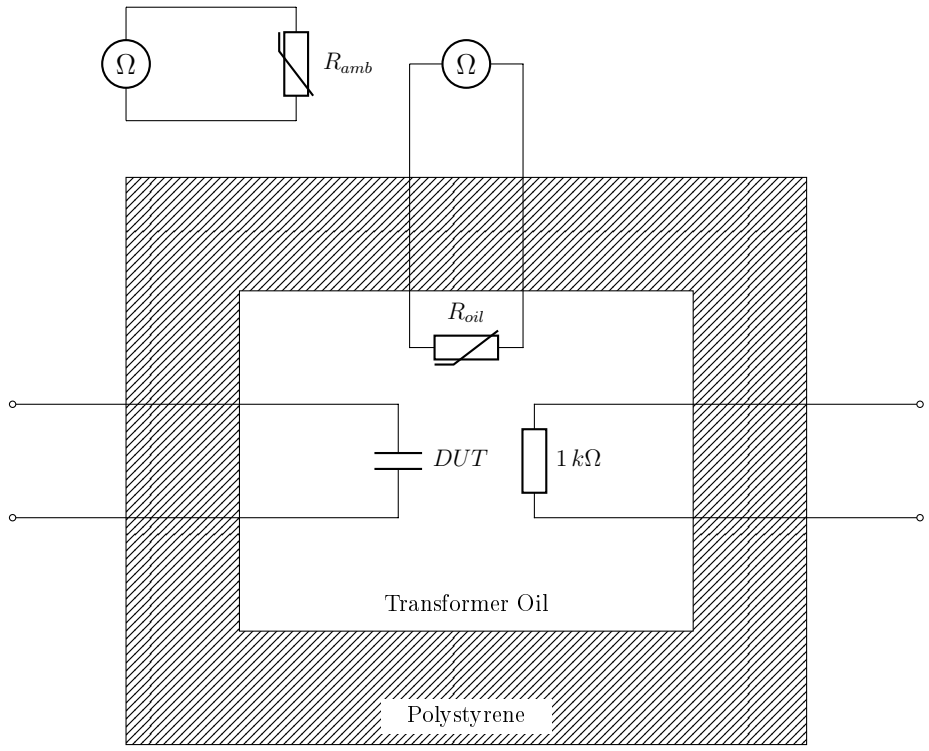

Figure 6.1: Schematic of the CMS

The oil is assumed to keep the temperature of the three elements on the same level. Thus the temperature difference between the DUT and the ambient air can be measured with the Pt100. Further the heat flow can be calculated with the equation

$$P_{loss} = \dot{Q} = \frac{\Delta T}{R_{th}} \tag{6.1}$$

where ΔT is the temperature difference between the inside and the ambient air. R_{th} is the thermal resistance of the polystyrene surrounding in parallel with the six copper leads which connect the three elements. $\dot{Q}$ is the heat flow through the polystyrene and the leads. The losses are completely converted into heat, so $\dot{Q}$ equals P_{loss}.

The reference resistor is inserted to obtain the thermal resistance R_{th}. To do so a voltage is applied to the resistor. The current through the resistor is measured and then calculated together with the voltage to the power

$$P = VI \tag{6.2}$$

The electrical energy applied to the resistor is again completely converted to heat thus the losses in the resistor equal the heat flow $\dot{Q}$. The thermal resistance can then be calculated using equation 6.1, resolved for R_{th} after some time when the internal temperature does not change any more.

Figure 6.2 shows the ESR with the PR of the same capacitor once in air (pink) and once immersed in oil (orange). Immersed in oil the PR of the capacitor decrease significantly. Possibly the oil damps the mechanical oscillations. Thus the losses caused by the PR would possibly decrease and would hence be more difficult to determine. To overcome this problem the CMS is adapted slightly as described in the next section.

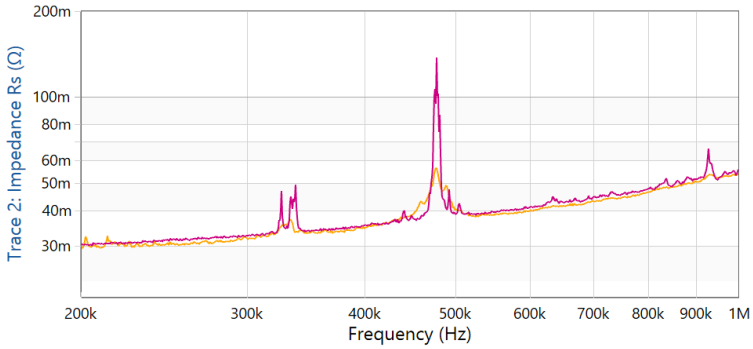

Figure 6.2: PR of a capacitor in air (pink) and in oil in the CMS (orange)

6.2 Adapted Calorimetric Loss Measurement

Figure 6.3 shows an adaption of the CMS. The DUT and the reference resistor are now surrounded by a cage made of a circuit board with copper area at the outside. The single parts are soldered together to make it leak-proof. Thus the DUT is not immersed in oil

but again in air. The cage is immersed into transformer oil which is again surrounded by polystyrene. The temperature of the oil and the ambient temperature is measured. It is assumed that in steady-state the temperatures of the DUT and the reference resistor are equal and the oil is equally tempered.

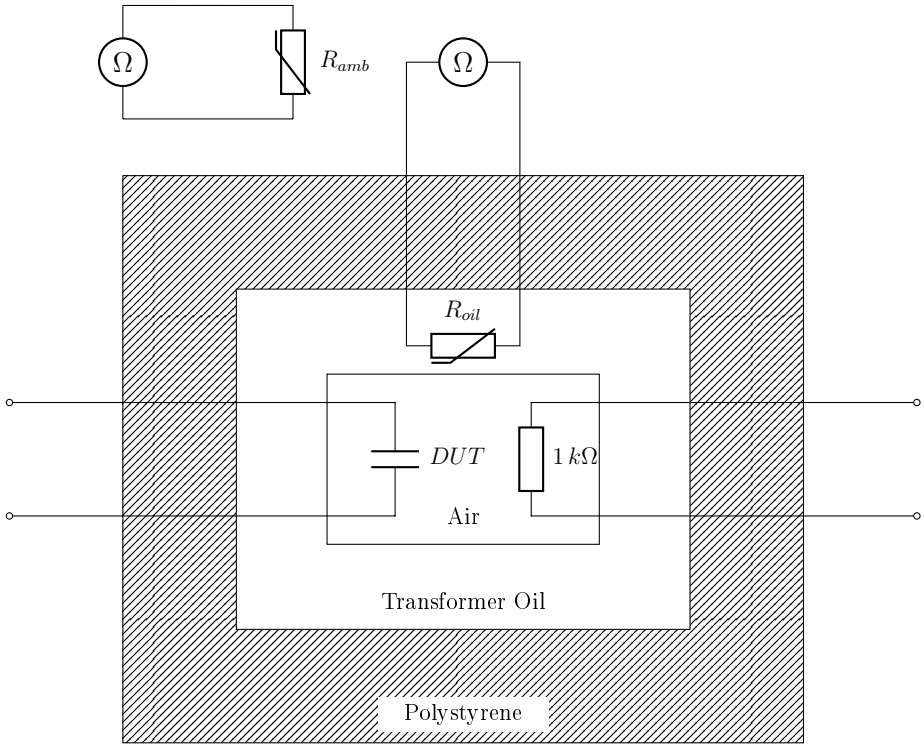

Figure 6.3: Schematic of the improved CMS

Figure 6.4 shows the equivalent thermal circuit of the CMS. If the temperature of the oil is evenly distributed then the total thermal resistance between the internal cage and the oil can be combined to R_{thCO}. Also the thermal resistance between the oil and the ambient air can be combined to R_{thOA}. In this case the thermal circuit is a simple circuit consisting of a heat source and two thermal resistors. Actually the internal Pt100 does not measure the total temperature difference, but the temperature difference between the oil and the ambient air. Also the measurement of the thermal resistance using the reference resistor does not give the total thermal resistance but the resistance R_{thOA}. Nonetheless the measurement provides the true power loss, since $\dot{Q}$ is flowing through both thermal resistances and

$$P_{loss} = \dot{Q} = \frac{T_{DUT} - T_{amb}}{R_{thCO} + R_{thOA}} = \frac{T_{oil} - T_{amb}}{R_{thOA}} \tag{6.3}$$

The temperature behaviour of the Pt100 elements can be approximated using the equation

$$R(T) = R_0 \cdot (1 + \alpha \cdot T) \tag{6.4}$$

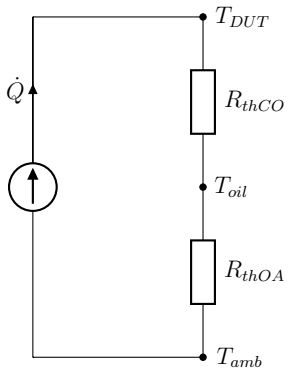

Figure 6.4: Equivalent thermal circuit of the CMS

where R_0 is the resistance at 0 °C and α is the linear temperature coefficient. T is the temperature in °C. For the Pt100 R_0 equals 100 Ω and α equals $3{,}85e{-}3\,{}^{1}/_{\circ C}$ according to the datasheet.

The temperature of each Pt100 can be calculated with

$$T = \frac{R(T) - R_0}{\alpha R_0} \tag{6.5}$$

and the power loss of the DUT with

$$P_{loss} = \frac{T_{oil} - T_{amb}}{R_{thOA}} \tag{6.6}$$

An applied voltage of 24 V at the 1 kΩ resistor with a measured current of 23,3 mA leads to a power of 560 mW. The temperature difference is measured to be 21,1 °C. This leads to the thermal resistance

$$R_{thOA} = \frac{\Delta T_{OA}}{VI} = 37{,}7\,\frac{^\circ C}{W} \tag{6.7}$$

The measurement is done overnight to obtain the steady-state without additional temperature changes. It is performed inside a closed chamber to reduce airflow.

6.3 Loss Measurement Setup and Preparation

The losses in the output capacitor are now measured in a synchronous buck converter. The used converter is integrated in the evaluation board DC2456A from Analog Devices. The board contains a synchronous non-inverting buck-boost converter which can operate in boost, buck-boost and buck operation mode, depending on the input voltage.

On the board all output capacitors are removed except two 0,1 µF capacitors located in parallel to the output capacitor. These seem to be essential for the converter's stability. The influence of the two capacitors is assumed to be negligible since their capacitances are much smaller than the capacitance of the output capacitor (54 µF). Also an pre-implemented average output current control loop is removed.

Figure 6.5 shows the measurement setup for the loss measurement. The buck-boost converter is operated with 120 V input voltage. Due to the high input voltage the controller operates the converter only in buck mode. The yielded buck converter is illustrated as the two switches Q_1, Q_2, the controller and the output filter. The latter consists of the 15 μH inductor and the DUT, which is integrated in the CMS.

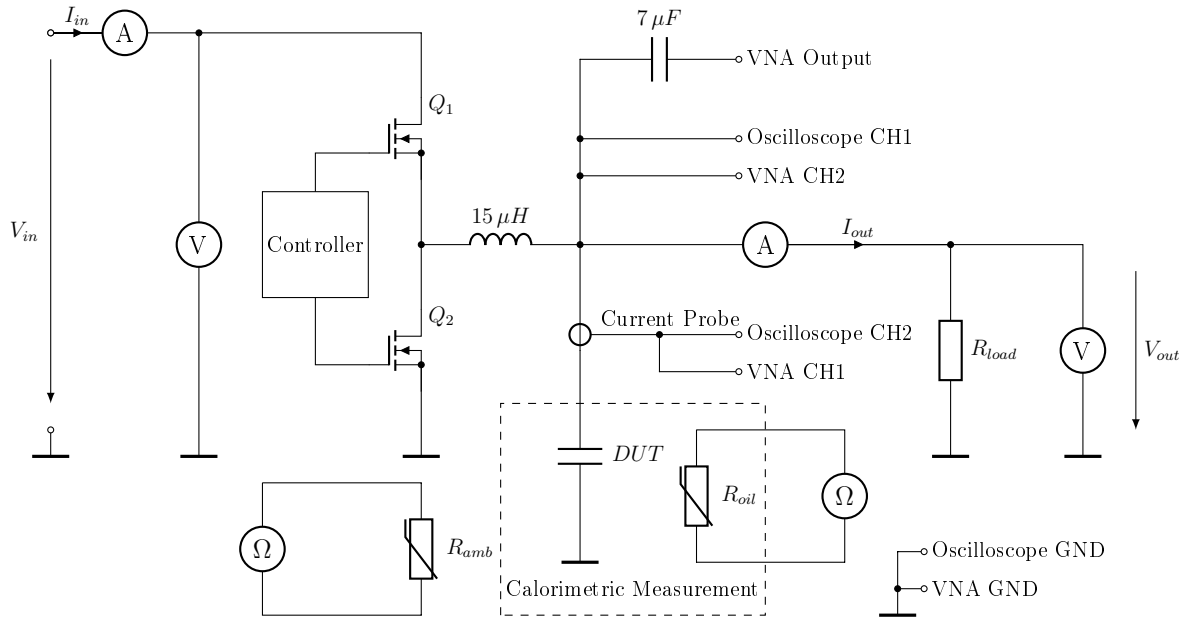

Figure 6.5: Capacitor loss measurement setup: measurement of the input and the output power with two ampere meters and two voltmeters, the ESR with the PR with the VNA, the voltage and current of the output capacitor with the oscilloscope and the capacitor losses with the two ohmmeters and the two temperature dependent resistors

The input and the output power is measured using a voltmeter and an ampere meter each time. The total efficiency of the converter can be calculated with

$$\eta = \frac{P_{out}}{P_{in}} \cdot 100\,\% = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}} \cdot 100\,\% \tag{6.8}$$

A current probe is used to measure the current through the DUT. The measured signal of the probe is forwarded to the oscilloscope and the VNA. Two voltage probes are used to measure the voltage once for the oscilloscope and once for the VNA.

The oscilloscope is used to plot the voltage and current curves in the time domain. With the integrated mathematics function the RMS current I and the average power is calculated.

$$I = \sqrt{\frac{1}{T} \int_{t_0}^{t_0+T} i(t)^2 dt} \tag{6.9}$$

$$P = \frac{1}{T} \int_{t_0}^{t_0+T} v(t) \cdot i(t) dt \tag{6.10}$$

where T is the period of the periodic signal.

The power calculation of the oscilloscope is assumed to be not accurate, since offset errors of the voltage and current probes can lead to significant errors. However this calculation is used to get a fast estimation of the power, since the response time of the CMS is very slow. With the oscilloscope also the frequency and the magnitude of the current's harmonics are calculated using the fast Fourier transform (FFT) and a peak finder function.

In section 5.2 on page 38 it is shown that the frequency of the PR can change with time, thus the VNA is used to monitor the location of the resonance peaks. The output of the VNA is capacitively decoupled and fed into the DUT. The impedance is then calculated by the VNA with the division of voltage and current. The measurement is not OSL calibrated; it is only used to locate the peaks and not to give an accurate result of the ESR.

The ohmmeters measure the resistance of each Pt100 temperature sensor. These measurements are used to calculate the temperature difference between the internal of the CMS and the ambient air for the loss measurement.

A load resistance of about 67 Ω (three times 200 Ω in parallel) is used as load.

The DUT consists of three 17 µF X7R capacitors with a rated voltage of 50 V which are placed in parallel. This results in an output capacitance of 54 µF. Experiments show that the converter on the evaluation board does not run in a stable operation when only one 17 µF capacitor is used as output capacitor.

In a parallel circuit the component with the least impedance contributes to the total impedance mainly. Hence to investigate the impact of the resonances, three capacitors with matching resonances must be inserted. Figure 6.6 shows the PR of three capacitors of the same type (X7R, 17 µF, 50 V). The three capacitors have a sufficient matching resonance peak between 450 kHz and 500 kHz.

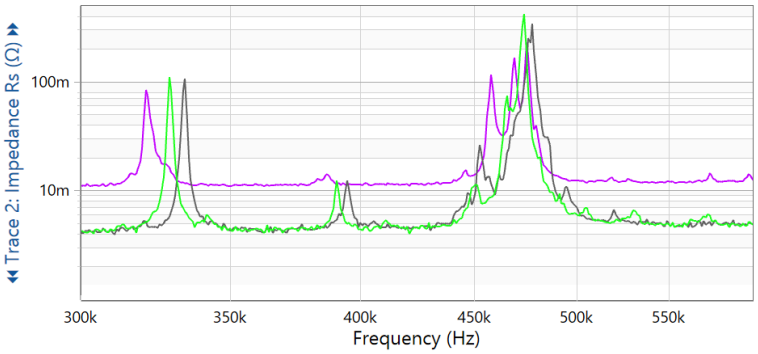

Figure 6.6: Resonances of three FDCCs of the same type with matching PR

A parallel circuit of the three mentioned capacitors exhibits the ESR curve shown in figure 6.7. The resonance peak at approximately 470 kHz is distinctive. This ca-

pacitor combination is used as output capacitors in the buck converter for further loss measurements described in the next section.

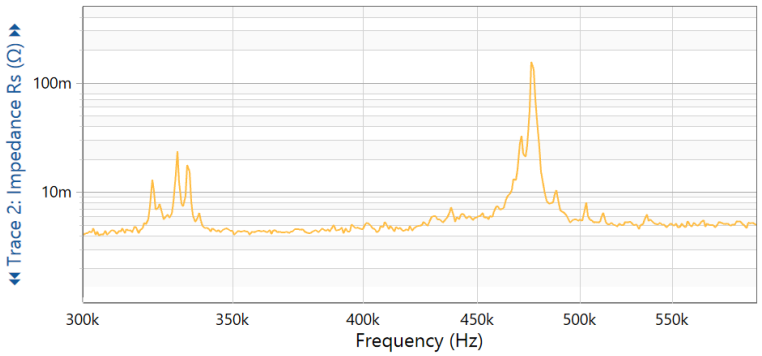

Figure 6.7: Resonances of the parallel circuit of three FDCCs with matching PR

6.4 Measurement and Results

The capacitor loss measurement is performed at three different frequency points. The switching frequency of the buck converter is adjusted to be one time below the PR, one time above the PR and one time exactly at the PR. A possible drop in the efficiency of the converter with increasing switching frequency caused by other parameters can thus be detected and removed by calculation.

Figure 6.8 shows the location of the resonances during the loss measurements. Initially the peak of the PR is at 483,2 kHz. The measurements above and below the PR frequency are performed at 460 kHz and 495 kHz. The measurement at the PR frequency is performed at the resonant peak at 492 kHz. The PR frequency increases during the measurement from 483,2 kHz (first measurement, green) to 483,8 kHz (second measurement, orange) to 492 kHz (third measurement, pink). Operating the capacitor at the PR increases the PR frequency significantly so the switching frequency has to be adjusted continually. The increase could be caused by a temperature rise of the component. However the behaviour of the PR is not the main topic of this thesis and hence not further investigated.

The spikes that are visible in the impedance spectrum are measurement errors caused by the respective switching frequencies. Also circa 20 kHz below and above the switching frequencies there are spikes visible which could be caused by some low frequency modulated control signal, but they are not further analysed.

The measurement results of the loss measurement are listed in table 6.1. The table shows the measured parameters at the three frequency points. The results of interest are the efficiency of the whole converter η and the losses in the capacitors P_{loss}. The efficiencies are calculated using equation 6.8, the temperatures with equation 6.5 and the losses in the capacitors with equation 6.6.

The losses in the capacitors are significantly higher when operating the converter in the PR frequency. The efficiency of the converter decreases with increasing frequency.

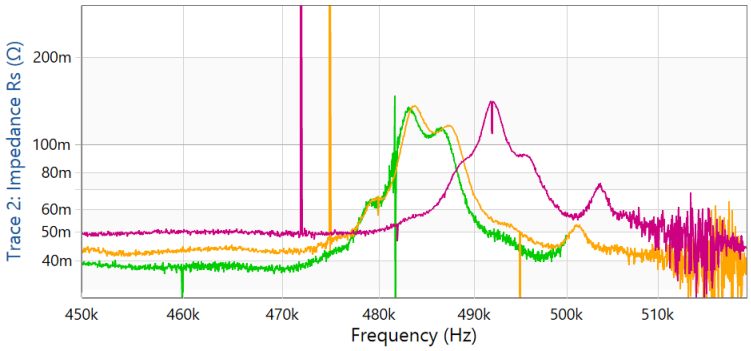

Figure 6.8: PR during the loss measurements: measurement at 460 kHz (green), 495 kHz (orange) and 492 kHz (pink)

Table 6.1: Results of the capacitor loss measurements

Parameter	Point 1	Point 2	Point 3
f_{switch} in kHz	460	492	495
V_{in} in V	120,02	120,01	120,02
I_{in} in mA	366,5	379,1	377,8
V_{out} in V	48,43	48,42	48,41
I_{out} in mA	721,5	724,2	723,8
P_{in} in W	43,99	45,50	45,35
P_{out} in W	34,94	35,06	35,04
η in %	79,43	77,07	77,27
R_{oil} in Ω	112,21	115,38	112,28
R_{amb} in Ω	110,04	110,07	110,05
T_{oil} in °C	31,71	39,95	31,90
T_{amb} in °C	26,08	26,16	26,10
ΔT in °C	5,64	13,79	5,79
P_{loss} in mW	149,5	365,9	153,7

Figure 6.9 shows the trend of the efficiency with frequency. The measured points and their interpolation are depicted in blue. In [EM04] the main contributors to the losses in PE are explained to be semiconductor switches and the inductors. The losses in semiconductor switches are explained to be linearly increasing with frequency. The losses in magnetic devices are more difficult to model and do not increase linearly with frequency.[1] However for the sake of simplicity the efficiency drop due to non PR related effects is assumed to be linear and plotted in red. The point shown in red is the expected efficiency without the influence of the PR based on a linear interpolation.

[1] [EM04] describes losses in inductors due to changing magnetisation in the core as linearly increasing with frequency, eddy current losses in the core increase with f^2 or stronger and losses due to skin- and proximity effect do increase with frequency, but the order is depending on the geometry.

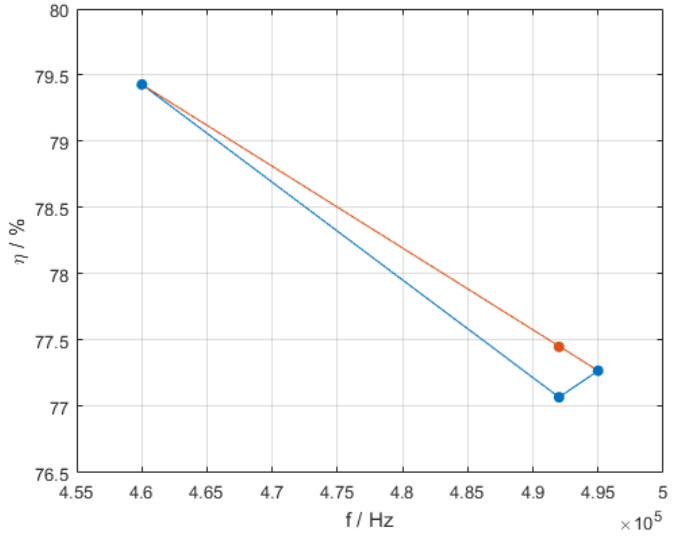

Figure 6.9: Efficiency of the converter at the three measurement points (blue) and interpolation with expected efficiency without PR (red)

The linearly interpolated efficiency can be obtained with

$$\eta_{2_{lin}} = \eta_1 - \frac{(\eta_1 - \eta_3) \cdot (f_2 - f_1)}{f_3 - f_1} = 77{,}45\,\% \tag{6.11}$$

The efficiency drop caused by the capacitor resonances is assumed to be the difference between the interpolated and the measured efficiency at point 2.

$$\eta_{res} = \eta_{2_{lin}} - \eta_2 = 0{,}38\,\% \tag{6.12}$$

This calculation shows that the efficiency of the converter drops by 0,38 % as a result of operating the converter in the frequency of the PR.

The influence of the PR on the efficiency can alternatively be calculated by directly taking the capacitor losses into account. Thus the converter's efficiency is calculated once with and once without the losses caused by the PR and then the results are subtracted. For the sake of simplicity the losses caused by the PR are assumed to be $P_{loss2} - P_{loss1}$, i.e. the capacitor loss difference between point 2 and point 1.

$$\eta_{res2} = \left| \eta_2 - \frac{P_{out}}{P_{in} - (P_{loss2} - P_{loss1})} \right| = 0{,}37\,\% \tag{6.13}$$

Using this calculation the efficiency decreases by 0,37 %. This result matches very accurate the calculations in the equations 6.11 and 6.12. Consequently the efficiency is stated to really drop because of the PR and for this narrow frequency range the linear approximation of the decrease of efficiency with frequency is valid.

Figure 6.10 shows a thermal image of the converter during the 495 kHz measurement. The main causers of heat and thus losses are indeed the switches and the inductor. The

output capacitor is not visible in the picture since it is embedded in the CMS. The load resistors which dissipate the most heat are also not shown.

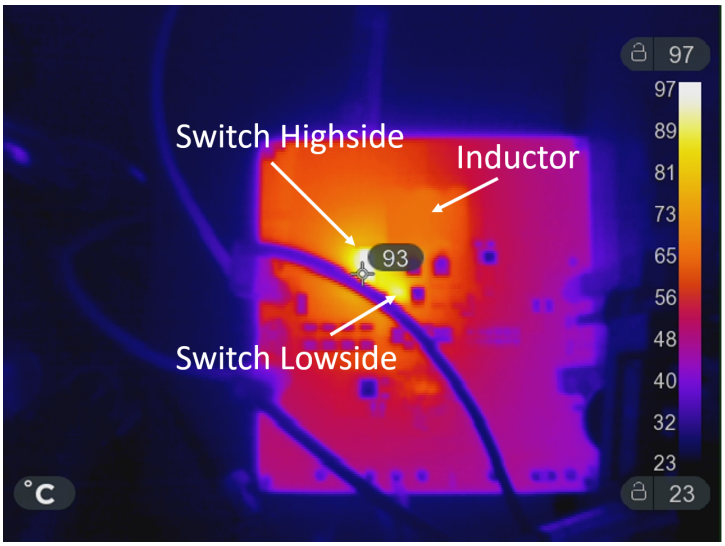

Figure 6.10: Thermal image of the buck converter on the evaluation board during the 495 kHz measurement

Figure 6.11 shows the ac voltage across the capacitor (blue) and the current through the capacitor (pink) at 460 kHz. Except different values for frequency and amplitude the curves look similar at the other two measured frequencies. Hence the signals in time domain are plotted only once.

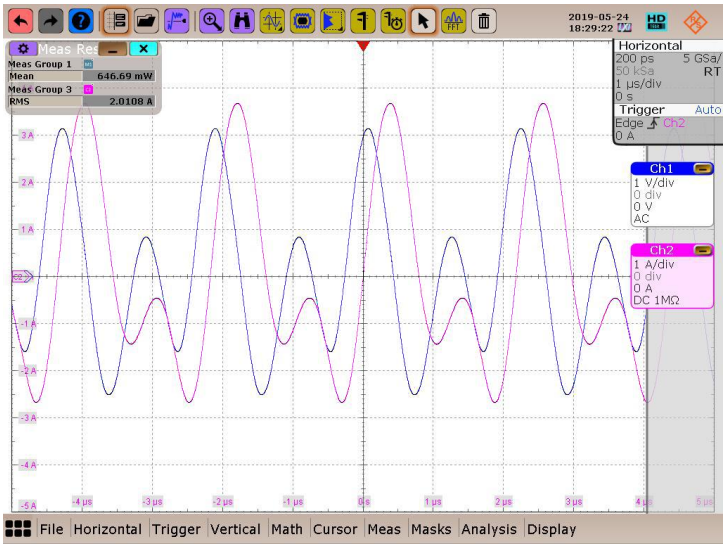

Figure 6.11: Ac voltage (blue) and current (pink) of the output capacitor at 460 kHz

The current of an ideal buck converter should be triangular, this is not the case in this measurement. Although the effect of the PR on the losses has been shown by

the thermal measurement the deviation of the current waveform is further investigated. Thus a transient simulation of the current is introduced in the next section.

6.5 Simulation of the Capacitor Current

The current through the output capacitor of a buck converter should ideally be triangular. The measured current shown in figure 6.11 on page 49 deviates from the triangular waveform strongly. The cause of the deviation is now investigated to exclude an error in the measurement setup.

The inductor current waveform of the ideal buck converter is shown in figure 6.12 without dc offset. The ac current through the capacitor is assumed to be the same than the ac current through the inductor[2]. The correlation between the voltage and the current in an inductor is given by

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{6.14}$$

and resolved for $i_L(t)$

$$i_L(t) = \int \frac{v_L(t)}{L} dt \tag{6.15}$$

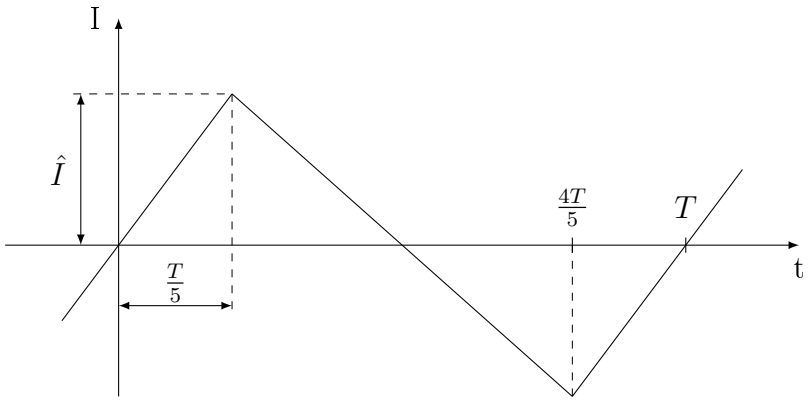

Figure 6.12: Inductor current of an ideal buck converter

The relation between input voltage and output voltage of a buck converter is given by the equation

$$V_{out} = DV_{in} \tag{6.16}$$

where D is the duty-cycle and is defined as

$$D = \frac{T_{on}}{T} \tag{6.17}$$

[2]The impedance of the capacitor equivalent circuit is measured to be 0,5 Ω at 460 kHz. It is significantly smaller than the load of 67 Ω, thus most of the ac current flows into the capacitor

and T is the period and T_{on} the time the switch connected to V_{in} is conducting and the switch connected to ground is blocking.

With $V_{in} = 120\,\mathrm{V}$ and $V_{out} = 48\,\mathrm{V}$ the duty-cycle is $D = {}^{V_{out}}/_{V_{in}} = {}^{2}/_{5}$ i.e. the current increases during ${}^{2}/_{5}$ of the period and falls during ${}^{3}/_{5}$ of the period.

The triangular current of the ideal buck converter as shown in figure 6.12 can be described with

$$f(t) = \begin{cases} \frac{5\hat{I}}{T}t, & 0 \le t < \frac{T}{5} \\ -\frac{10\hat{I}}{3T}t + \frac{5\hat{I}}{3}, & \frac{T}{5} \le t < \frac{4T}{5} \\ \frac{5\hat{I}}{T}t - 5\hat{I}, & \frac{4T}{5} \le t < T \end{cases} \qquad f(t) = f(t+T) \tag{6.18}$$

In steady-state the inductor current is in equilibrium over one period i.e. $i_L(t) = i_L(t+T)$. Thus the amplitude of the ac current can be calculated by the current increase over half of the on-time. For the time of $T_{on} = {}^{2T}/_{5}$ the inductor is attached to $120\,\mathrm{V} - 48\,\mathrm{V} = 72\,\mathrm{V}$; the current is rising during this time. During off time the voltage is $0\,\mathrm{V} - 48\,\mathrm{V} = -48\,\mathrm{V}$; the current is falling then. The peak current can be calculated with

$$\hat{I} = \int_0^{T/5} \frac{72\,V}{15\,\mu H} dt = 2{,}09\,A \tag{6.19}$$

These calculations are performed using steady-state analysis with the small-ripple approximation which is explained in [EM04], among others.

The RMS of the ideal current is

$$I = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} i(t)^2 dt} = 1{,}205\,A \tag{6.20}$$

The measured RMS current is 2,011 A. The measured current is significantly higher than the calculated one. Considering equation 6.15 the inductor current depends on the attached voltage and the reciprocal of the inductance. Thus the current can increase either with increasing voltage or decreasing inductance.

The inductance of the inductor is shown in figure 6.13 in red. The ESR of the inductor is shown in blue. Note that the scaling of trace 1 is linear and the scaling of trace 2 is logarithmic. The inductance does not change much below about 3 MHz and lies between $14\,\mu\mathrm{F}$ and $15\,\mu\mathrm{F}$. The ESR though increases very fast but is small at the switching frequency ($0{,}38\,\Omega$). Considering this impedance measurement the inductor seems not to be responsible for the waveform deviation. The saturation current of the inductor is 26 A according to the datasheet[3] thus a significant change of the inductance with current due to saturation is not expected.

Figure 6.14 shows the voltage across the inductor. The voltage should swing between $-48\,\mathrm{V}$ and $72\,\mathrm{V}$. The measured voltage does not match exactly the ideal waveform but the deviation is to small to explain the difference of the current waveforms. Considering the voltage at the inductor and the measured inductance leads to the conclusion that the

[3]The inductor is: $L = 15\,\mu\mathrm{H}$, $I_{rated} = 30\,\mathrm{A}$; manufacturer: Würth Elektronik; code: 7443641500

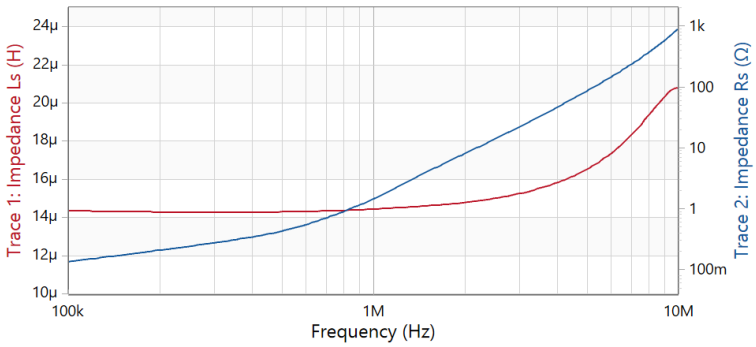

Figure 6.13: Measured inductance (red) and ESR (blue) of the inductor in the buck converter

assumption that the inductor current and the capacitor current are the same is wrong. Thus the circuit is simulated in LTspice to get more information about the deviation.

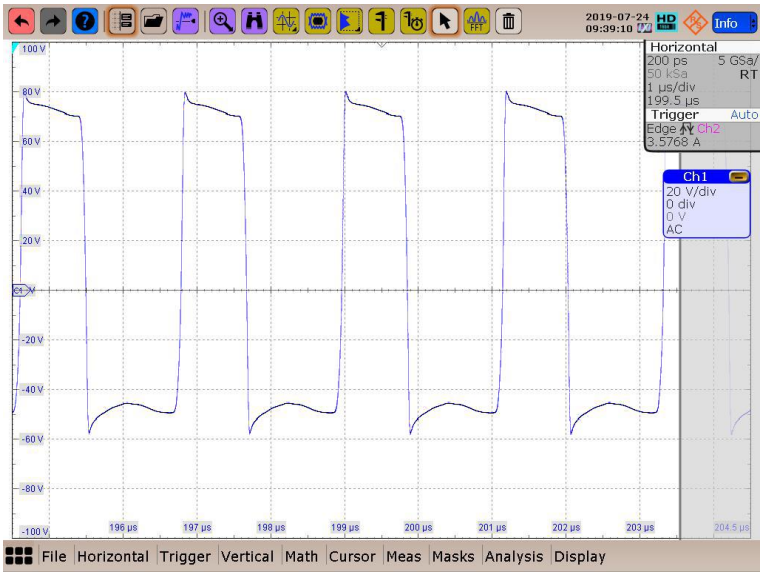

Figure 6.14: Measured inductor voltage at 460 kHz

Figure 6.15 shows the schematic of the spice simulation of the buck converter. The converter is simulated with two ideal voltage controlled switches Q_1 and Q_2 (depicted as Mosfets[4]), the ideal inductor with its nominal value of $15\,\mu$H and the equivalent circuit of the output capacitor. The values of the output capacitor's equivalent circuit are measured to be $C = 15\,\mu$F (at 48 V dc bias), $ESR = 50\,\text{m}\Omega$ and $ESL = 150\,$nH. Also the load resistor is included in the simulation. The switches are controlled via a rectangular voltage source. Q_2 is fed with the inverted rectangular voltage (realised with the additional inverter) i.e. Q_2 is off while Q_1 is on and vice versa. The in section 6.3

[4]Mosfet stands for metal oxide semiconductor field effect transistor and is a voltage controlled semiconductor switch

on page 43 mentioned capacitors in the evaluation board which have been neglected so far are also included in the simulation.

With 460 kHz the period of the rectangular voltage source is $^1/_{460\,kHz} = 2174$ ns and the on-time is $T_{on} = DT = 870$ ns, when $D = 0{,}4$. Q_1 is low-ohmic during T_{on} and high-ohmic the rest of the time. Q_2 behaves conversely.

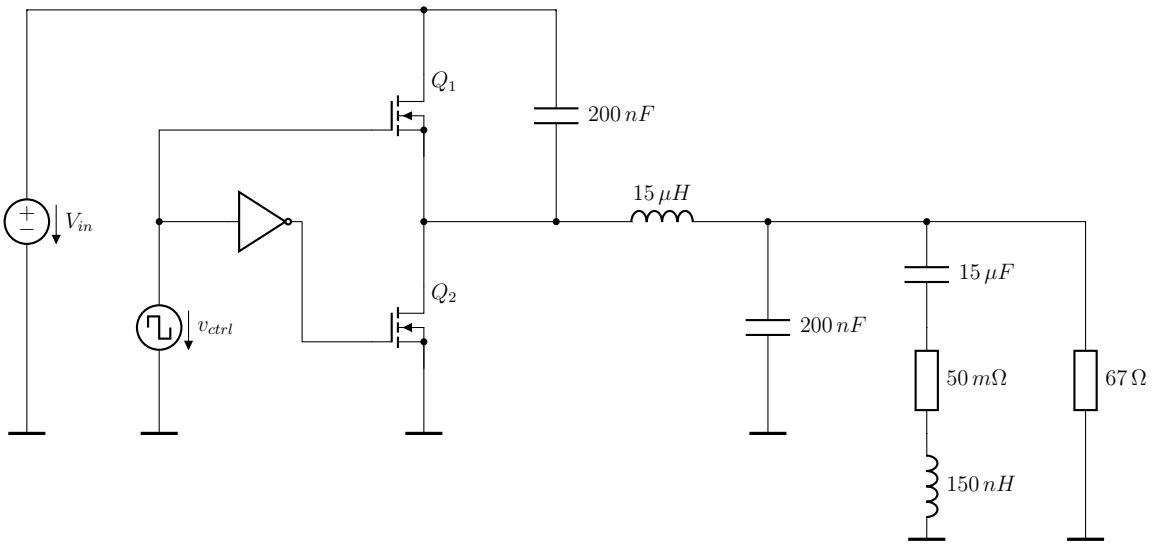

Figure 6.15: Schematic of the capacitor current simulation

Figure 6.16 shows the simulated current through the output capacitor (blue) in steady-state. The output capacitor current of an ideal buck converter is shown in red[5]. The simulated current shows similar oscillations than the measured current shown in figure 6.11 on page 49. The oscillations seem to be caused by the resonant circuit consisting of the 150 nH parasitic inductance of the DUT and the 200 nF capacitor which is placed directly after the inductor. The resonance frequency of a parallel resonant circuit consisting of a 200 nF capacitor and a 150 nH inductor is coincidentally $f_r = {}^1/_{2\pi\sqrt{200\,nF \cdot 150\,nH}} = 918{,}8$ kHz and thus nearly exactly the frequency of the second harmonic of the triangular 460 kHz inductor current. This oscillations explain not only the deviation of the current waveform but also the increased amplitude of the current.

The simulation shows that the odd current waveform is not caused by errors in the measurement setup but by the two 200 nF capacitors. If the losses in the output capacitor depend only on the current and the ESR then a different current waveform should not influence the analysis negatively if the PR affect the losses.

The losses of the capacitor are estimated using the harmonics of the current in the next section.

[5]The ideal buck converter is simulated without the two 200 nF capacitors, the ESR and the ESL

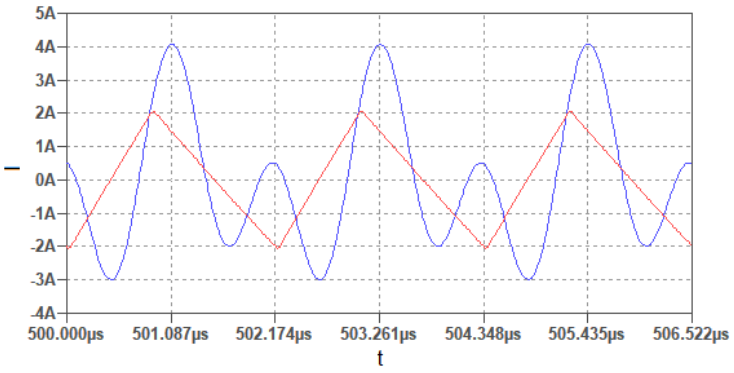

Figure 6.16: Simulated current of the output capacitor (blue) and output capacitor current of an ideal buck converter (red)

6.6 Loss Calculation with Fourier Analysis

The losses are now calculated using the harmonics of the current with the ESR at the respective frequency. The calculated losses are then compared to the measurements to evaluate the potential to estimate the power using the ESR at a dc operating point. Also the deviation of the harmonics of the measured and the ideal current is taken into account.

In figure 6.17 the curves of the voltage, the current and the instantaneous power are plotted on the top half and the spectrum of the current, which is of interest, is plotted in the bottom window. Also the frequencies and the amplitudes of the current harmonics are displayed in the result table. The peak at 186 Hz shows the insufficient ac decoupling which was mentioned in the previous section 6.3 to lead to miscalculations in the power measurement.

The unit dBm is the logarithmic power level referred to 1 mW. It can be calculated from an RMS value with the equation.

$$P_{db} = 10 \cdot \log\left(\frac{P}{1\,mW}\right) \tag{6.21}$$

with

$$P = \frac{V^2}{R} \tag{6.22}$$

and $R = 50\,\Omega$. The RMS voltage can be obtained by inserting equation 6.22 into equation 6.21 and resolving for V

$$V = \sqrt{50\,\Omega \cdot 1\,mW \cdot 10^{\frac{P_{dB}}{10}}} \tag{6.23}$$

Although as seen in figure 6.17 the oscilloscope displays the current in A, the displayed harmonics in dBm are still calculated to an RMS value with the equation 6.23 since the oscilloscope can only measure voltages.

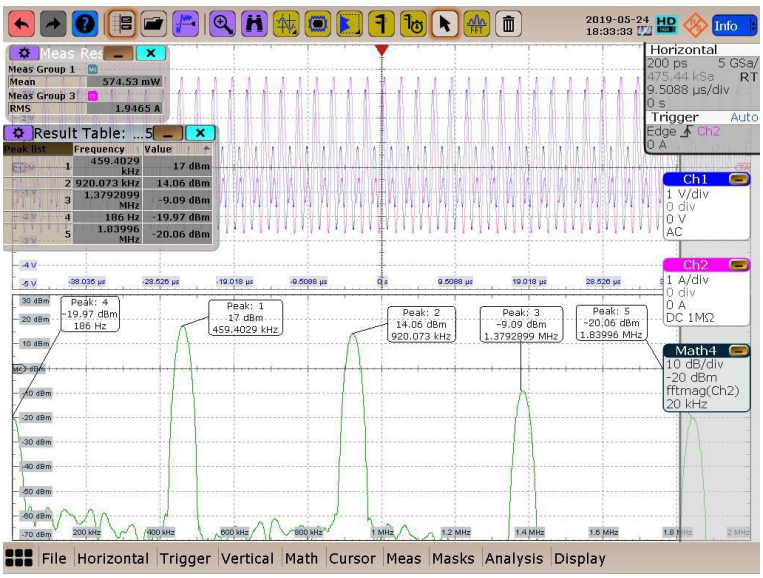

Figure 6.17: Oscilloscope measurement at 460 kHz. Top: voltage, current and instantaneous power of the output capacitor in time domain; bottom: spectrum of the capacitor current

The harmonics of the measurement and the simulation are compared with the harmonics of the current of the ideal buck converter. The harmonics can be obtained using the Fourier series. The Fourier series can be calculated with

$$f(t) = \frac{a_0}{2} + \sum_{k=1}^{\infty} \left(a_k cos\left(k\omega t\right) + b_k sin\left(k\omega t\right)\right) \tag{6.24}$$

where the coefficients a_k and b_k can be calculated with

$$a_k = \int_0^T f(t) cos\left(k\omega t\right) dt \quad k \geq 0 \tag{6.25}$$

$$b_k = \int_0^T f(t) sin\left(k\omega t\right) dt \quad k > 0 \tag{6.26}$$

and

$$\omega = \frac{2\pi}{T} \tag{6.27}$$

Applying the equations 6.25 and 6.26 on the triangular function defined in equation 6.18 on page 51 the parameters a_k and b_k can be obtained.

All a coefficients are zero because the function is an odd function

$$a_k = 0 \tag{6.28}$$

The coefficients of the spectrum can be obtained with

$$A_k = \sqrt{a_k^2 + b_k^2} \tag{6.29}$$

Since a_k is zero for each k, $A_k = |b_k|$.

The RMS of the harmonics can be obtained with

$$I_k = \frac{A_k}{\sqrt{2}} \tag{6.30}$$

For $\hat{I} = 4{,}5\,\mathrm{A}$ and $T = 1/460\,\mathrm{kHz}$ the calculated coefficients are listed in table 6.2. The table contains also the measured Fourier coefficients obtained by the FFT function of the oscilloscope. Also the coefficients of the simulated current are listed, which are obtained with the FFT function in LTspice.

Table 6.2: Fourier coefficients of the capacitor current; calculated, measured and simulated

k	I_{calc} in A	I_{meas} in A	I_{sim} in A
1	1,185	1,583	1,339
2	0,183	1,129	1,606
3	0,081	0,078	0,033

Figure 6.18 shows the spectrum of the ideal triangular signal (yellow), the with the oscilloscope measured (blue) and the simulated signal (red) at 460 kHz. The vertical axis is linear. The plotted currents are RMS currents. Both the measured and the simulated signals exhibit significantly higher first and second harmonics than the calculated one. The second harmonic of the simulated signal is even higher than the respective first harmonic.

In figure 6.19 the ESR of the capacitors in the CMS is shown at 48 V dc bias. This measurement is done with the measurement bridge while the capacitors are not connected to the buck converter.

The power loss is approximated using the first three harmonics and is calculated with

$$P_{loss} \cong I_1^2 \cdot ESR_1 + I_2^2 \cdot ESR_2 + I_3^2 \cdot ESR_3 \tag{6.31}$$

In table 6.3 the amplitudes and the respective ESR values are listed for the first three harmonics of the three currents at the three measured points. Also for each harmonic the with $P = I^2 \cdot ESR$ calculated loss is listed. The ESRs are taken from the ESR measurement shown in figure 6.19. Only the ESR at the resonant point in the 492 kHz measurement is taken from the live measurement. This measurement is assumed to be less accurate, but it is the only value available. At all three frequencies the third harmonic contributes to the losses with less than 1 %.

The losses of each harmonic listed in table 6.3 are summed up and listed in table 6.4 denoted as $P_{lossCalc}$. Also the measured losses ($P_{lossMeas}$) and the deviation to the calculations (ΔP_{loss}) are listed. The deviation of the measured and the calculated values is of

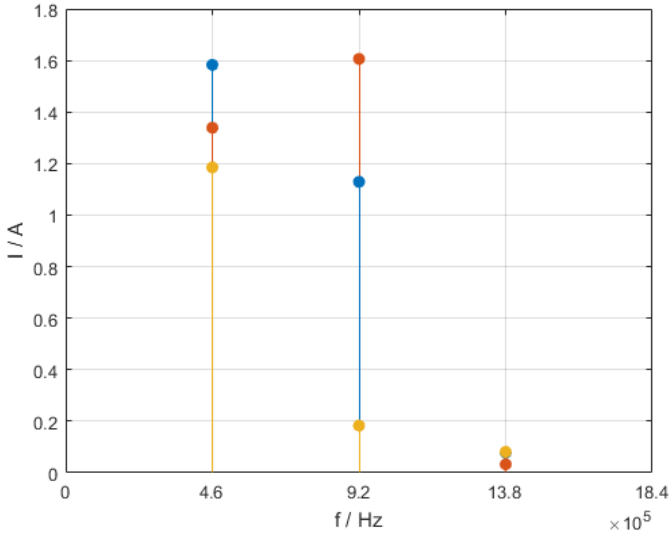

Figure 6.18: Fourier coefficients measured (blue), simulated (red) and calculated (yellow)

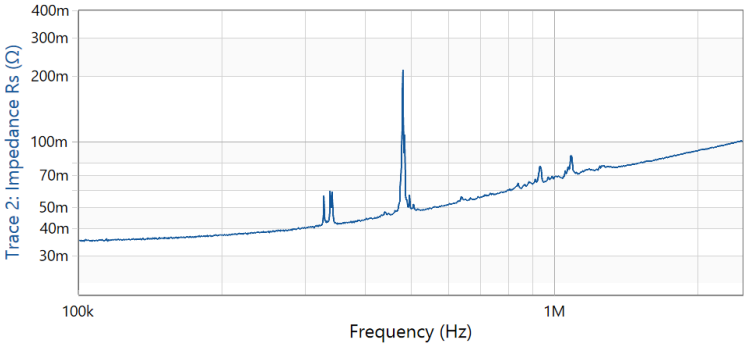

Figure 6.19: ESR of the capacitor inserted in the cage

the same order for all three measurements and the trend is the same for the calculation and the measurement.

Figure 6.20 shows the losses at the three frequency points. The measured losses are plotted in blue and the calculated losses in red. The calculation deviates to the measurement for all points in the same order. The figure shows clearly that the trend is the same, for the measurement and the calculations.

The influence of the PR is clearly visible despite the fact that the second harmonics do contribute much to the current and only the first harmonic lies at the PR. To estimate the effect without the additional oscillations described in section 6.5 the losses are calculated with the current waveform of the ideal buck converter. Therefore the obtained coefficients for the 460 kHz current are inserted into the 460 kHz loss calculation. The ideal coefficients for the 492 kHz and the 495 kHz are also calculated using the same procedure than for 460 kHz. The results of the calculations are listed in table 6.5. It can

Table 6.3: Results of the loss calculations for the three harmonics at the three frequency points

Parameter	1st harmonic	2nd harmonic	3rd harmonic
Point 1			
f in kHz	460	920	1380
I in dBm	17	14,06	−9,09
I in A	1,583	1,129	0,078
ESR in mΩ	46	65	76
P_{loss} in mW	115,3	82,9	0,5
Point 2			
f in kHz	492	984	1476
I in dBm	16,73	12,98	−11,88
I in A	1,535	0,997	0,057
ESR in mΩ	141	67	78
P_{loss} in mW	332,2	66,8	0,3
Point 3			
f in kHz	495	990	1485
I in dBm	16,58	12,77	−12,2
I in A	1,508	0,973	0,055
ESR in mΩ	52	68	78
P_{loss} in mW	118,3	64,4	0,4

Table 6.4: Measured and calculated losses of the output capacitor for the three measurement points

f in kHz	460	492	495
$P_{lossMeas}$ in mW	149,5	365,9	153,7
$P_{lossCalc}$ in mW	198,7	399,3	183,1
ΔP_{loss} in mW	49,2	33,4	29,4

be seen that compared to the measured values the ideal triangular current exhibits by far the most losses at the first harmonic.

The losses with the specific ESR but the ideal triangular waveform would be for the first three harmonics 67,3 mW at 460 kHz, 175,5 mW at 492 kHz (resonance) and 65,5 mW at 495 kHz. In this ideal simulation the overall capacitor losses are less but the effect of the resonances does even more contribute (a factor of about 2,7 from 460 kHz to 492 kHz instead of 2 for the calculation with the measured harmonics).

The difference between the measured losses and the calculated losses can be caused by an error in the measurement of the current harmonics, the ESR or the losses. Previous mentioned miscalculations of the power done by the oscilloscope due to offset errors cannot contribute to the deviation of the calculations to the measurements in this chapter. Only the harmonics of the current are considered and not the dc values. The ESR

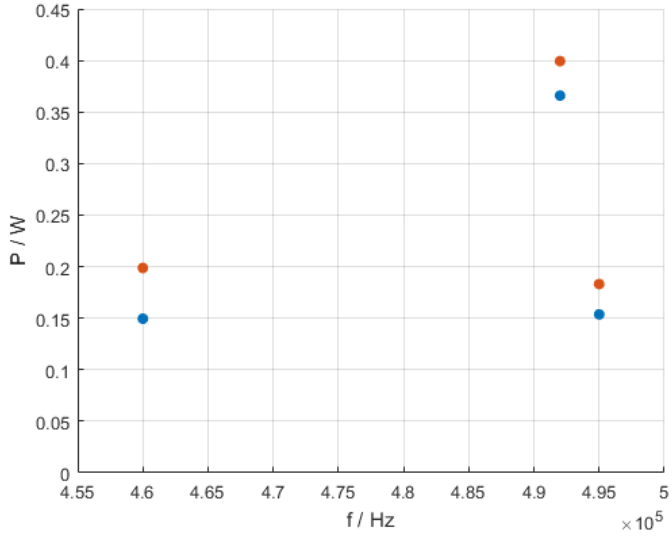

Figure 6.20: Measured and calculated losses of the output capacitor for the three measurement points. Blue: measured losses; red: calculated losses

Table 6.5: Results of the loss calculations for the three harmonics at the three frequency points using the ideal triangular current

Point	1st harmonic	2nd harmonic	3rd harmonic
Point 1			
f in kHz	460	920	1380
I_{calc} in A	1,185	0,183	0,081
ESR in mΩ	46	65	76
P_{loss} in mW	64,6	2,2	0,5
Point 2			
f in kHz	492	984	1476
I in A	1,108	0,171	0,076
ESR in mΩ	141	67	78
P_{loss} in mW	173,1	2,0	0,5
Point 3			
f in kHz	495	990	1485
I in A	1,101	0,170	0,076
ESR in mΩ	52	68	78
P_{loss} in mW	63,1	2,0	0,5

measurement with the VNA and the measurement bridge is also assumed to be correct. The error seems to be of a systematic nature since the amount is in the same order and the direction is the same for all measurements. Thus the error could be caused by the CMS.

The thermal resistance of the CMS is calculated with a reference resistor with a resistance of 1000 Ω. The lead resistances do not contribute much to the overall resistance and the losses are mainly generated inside the resistor. For the capacitor loss measurement the same type of leads are used for connecting the DUT. Due to the small ESR of the capacitor the leads do contribute very much to the overall resistance and thus the losses are partially generated in the leads.

The leads are copper leads with zinc alloy with a diameter of 0,4 mm and a length of approximately 0,1 m each. Assuming a composition with copper only the resistance can be calculated with

$$R = \rho \frac{l}{A} \tag{6.32}$$

using $\rho \cong 0{,}017\,{}^{\Omega mm^2}/_{m}$ leads to

$$R = 0{,}017\,\frac{\Omega mm^2}{m} \cdot \frac{4 \cdot 0{,}1\,m}{(0{,}4\,mm)^2\,\pi} = 27\,m\Omega \tag{6.33}$$

per lead, not including the skin-effect which does even more increase the resistance. Thus a significant amount of the losses is generated in the connection leads and the simple thermal equivalent circuit introduced in figure 6.4 on page 43 does not apply. The heat is not only generated inside the oil which leads to a lesser temperature difference between oil and ambient air. To overcome this problem a thicker lead could be used or a litz wire to reduce the skin effect. This on the other hand would decrease the overall thermal resistance due to the lesser thermal resistance of copper compared to polystyrene. However there is potential for improvement in the CMS.

7 Conclusion and Outlook

In the thesis a possible circuit to measure the ESR of capacitors with dc bias has been introduced. The functionality of the circuit has been verified. The ESR behaviour with dc bias of different capacitor types has been analysed. The influence of dc bias on PR of FDCCs has been investigated. A correlation of the losses and the ESR has been found in a PE application. An increase in the losses and thus a decrease of the efficiency in a PE system due to the influence of PR has been found. A calculation of the losses using the capacitor's current harmonics and the ESR at dc bias has been introduced and performed.

7.1 Findings

A circuit to measure the impedance and hence the ESR has been developed. With this circuit a dc biased measurement with up to 1000 V dc bias is possible. Its functionality has been tested by comparing the results to a TCM of the same capacitor. No significant deviation of the two measurements has been detected. The developed circuit exhibits better performance than the TCM, e.g. the possibility to measure one single capacitor and no influence of the dc source.

The drift of used film capacitors can lead to an error in the capacitance and ESR measurements. Simulations show an error in the capacitance measurement below 1 % for capacitances up to 100 μF over a frequency range between 1 Hz and 50 MHz. The ESR error is higher and has been evaluated for a specific FDCC with 330 nF. For this the FDCC the ESR has been measured and inserted into a simulation. The error is at max about 20 % at circa 25 Hz and drops with higher frequencies. This amount of error is assumed to be acceptable for dc biased measurements.

ESR measurements for different capacitor technologies have shown that the ESR of film capacitors and e-caps remains stable up to the rated voltage. The ESR of an X7R capacitor increases nearly linearly with voltage while the ESR of a CeraLink capacitor increases stronger in the beginning and falls again above a peak of about 70 % of the rated voltage. The ESR of a C0G capacitor falls with dc bias down to about 80 %. The trends of the ESRs for different capacitors type is a valuable information since the losses in capacitors depend linearly on the ESR.

FDCCs exhibit PR with applied dc bias. Their intensity seems to increase with dc bias. The frequency of the PR can change. The reason is not clarified but at a first glance it seems to correlate with the change of capacitance. If the PR frequencies depend on the capacitance or both parameters depend on an other yet unknown parameter is not clarified. The amplitude of the PR decreases when the capacitor is immersed into

oil. The reason could be that the oil damps the mechanical oscillations of the capacitor. Also it is observed that the frequency of the PR does increase when the capacitor losses increase. An explanation could be the increased temperature of the capacitor.

The losses of an output capacitor of a buck converter are measured with a CMS. The losses are obtained by measuring the temperature rise of the capacitor. The CMS is naturally only able to measure real power loss and not any imaginary power and a temperature rise of the internal of the CMS can only be caused by losses of the capacitor (if the reference resistor is not connected). Thus a higher temperature at the PR leads to the conclusion that the losses indeed increase when operating the converter at the PR.

The losses in the output capacitor increase when operating the converter at the PR of the capacitor. The efficiency decreases by about 0,38 % because of the PR. The losses in the capacitor increase from about 149,5 mW below the PR to 365,9 mW at the PR. Above the PR it decreases again to 153,7 mW. Although it is assumed that the loss measurement is not exact the trend of rising losses at PR is visible.

The capacitor current waveform of the measured buck converter does not match the triangular waveform which is expected in an ideal buck converter. The deviation has been analysed to be caused by a 200 nF capacitor which is placed in parallel to the measured output capacitor. This additional capacitor causes oscillations which increase the second harmonic of the capacitor current.

The loss measurement of the CMS does not match the loss calculations using the current harmonics exactly. For all three measured points the calculations provide higher losses than the measurements. The deviation is of the same order for all points. It is assumed that the deviation is caused by a measurement error of the calorimetric measurement. The assumption is that a significant amount of loss occurs in the connection leads and thus not in the capacitor itself. Hence not all losses are produced inside the CMS and the thermal circuit which is the basis for the loss calculation is not right.

7.2 Conclusion

The dc biased ESR measurement circuit is suitable to measure the ESR with an acceptable error. The trend of the ESR is not the same for all capacitor technologies; some technologies exhibit a significant increase or decrease of the ESR with dc bias. Using the current and the ESR to calculate the losses it is hence important to measure the ESR at the specific bias voltage. Considering that the losses increase linearly with the ESR and the ESR of e.g. CeraLink capacitors can increase by a factor of three the dc biased measurement is meaningful when choosing a capacitor in a PE system.

The PR can be measured with the measurement circuit but due to changes in amplitude and frequency an estimation in advance is not possible and the location of the PR has to be measured in a real operating circuit where the capacitors are supposed to be operated. During the loss measurements the frequency of the converter had to be increased continually to match the PR. This is in fact not close to reality for a PE system. Also in PE systems often various output capacitors with different technologies

are placed in parallel. Hence it is unlikely that PR of single FDCCs lead to a significant loss increase. All in all the PR maybe not responsible for a loss increase for most PE systems. On the other hand the measurements showed that there is a possibility that the losses increase and especially considering products with a high number of units the small losses can sum up to a very high amount of losses. However the influences of the PR on losses need definitely more research.

The output capacitor current of the buck converter in the loss measurement has exhibited oscillations which can be avoided in a real application. Nonetheless the effect of the PR could be shown. A calculation showed that the losses in the capacitors should be less without the oscillations but also the relative increase of the losses caused by the PR should be higher.

7.3 Outlook

The functionality of the developed measurement bridge has been verified for a specific case. It is not clarified yet if the circuit does provide the functionality for the whole demanded frequency and impedance range which is required by the company Omicron. In further developments this has to be checked.

The trend of the ESR has been analysed for five capacitors of different technologies. It is of course not said that the measured trends are representative for each respective technology. Investigating the respective trends and thus measuring an increased amount of capacitors with the developed circuit could be a further topic.

The behaviour of the PR could be further analysed. The PR frequencies could depend on the temperature of the component, the applied dc or ac voltage, the dimension of the respective capacitor or the dielectric, among others.

The loss measurements could be repeated with an other PE system. Alternatively the used buck converter could be adapted that the oscillations in the output do not occur. Hence the measurements could be done in a more realistic application.

The error of the CMS could be reduced by decreasing the resistance of the connection leads. Thus the deviation of the calculations to the measurements could possibly be reduced. A decreased resistance of the connection leads would possibly lead to a decreased thermal resistance of the CMS since the cross section of the leads would be increased. If no suitable trade-off between these parameters can be found a better suited loss measurement should be developed for further measurements.

8 Summary

Ferroelectric dielectric ceramic capacitors (FDCC) are widely used in power electronics today. FDCCs can exhibit several advantages like high capacity density, low equivalent series resistance (ESR) and especially compared to electrolytic capacitors an increased lifetime. Negative attributes of FDCCs are temperature and voltage dependence of the capacitance, dielectric losses and sound emissions due to the inverse piezoelectric effect, among others. Current investigations show also peaks in the ESR, in component specific frequencies when dc bias is applied. Their cause is assumed to be resonances due to mechanical oscillations caused by the inverse piezoelectric effect [TB16] [Nov+11].

The decrease of capacitance with dc voltage bias is generally known and has been focus in many investigations in the past [Nov+11] [BLD00]. However the behaviour of the ESR with dc bias is not fully analysed and a general trend is to the knowledge of the author not documented yet.

In this thesis the research question is discussed how the ESR of FDCCs can be measured with dc bias and how the dc bias influences the losses of FDCCs in power electronic applications. Thus a suitable measurement circuit is developed to measure the ESR over frequency with applied dc bias. With this circuit the effect of dc bias on the ESR and further on the losses is investigated. The losses in a measured FDCC are determined in a power electronic system when the system's switching frequency is adjusted to match exactly a piezoelectric resonance (PR). Thus the amount of losses caused directly by the PR is investigated.

Measurement Circuit

The ESR of capacitors over a specific frequency range can be measured with a vector network analyser (VNA), among others. To overcome the harm of the VNA's output by high dc voltage there are several possibilities. [Tec16] proposes a series circuit of a dc and an ac voltage source and [Ham+14] proposes an inductive decoupling using a transformer. An other possibility is a two capacitor measurement (TCM) where a series circuit of two equal capacitors is measured. The dc voltage is applied between the capacitors via a high-ohmic resistor. If both capacitors are exactly equal the measurement provides the twice the ESR and half of the capacitance of each capacitor.

Taking the proposed circuits into account a measurement bridge is developed as shown in figure 8.1. The device under test (DUT) is charged to V_{dc} over the high-ohmic resistor R_5. The VNA's output (depicted as ac voltage source and $50\,\Omega$ resistor) and the measurement channel 1 (CH1) are capacitively decoupled with linear film capacitors. At the voltage divider consisting of R_1 and R_2 the voltage across the DUT is measured.

The current flowing through the DUT is obtained by measuring the voltage drop at the shunt R_3 with CH2. Influences on the voltage and the current measurements caused by circuit or parasitic elements are mathematically removed with the open-short-load (OSL) calibration by the VNA.

The OSL calibration can only be performed without dc bias. A drift of capacitance of the capacitor C_2 can lead to a significant phase and magnitude error of the impedance measurement and thus an ESR error. For measuring FDCCs the error is simulated to be sufficiently small due to their their typical ESR behaviour. A simulation shows that the capacitance error is below 1 % for all frequencies. The ESR error is simulated to be at max 20 % for a specific FDCC. This is an acceptable amount.

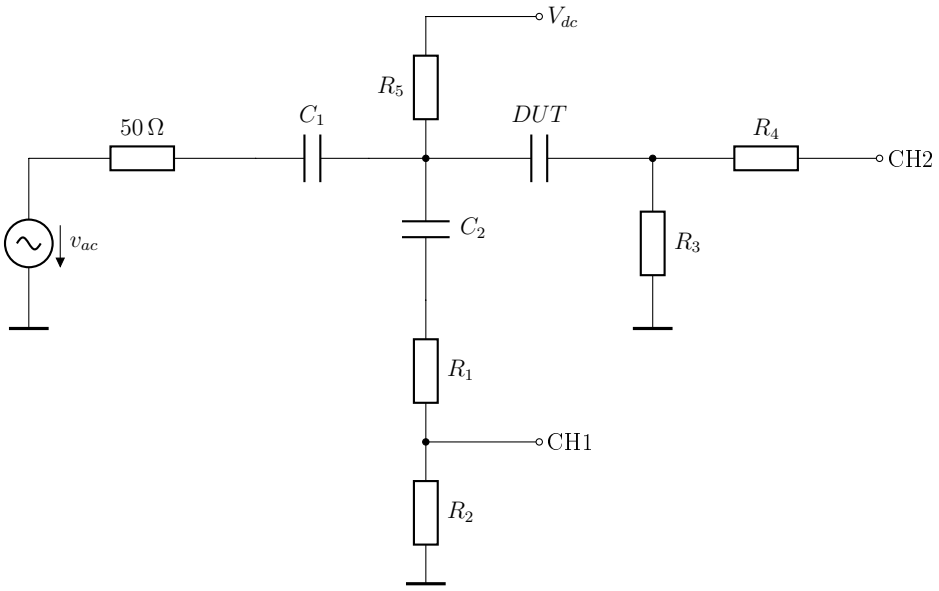

Figure 8.1: Circuit of the impedance measurement bridge

The measurement bridge is built up and verified with a measurement of a 68 nF C0G capacitor during 24 hours. The dc voltage is varied during the measurement between 0 V and 1000 V. The same measurement is performed using the TCM as reference. Both measurements exhibit the same behaviour without significant drifts.

Dc Biased ESR Measurement

The behaviour of the ESR is analysed for capacitors of different technologies. Figure 8.2 shows the ESR referred to the respective ESR without dc bias versus the applied dc bias referred to the rated voltage of each capacitor. The measured capacitors are a CeraLink capacitor (blue), an electrolytic capacitor (red), an X7R capacitor (yellow), a film capacitor (violet) and a C0G capacitor (green). The ESR of the two FDCCs (CeraLink and X7R) rise with dc bias. The ESR of the C0G capacitor falls with dc bias. The ESR of the other two capacitors remain stable with dc bias.

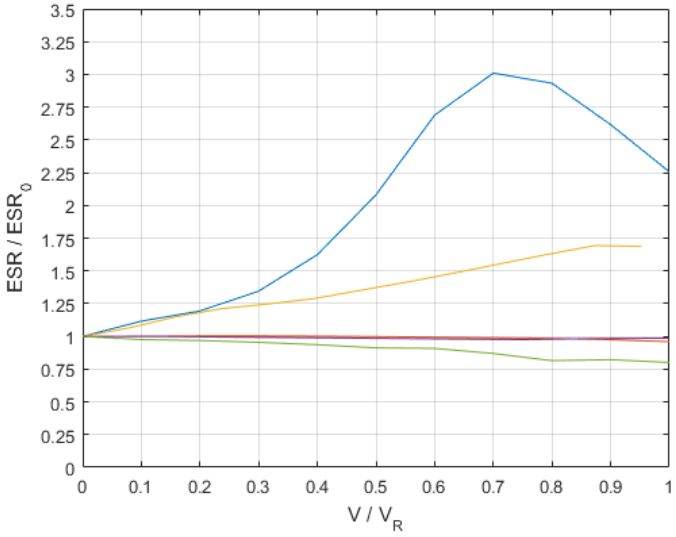

Figure 8.2: Relative ESR change of capacitors with dc bias. Blue: CeraLink; red: electrolytic capacitor; yellow: X7R; violet: film; green: C0G

Figure 8.3 shows the ESR of the X7R capacitor versus frequency. The ESR is shown at a dc bias of 0 V (blue), 150 V (red), 300 V (yellow), 450 V (violet) and 600 V (green). Above circa 300 kHz the PR are visible. The PR do not occur without dc bias and increase with increasing dc bias.

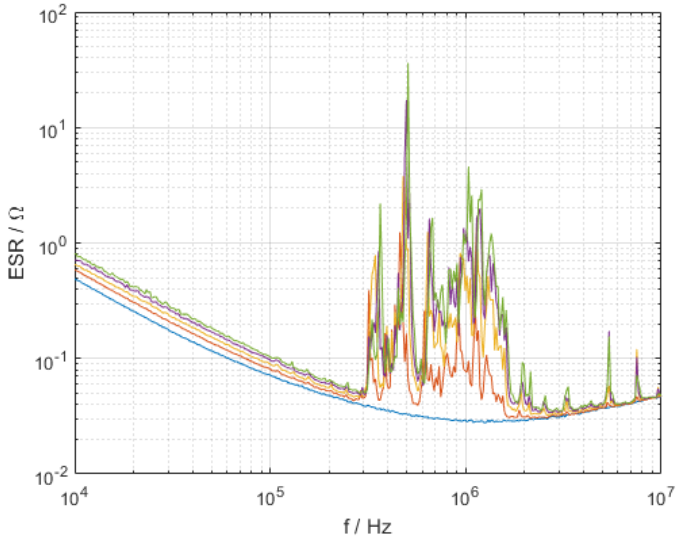

Figure 8.3: ESR versus frequency with dc bias. Blue: 0 V dc bias; red: 150 V; yellow: 300 V; violet: 450 V; green 600 V

Investigations show that the frequency of the PR changes with time when dc voltage is applied. The reason for the change is not determined.

Loss Measurement in Power Electronics Application

The losses in the output capacitor of a power electronic system are measured. Therefore a buck converter's output capacitor (the DUT) is inserted in a self developed calorimetric measurement system (CMS). In the CMS the DUT is surrounded by a polystyrene container. The temperature difference between the DUT and the ambient air is measured and together with the thermal resistance of the system resolved for the losses.

In the buck converter the input and the output power are measured and the efficiency is hence obtained. The losses in the DUT (output capacitor) are measured with the CMS. An oscilloscope is used to measure the voltage and the current at the DUT in time domain and also to calculate the harmonics of the current. A VNA is used to continually track the location of the PR to analyse if the PR frequency is changing. So the switching frequency of the buck converter can be adjusted to either lie below, above or exactly at the PR.

The capacitor losses are measured at a PR of 492 kHz. Two additional measurements are performed at 460 kHz and 495 kHz. The losses in the capacitor are measured to be 149,5 mW at 460 kHz, 365,9 mW at 492 kHz (PR) and 153, 7 mW at 495 kHz. Thus the losses at the PR are significantly higher. The efficiency drop caused by the PR is obtained to be circa 0,38 %.

Based on the capacitor current harmonics the capacitor losses are calculated. The harmonics are used because the output capacitor current in a buck converter is not sinusoidal. Hence it is investigated how accurate the losses can be estimated using the harmonics and the ESR at the respective frequency. The power is calculated for the first three harmonics and then summed up.

Figure 8.4 shows the measured losses (blue) and the calculated losses (red) for the three measured frequencies. The increased losses at the measurement at the PR are clearly visible. It can also be seen that the calculations do not match the measurements exactly but the deviation between the measurements and the calculations are of the same order for all three frequencies. The deviation is assumed to be caused mainly by inaccuracies of the measurement with the CMS.

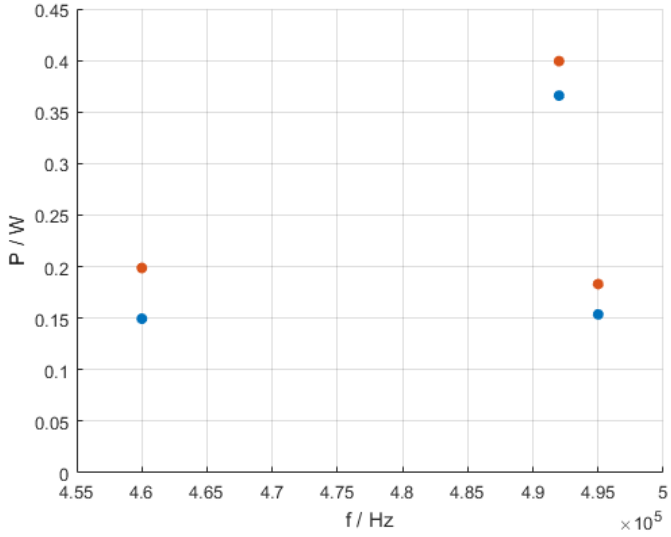

Figure 8.4: Measured and calculated losses of the output capacitor for the three measurement points. Blue: measured losses; red: calculated losses

Conclusion

The dc biased ESR measurement circuit is suitable to measure the ESR with an acceptable error. The trend of the ESR is not the same for all capacitor technologies; some technologies exhibit a significant increase or decrease of the ESR with dc bias. Using the current and the ESR to calculate the losses it is hence important to measure the ESR at the specific bias voltage.

The frequency of the converter had to be increased continually during the loss measurement to match the PR. In power electronic systems often various output capacitors with different technologies are placed in parallel. Hence it is unlikely that PR of single FDCCs lead to a significant loss increase. However there is a possibility for increased losses due to PR. A potential influence of the PR should be considered in power electronic circuits and the behaviour of the PR needs more research in general.

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Appendix

Appendix A - Open Short Load Calibration

The connection network to the DUT is modelled with a chain matrix. The chain matrix coefficients can be obtained with three measurements, the measurement of an open circuit, a short circuit and the measurement of a known device, e.g. a 50 Ω resistor. The calculations in this section have been taken out of [Tec16].

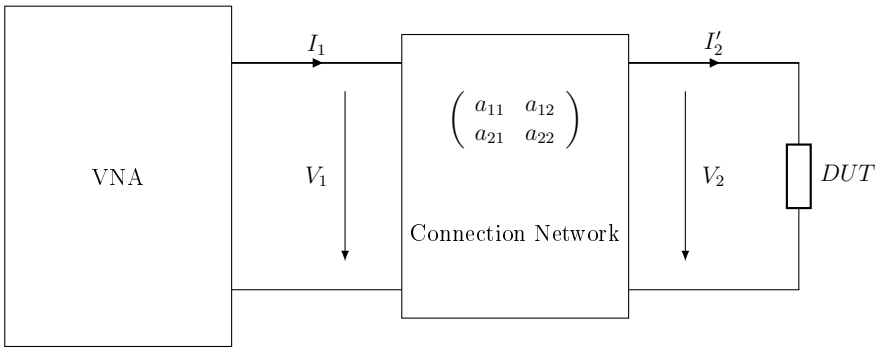

Figure 8.5: Impedance measurement circuit with an arbitrary connection network

A custom linear connection network to connect the input and output of the VNA to the DUT is replaced by the respective chain matrix. The correlation between the input and the output of the connection network is

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_2 \\ I_2' \end{pmatrix} \tag{8.1}$$

where a_{11}, a_{12}, a_{21} and a_{22} are the coefficients of the chain matrix. Hence the matrix can be expanded into the equations

$$V_1 = a_{11}V_2 + a_{12}I_2' \tag{8.2}$$

$$I_1 = a_{21}V_2 + a_{22}I_2' \tag{8.3}$$

For these four coefficients can be resolved using the measured impedances of the OSL-calibration. The further equations use following nomenclature:
Z_{dut} ... Corrected impedance of the DUT
Z_{xm} ... Measured impedance of the DUT
Z_o ... Measured impedance when the measurement terminals are open

Z_s ... Measured impedance when the measurement terminals are shorted
Z_{sm} ... Measured impedance of the load device
Z_{std} ... True value of the load device
Combining the equations 8.2 and 8.3 via ohm's law leads to

$$Z_{xm} = \frac{V_1}{I_1} = \frac{a_{11}V_2 + a_{12}I_2'}{a_{21}V_2 + a_{22}I_2'} \tag{8.4}$$

and with

$$Z_{dut} = \frac{V_2}{I_2'} \tag{8.5}$$

to

$$Z_{xm} = \frac{a_{11}Z_{dut} + a_{12}}{a_{21}Z_{dut} + a_{22}} \tag{8.6}$$

For the open calibration, where $I_2 = 0$ equation 8.4 reduces to

$$Z_o = \frac{a_{11}V_2}{a_{21}V_2} = \frac{a_{11}}{a_{21}} \tag{8.7}$$

$$a_{21} = \frac{a_{11}}{Z_o} \tag{8.8}$$

and similar for the short calibration where $V_2 = 0$ equation 8.4 gives

$$Z_s = \frac{a_{12}I_2'}{a_{22}I_2'} = \frac{a_{12}}{a_{22}} \tag{8.9}$$

$$a_{12} = a_{22}Z_s \tag{8.10}$$

The equation 8.6 combined with the equations 8.8 and 8.10 can be resolved to

$$Z_{dut} = \frac{D\,(Z_s - Z_{sm})}{A\,(Z_{xm} - Z_o)}Z_o \tag{8.11}$$

In the load calibration the equation

$$Z_{std} = \frac{V_2^*}{I_2^*} \tag{8.12}$$

applies when the voltage across the load device is V_2^* and the current through the device is I_2^*. This gives with the equations 8.2 and 8.3

$$Z_{sm} = \frac{a_{11}Z_{std} + a_{12}}{a_{21}Z_{std} + a_{22}} \tag{8.13}$$

Inserting the equations 8.8 and 8.10 into equation 8.13 can be resolved to

$$Z_{sm} = Z_o\frac{a_{11}Z_{std} + a_{22}Z_s}{a_{11}Z_{std} + a_{22}Z_o} \tag{8.14}$$

and further resolved to a_{22}

$$a_{22} = \frac{Z_{std}Z_{sm} - Z_{std}Z_o}{Z_oZ_s - Z_{sm}Z_o}a_{11} \tag{8.15}$$

respectively. Replacing a_{22} in equation 8.11 with equation 8.15 leads to the final calibration formula

$$Z_{dut} = \frac{(Z_s - Z_{xm})(Z_{sm} - Z_o)}{(Z_{xm} - Z_o)(Z_s - Z_{sm})}Z_{std} \tag{8.16}$$

Appendix B - List of Measured Capacitors

In table 8.1 all capacitors measured in the thesis are listed by occurrence. The capacitor type, the specific manufacturer and manufacturer's order code is also listed.

Table 8.1: List of the capacitors used for the measurements sorted by occurrence

Occurrence	Type	Manufacturer	Code
3.1, 4.1, 4.3	Film 7 μF	TDK	B32774D0705K000
4.3.1, 5.1	X7R 330 nF	Kemet	C2220W334KBRACTU
4.4, 5.1	C0G 68 nF	Kemet	C4540C683JDGACAUTO
5.1	CeraLink 1 μF	TDK	B58031I5105M062
5.1	E-cap 1 μF	Multicomp	MCTEA010M2WB-0816P
5.1	Film 330 nF	Vishay	BFC237390142
5.2	X7S 22 μF	TDK	C7563X7S1H226M230LE
6.1, 6.3, 6.6	X7R 17 μF	Murata	KCM55QR71H176KH01K

Statement of Affirmation

I hereby declare that all parts of this thesis were exclusively prepared by me, without using resources other than those stated above. The thoughts taken directly or indirectly from external sources are appropriately annotated. This thesis or parts of it were not previously submitted to any other academic institution and have not yet been published.

Dornbirn, 13.08.2019