Agenda

10th Power Analysis & Design Symposium

	Central European Time (CET/UTC +2)	Eastern Standard Time (EST/UTC-5)	Hong Kong Time (HKT/UTC+8)
Welcome and introduction	*09:00 - 09:10 am*	*03:00 - 03:10 am*	*04:00 - 04:10 pm*
Net Capacitance by Axel Schmidt (KEMET Electronics) & Günther Klenner (K&K Prime Engineering)	09:10 - 09:50 am	03:10 - 03:50 am	04:10 -04:50 pm
10 min break			
Measurement-based Characterization of Passive Electronic Components by Martin Saliternig & Peter Maisel - MSPM Power	10:00 - 10:40 am	04:00 - 04:40 am	05:00 - 05:40 pm
10 min break			
The Search for the Best DC-Bias Components by Melanie Klenner (K&K Prime Engineering) & Joanne Wu (Würth Elektronik)	10:50 - 11:30 am	04:50 - 05:30 am	05:50 - 06:30 pm
1.5 h break			
Single Cable and Connector Bode Diagrams and Step-Load Adapter for DC/DC Bode Measurements by Christian Kück - Monolithic Power Systems	01:00 - 01:40 pm	07:00 - 07:40 am	08:00 - 08:40 pm
10 min break			
PCB Layout Fundamentals by Dr. Ali Shirsavar - Biricha Digital	01:50 - 02:40 pm	07:50 - 08:40 am	08:50 - 09:40 pm
20 min break			
Seamless Software Adaptation of High Performance Power Modules in Power Distribution Networks by Andreas Reiter - Microchip Technology	03:00 - 03:40 pm	09:00 - 09:40 am	10:00 - 10:40 pm
10 min break			
The Interactions Between Power Electronics, Power Integrity, Signal Integrity and EMI by Steve Sandler - Picotest	03:50 - 04:40 pm	09:50 - 10:40 am	10:50 - 11:40 pm
Discussion & Closing			