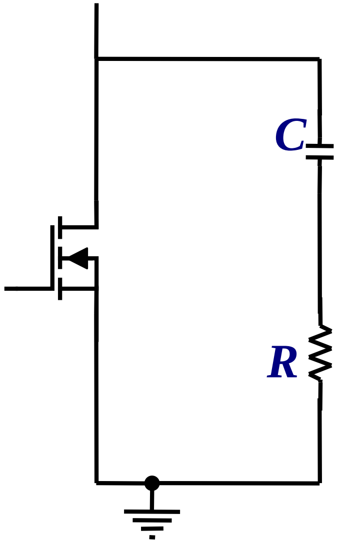
Step-by-step Snubber and Clamp Design for Power Supplies

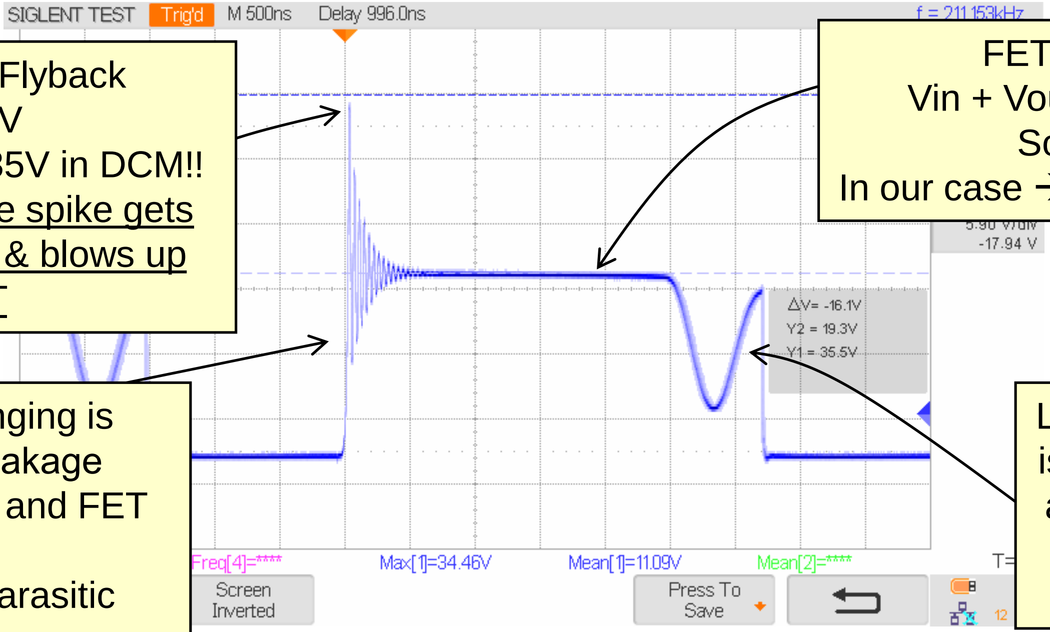
by Dr. Ali Shirsavar

9251 Yonge Street, Suite 206,
Richmond Hill, L4C 9T3,
Ontario, Canada
www.biricha.com

RC Snubber and RCD Clamp Design

- Many topologies require either a snubber or a clamp circuit to suppress ringing and spikes
  - Spikes are usually generated because of leakage inductances
  - Ringing is usually due to Ls and Cs resonating together
- Flyback converters are notorious for having both ringing a large leakage spikes
  - Without snubbers/clamps these spikes/rings could put excessive stress on the device and blow it up





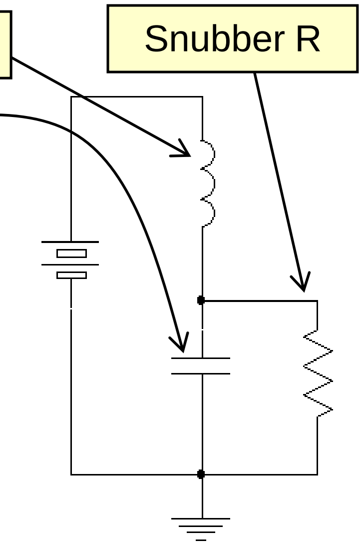
Our workshop Flyback
Vin = 12V
Leakage spike = ~35V in DCM!!
<u>In CCM/full load the spike gets much much larger & blows up the FET</u>

FET reverse voltage =
Vin + Vout (referred to Primary)
So = Vin + N Vout
In our case → 12 + (1:1) x 7.5 = ~19.5V

High frequency ringing is "mostly" due to leakage inductance ($L_{leakage}$) and FET Coss
It decays due to parasitic resistances

Low frequency ringing is occurs in DCM only and is"mostly" due to Primary Inductance, Lp and FET Coss

Primary RC Snubber Design



- Ignoring the snubber cap and the inductor resistance (for ease of analysis) we have:

$$H(s)=\frac{1}{LC\,s^2+\left(\frac{L}{R}\right)s+1}$$

- Comparing this directly with the standard equation for a 2nd order system
  - Where ω_n = resonant frequency and Q is the quality factor (i.e. related to the our resonant bump & our spike
  - We have:

$$H(s)=\frac{1}{\left(\frac{s^2}{\omega_n^2}\right)+\left(\frac{1}{Q\,\omega_n}\right)s+1}$$

$$\boxed{\omega_n=\frac{1}{\sqrt{LC}}\Rightarrow f_r=\frac{1}{2\pi\sqrt{LC}}}\quad\&\quad\boxed{Q=\frac{1}{2\varsigma}=R\sqrt{\frac{C}{L}}}$$

Where *Fr* is the resonant frequency in Hz
& ζ is the damping ratio
(rarely used in PSU analysis and only included for completeness)

- As you can see Q is related to damping; we would like to set Q to 1 so as to damp our system and reduce the spike
- So for Q = 1 we have

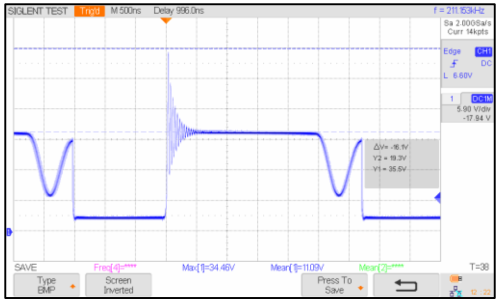
$$\boxed{R=\sqrt{\frac{L}{C}}}$$

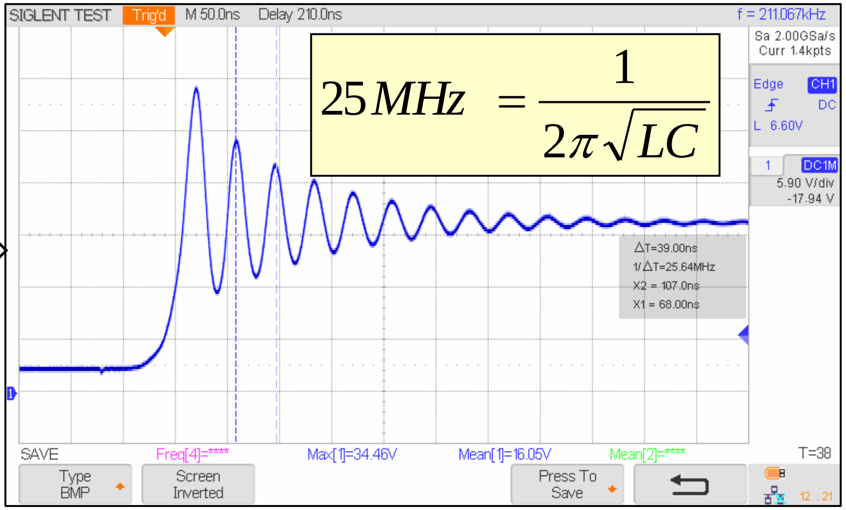
Note: Equations are exactly the same as 2nd stage LC filter discussed earlier

Primary RC Snubber Design

$$R = \sqrt{\frac{L}{C}}$$

- We would like to calculate R
  - We know the leakage L as we can measure it
    - This is total leakage inductance as seen on the primary
    - We measured it in the last lab
- All we need to do it to calculate our parasitic capacitances in our circuit
  - We can do this very easily because we know the equation for the ringing frequency + we can measure the ringing frequency with our scope





$$25\,MHz = \frac{1}{2\pi\sqrt{LC}}$$

We have already measured our transformer leakage, we know the ringing frequency so we can calculate the parasitic capacitance

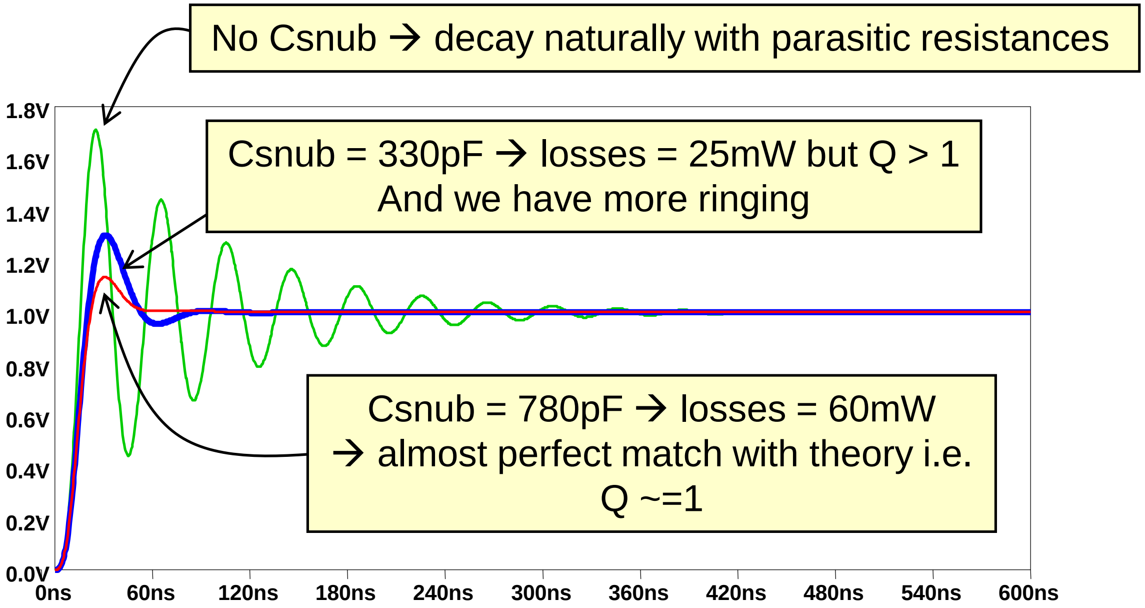
RC Snubber Design

- On the previous slide we measured our leakage to be ~250nH & Fr = 25MHz, therefore:
  - C =~162 pF
  - For Q of 1 R = √(L/C) → R = 39Ω
- An easier method is to substitute equation for Fr from previous sides into equation for R to get:

$$\boxed{For\ Q = 1 \Rightarrow R = 2\pi\ F_r\ L} \quad \Longrightarrow \quad \boxed{2\pi \times 25MHz \times 250nH = \underline{\underline{39\Omega}}}$$

- Up until now we had ignored the impact of the capacitor in our RC snubber
  - Its inclusion would make our equations very complicated so we will use an empirical method
- The snubber capacitor has the following impact
  - The larger the cap, the larger the power loss but the better our Q; i.e.
    - If we use a large cap we will get perfect correlation and a Q of 1 but have massive losses
    - If we use a very small cap then we will have low losses but larger Q and more oscillations
    - A good compromise is to calculate the cap value such that the losses are limited to around 25 to 60mW → this will avoid creation of hot spots on the PCB whilst maintaining a low Q
- The equation for losses in our snubber is: $\boxed{P_{loss\_snub} = C_{snub}\ V_{C\_snub}^{2}\ F_s}$

Primary RC Snubber Design



No Csnub → decay naturally with parasitic resistances

Csnub = 330pF → losses = 25mW but Q > 1
And we have more ringing

Csnub = 780pF → losses = 60mW
→ almost perfect match with theory i.e. Q ~=1

A good compromise is to calculate capacitor such the losses are circa 25 to 60mW to avoid hot spots on the PCB

$$P_{loss\_snub} = C_{snub} V_{C\_snub}^{2} F_{s}$$

Voltage on drain at at turn off = (Vin + N Vo)
In our case = 12V + (1:1)Vo = 19.5V

In our case for 25mW, Vsnub = 19.5V & Fs =200kHz → <u>Csnub = 330pF</u>

Secondary RC Snubber Design

- At diode turn off the secondary diode parasitic capacitance will ring with the leakage of the Flyback transformer
- The procedure and the design equations are exactly the same as primary:
  - Step 1: Measure leakage (L) as seen on the primary and refer to secondary

Measured total leakage on the secondary side

In our case

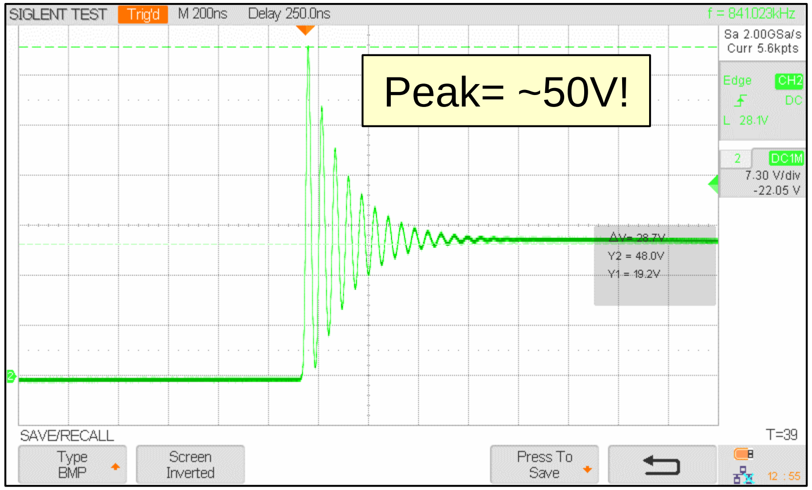
250nH

  - Step 2: Measure resonant frequency from the ringing on the scope plot and use along with leakage inductance to calculate Rsnub

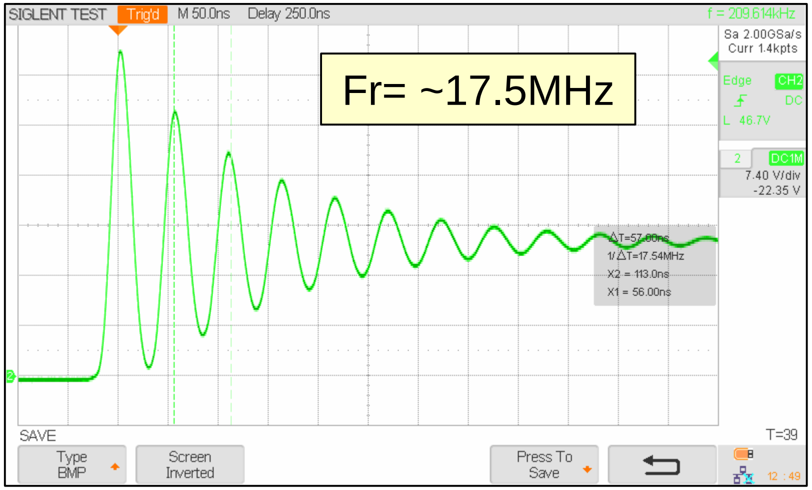
$$For\ Q = 1 \Rightarrow Rsnub = 2\pi\ F_r\ L$$

In our case

2π 17.5MHz 250nH = ~27Ω
We actually used 33Ω



Peak= ~50V!



Fr= ~17.5MHz

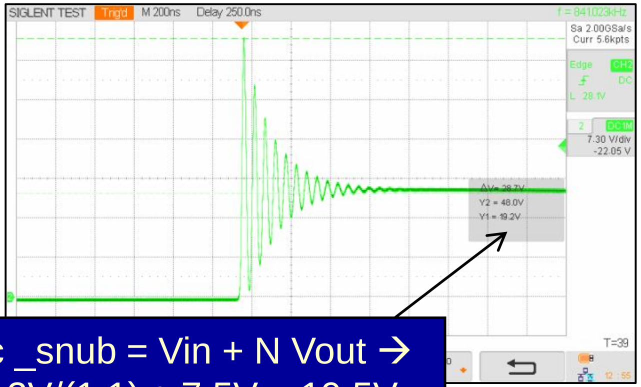
Secondary RC Snubber Design

- Secondary Snubber Design Steps (continued)
  - Step 3: Calculate Csnub based on power dissipation of 25 to 60mW

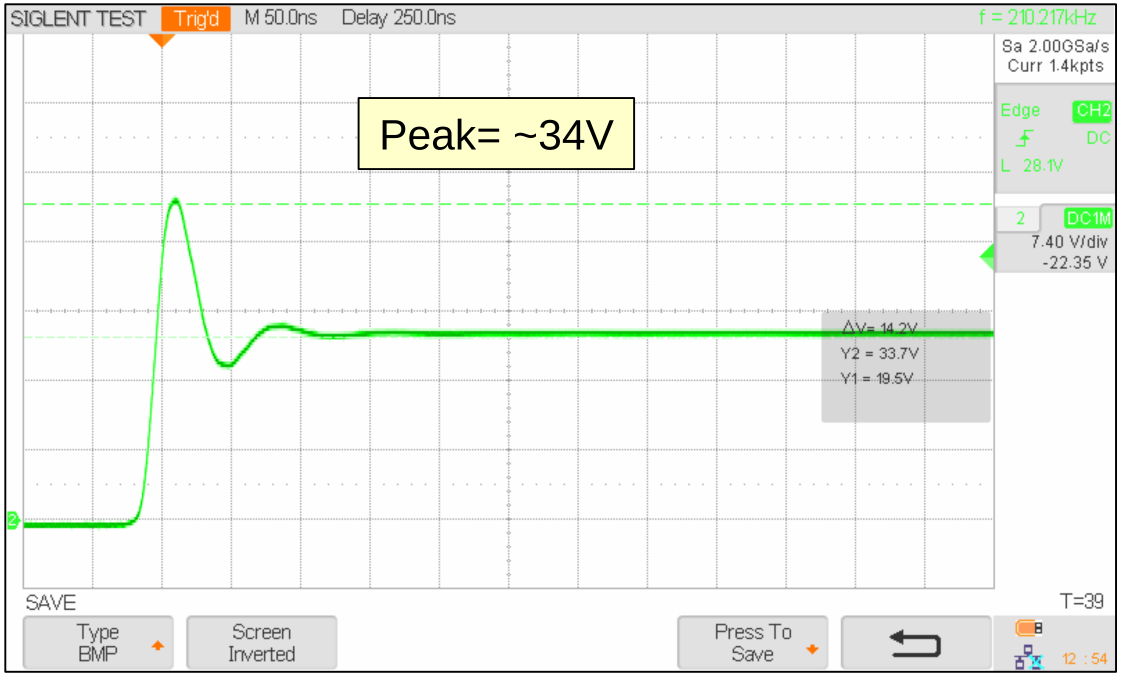
$$P_{loss\_snub} = C_{snub} V_{C\_snub}^2 F_s$$

In our case
Let's say 35mW
dissipation

Csnub = 35mW / (19.5^{2}V x 200kHz) = 460pF
We actually used 470pF



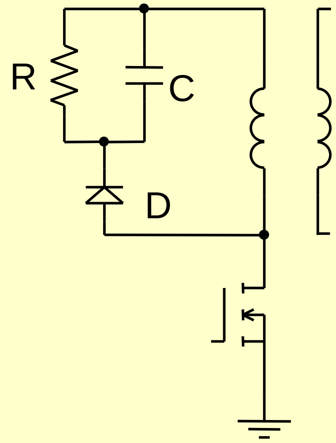
Vc _snub = Vin + N Vout →
12V/(1:1) + 7.5V = 19.5V



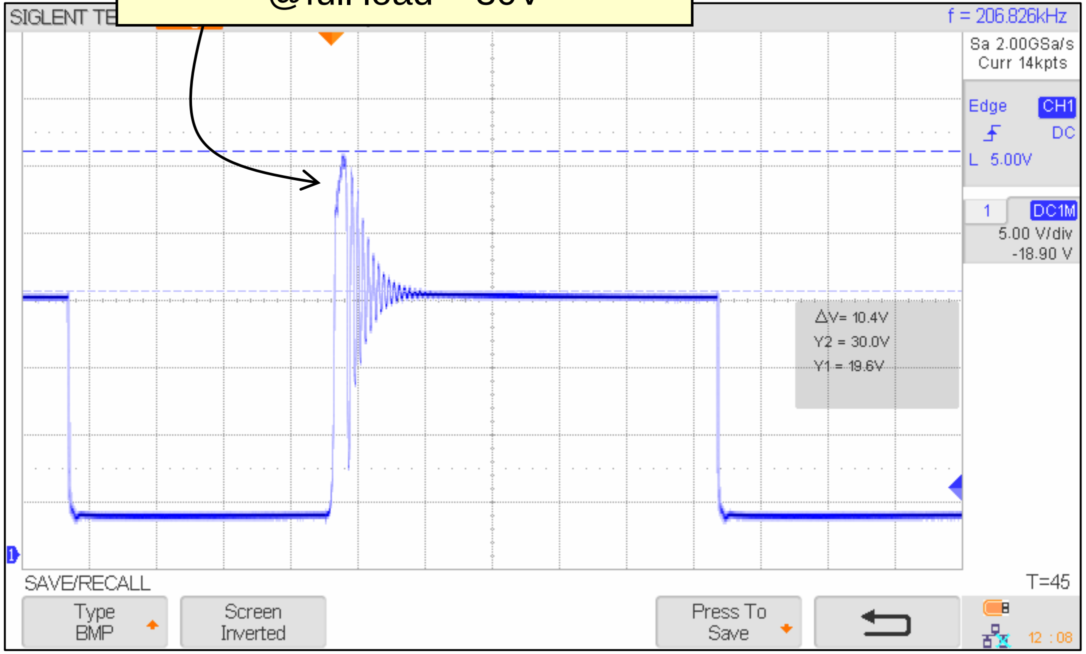
Peak= ~34V

RCD Clamp Design

- On some occasions (particularly in Flybacks) where the leakage spike is very high, an RC snubber is not enough
  - We would like physically clamp/clip the peak of the spike to a voltage that is not going to damage our FET
  - The most common is an RCD clamp



RCD Clamp

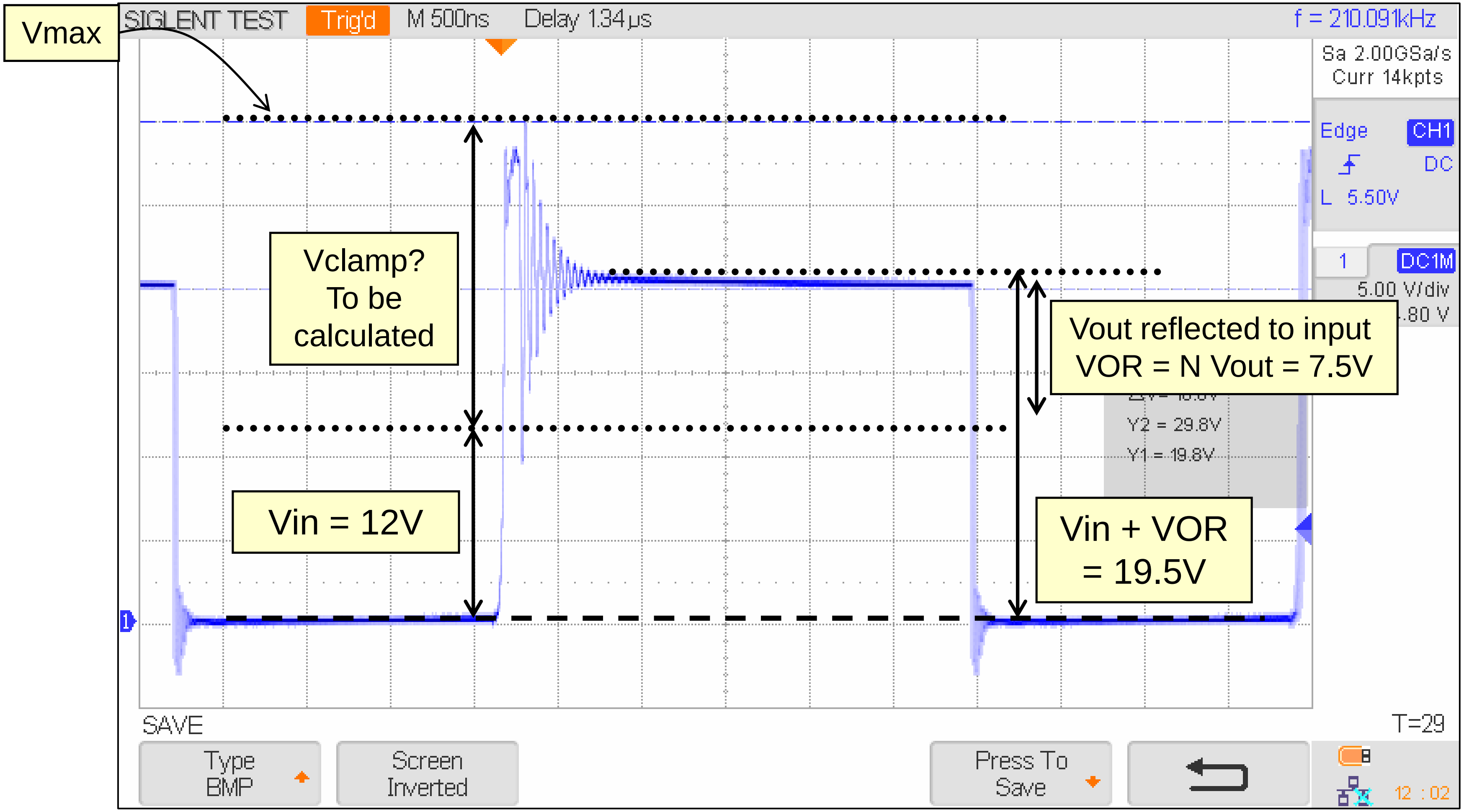


Leakage spike with RCD clamp
@full load = 30V

SIGLENT TE
f = 206.826kHz
Sa 2.00GSa/s
Curr 14kpts
Edge CH1
DC
L 5.00V
1 DC1M
5.00 V/div
-18.90 V
ΔV= 10.4V
Y2 = 30.0V
Y1 = 19.6V
SAVE/RECALL
T=45

RCD Clamp Design

If max desired voltage on FET = 30V
Then Vclamp = 30 – 12 = 18V



Vmax

Vclamp?
To be calculated

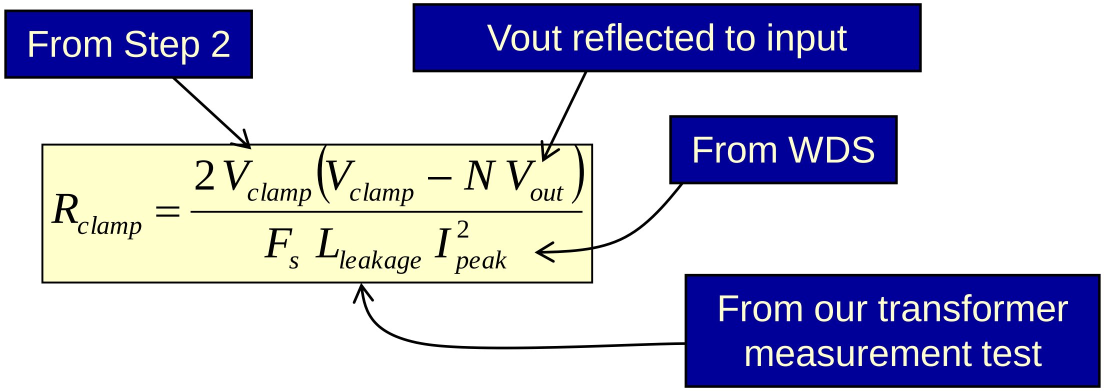
Vin = 12V

Vout reflected to input
VOR = N Vout = 7.5V

Vin + VOR
= 19.5V

RCD Clamp Design

- Step 1: Select maximum voltage, Vmax that we are going to allow on our FET
  - The higher this voltage the lower the losses in the snubber, we would like the maximum spike possible without damaging the FET
    - Typically 66% of the FET's maximum allowable voltage or 85% of FETs maximum allowable voltage minus 20V to allow for overshoot is a good compromise
    - As an alternative you can calculate exactly how much power loss you are willing to tolerate in the clamp and make sure and then reverse calculate the maximum clamp voltage
      - Please see Basso's book for exact equations
- Step 2: Calculate Vclamp
  - From previous slides: Vclamp = Vmax - Vin
- Step 3: Calculate Rclamp from this*:



From Step 2

Vout reflected to input

From WDS

From our transformer measurement test

$$R_{clamp} = \frac{2\,V_{clamp}\left(V_{clamp} - N\,V_{out}\right)}{F_s\;L_{leakage}\;I_{peak}^2}$$

* See Basso "Switch-Mode Power Supplies Spice Simulations and Practical Designs" for full proofs of equations

RCD Clamp Design

- Step 4: Calculate Cclamp
  - Unlike the RC snubber, the value of RCD capacitor does not impact the losses
  - Its value therefore is not crucial; it just needs to be large enough such that voltage remains constant during the snubber operation
  - It is essentially an RC circuit so a good compromise would be to allow 2.5 to 5 time constants*:

$$\boxed{C_{clamp} = \frac{5}{R_{clamp} \; F_s}}$$

  - Step 5: Calculate total power loss in the snubber*

$$\boxed{P_{loss\_clamp} = \frac{1}{2} L_{leakage} \; I_{peak}^{2} \; F_s \left(\frac{V_{clamp}}{V_{clamp} - N V_{out}} \right)}$$

    - If power loss is too much then you need to increase the clamping voltage which could mean buying a bigger FET

---

* See Basso “Switch-Mode Power Supplies Spice Simulations and Practical Designs” for full proofs of equations

RCD Clamp Real Life Example

- Steps 1 & 2: for our workshop Flyback:
  - Vin = 12V, Vout = 7.5V, N = 1:1 → N Vout = (1:1) x 7.5V = 7.5V,
  - Ipeak = 2.5A from WDS
  - We select Vmax = 30V; therefore Vclamp = 30V – 12V = 18V
- Step 3:

$$R_{clamp} = \frac{2\,V_{clamp}\left(V_{clamp} - N\,V_{out}\right)}{F_s\ L_{leakage}\ I_{peak}^2} = \frac{2\times 18V\times\left(18V - \left(\left(1:1\right)7.5V\right)\right)}{200kHz\times 250nH\times\left(2.5A\right)^2} = \underline{\underline{1200\Omega}}$$

- Step 4: Cap value not crucial

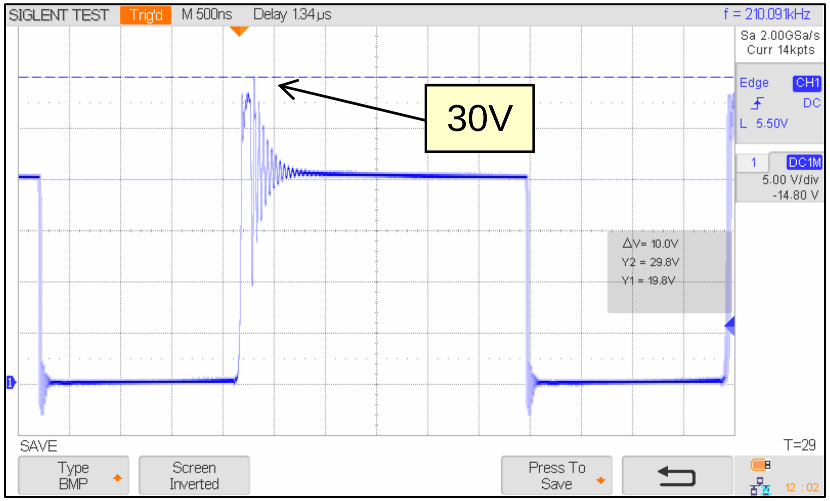
$$C_{clamp} = \frac{2.5\ to\ 5}{R_{clamp}\ F_s} = \underline{\underline{10\ to\ 20nF}} \Rightarrow We\ in\ fact\ used\ 10nF$$

- Step 5: total snubber power loss:

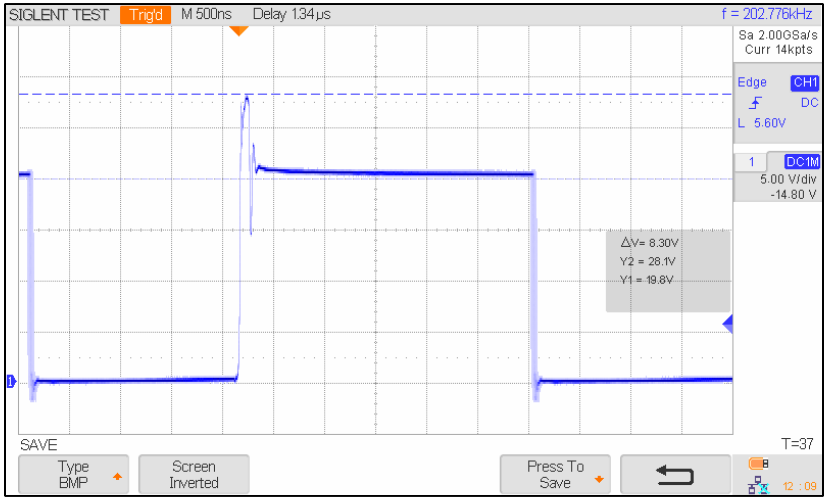
$$P_{loss\_clamp} = \frac{1}{2}\,L_{leakage}\ I_{peak}^2\ F_s\left(\frac{V_{clamp}}{V_{clamp} - N\,V_{out}}\right) = 267mW$$

RCD Clamp Real Life Example

- Real results match almost perfectly with theoretical calculated values:



30V



RCD Clamp only
As designed in previous slides

RCD clamp + primary RC snubber
As designed in previous slides

Important Notice

All material presented in this workbook, associated software, exercises, appendices and oral presentations made as part of Biricha Digital Power Ltd's workshops and seminars are for educational purposes only and are not intended for production or commercial applications and may contain irregularities and defects or errors. Furthermore, none of the material has been tested or certified by any government agency or industry regulatory organization or any other third party organization.

Biricha Digital Power Ltd makes no warranties or representations, express, implied or statutory, including any implied warranties of merchantability, fitness for a particular purpose, lack of viruses, lack of patent infringements, accuracy or completeness of responses and lack of negligence. Prior to using, incorporating or distributing any of the material that has been presented to you as part of this workshop in any commercial product, you must thoroughly test the product and the functionality in that product and be solely responsible for any problems or failures.

In no event shall Biricha Digital Power Ltd, or any applicable licensor, be liable for any special, indirect, incidental, or punitive damages, however caused, arising in any way out of your use of the material presented in this workshop. These excluded damages include, but are not limited to, cost of removal or reinstallation, procurement of substitute goods or services, outside computer time, labour costs, loss of data, loss of goodwill, loss of profits, loss of savings, loss of use or interruption of business or other economic loss.