Automated PCB Parasitics Extraction from EDA Tools for Power Electronics Design Support

Sven FIEßER, PhD student, Technical University Ilmenau

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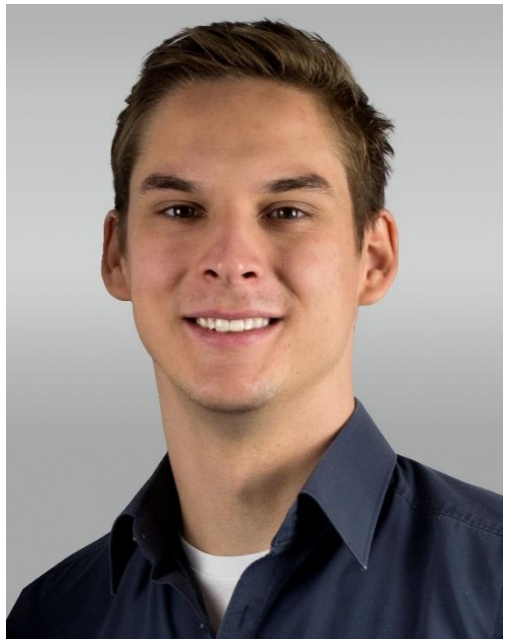
Personal Introduction



Sven Fießer

PhD Student: Research in HV-SMPS for magnetron applications and SMPS/PCB design at the Technical University Ilmenau

In cooperation with:

University of Applied Sciences Fulda, Germany

Prof. Dr.-Ing. Ulf Schwalbe

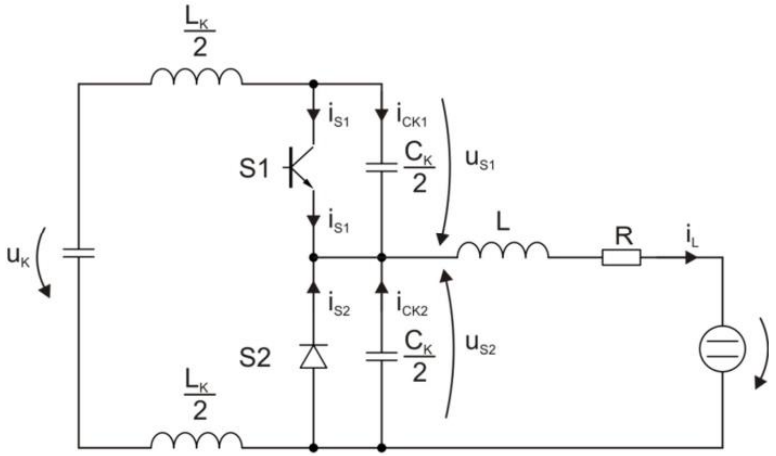
University of Applied Sciences Fulda

- Renewable Energies
- E-Mobility
- Power Electronics
- Energy Storage Systems for Grid Integration

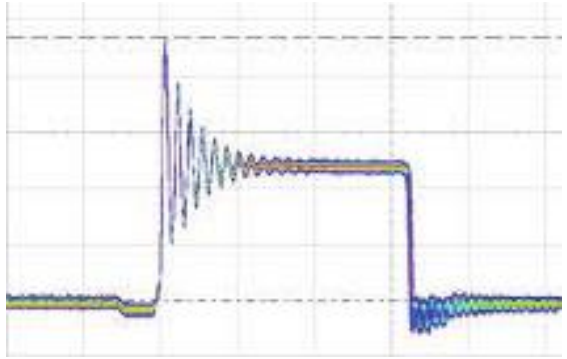
Agenda

1. Background Information
2. Methods for Parasitic Extraction
   a. Inductances and Resistances
   b. Capacitances
3. Verification
4. Automated Parasitic Extraction
5. Simplification by Critical Path Extraction
6. Conclusion

Background Information



Parasitic components in every power converter



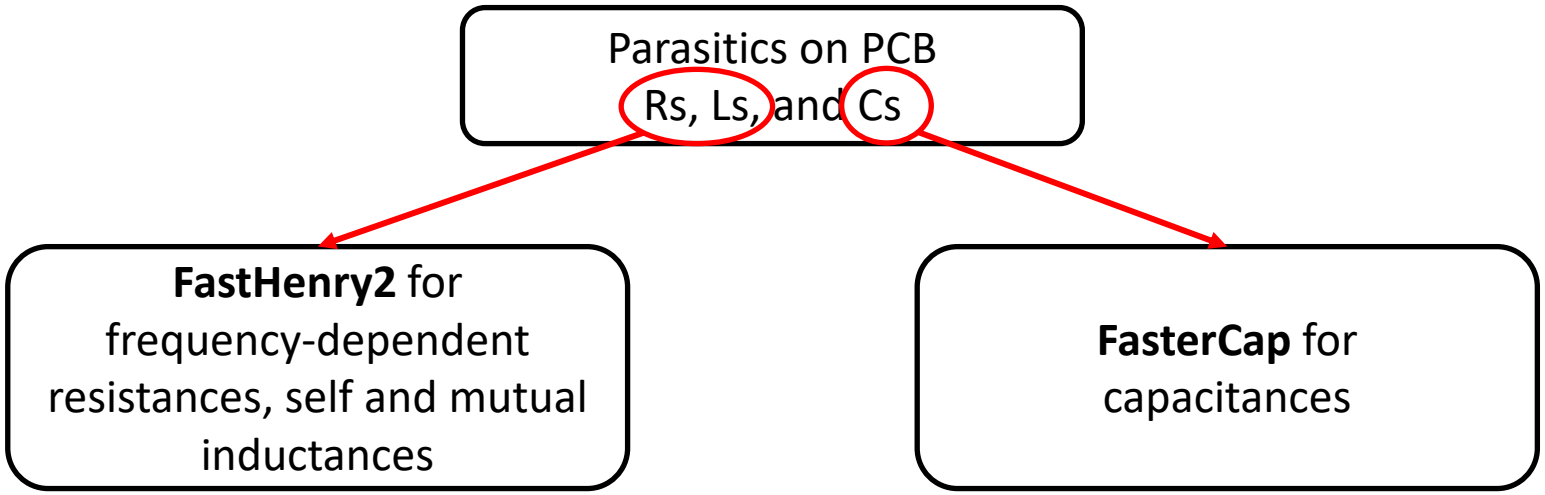
Source: R. Taylor 2012

Results in unwanted ringing in the switching elements

Increasing the power density by higher switching frequencies (e. g. with GaN and SiC semiconductors)
→ Low parasitic PCB components are necessary

→ Several design iterations until a good layout is created
→ Reduce design process by evaluating its effects while routing the PCB

Method for Parasitic Extraction



Method for Parasitic Extraction

FastHenry

- Developed at M.I.T. on Unix platform
- For the solution of Maxwell equations and extraction of **inductances** and **resistances** (includes **coupling** effects) in 3D
- FastHenry2 as a Windows porting

FastCap

- Developed at M.I.T. on Unix platform
- For the solution of Maxwell equations and extraction of **capacitances** in 3D
- FastCap2 as a Windows porting
- FasterCap with several improvements (lossy dielectrics, automatic mesh refinement, …)

→ FOSS

Source: fastfieldsolvers.com

Method for Parasitic Extraction

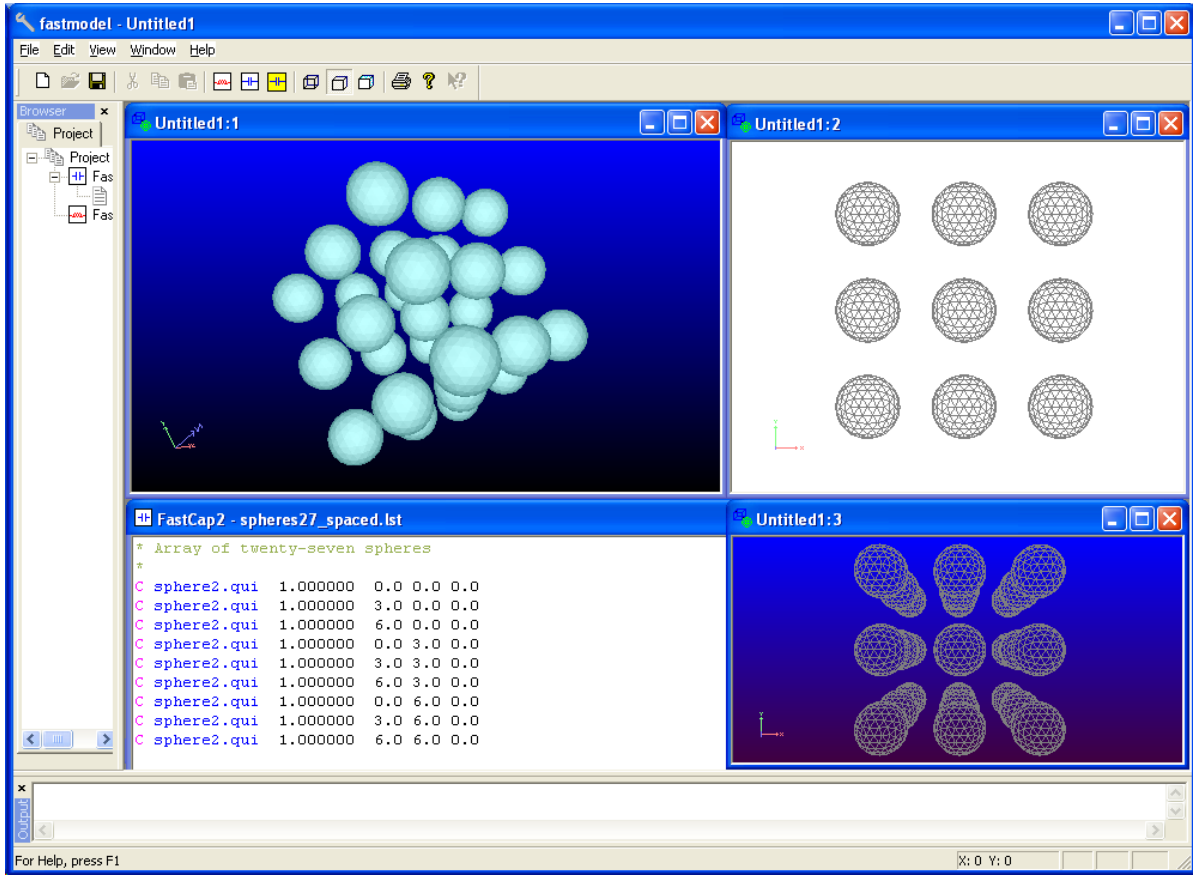
FastModel

Windows 3D viewer and text editor for FastCap2, FasterCap and FastHerny2

Download:

www.fastfieldsolvers.com/download.htm

(contact form can be left empty)



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Method for Parasitic Extraction

Converter for FastHenry2

Input

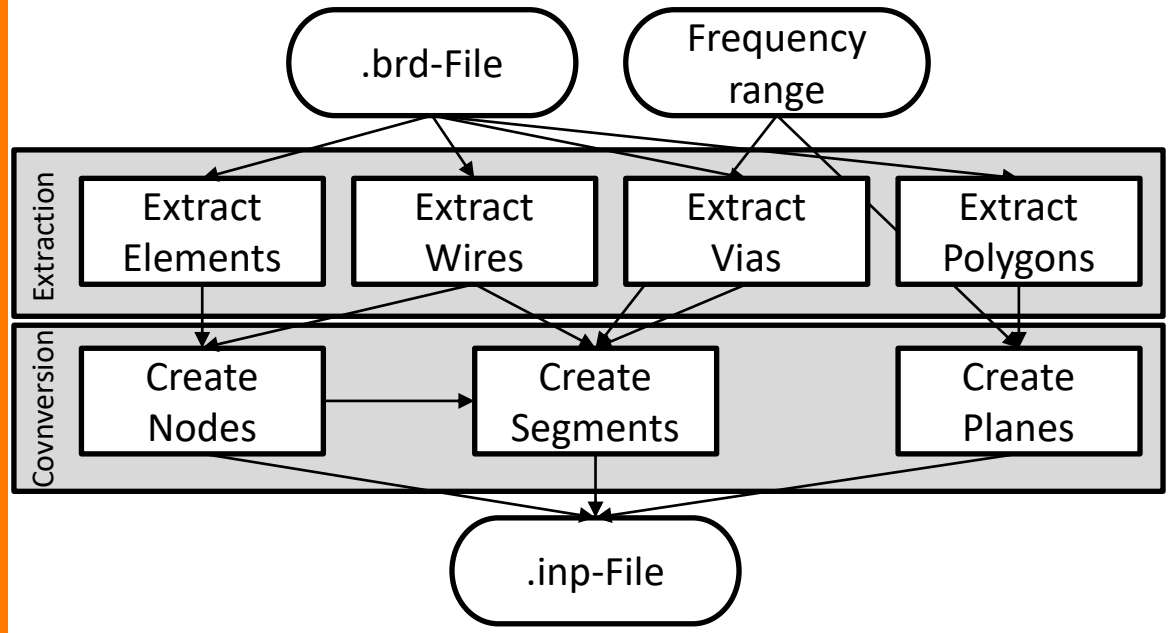
- Geometry of the *copper traces* in 3D using
  - Elements (connection between two Nodes) → Wires
  - Planes (incl. Holes) → Planes
- Frequency range
- Material properties of the copper (conductivity)

Output

- Maxwell matrix for each frequency
- SPICE model

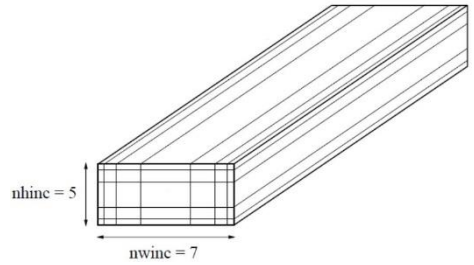
Method for Parasitic Extraction

Converter for FastHenry2



FastHenry2 Inputfile Example

```
.Units MM
.Default z=0 sigma=5.8e4

*NODES
*=====
N1_X16_1 x=23.025 y=53.5611 z=1.6
N2 x=38.5889 y=53.5611 z=1.6
N3_C12_+ x=39.0 y=53.15 z=1.6
...

*ELEMENTS (== wires)
*===================
E1 N1_X16_1 N2 w=2 h=0.035 nwinc=15 nhinc=4
E2 N2 N3_C12_+ w=2 h=0.035 nwinc=15 nhinc=4
...

*PLANES
*======
g1N$27 x1=69.0 y1=23.0 z1=1.6 x2=69.0
+y2=58.0 z2=1.6 x3=121.0 y3=58.0 z3=1.6
+thick=0.035 seg1=100 seg2=100
+nQ6_2 (100,28,1.6)
+nD3_1 (118,48,1.6)
+hole rect (115,29,1.6,121,23,1.6)
+hole rect (112,26,1.6,115,23,1.6)
…

*START- AND ENDPOINTS
*====================
.external nQ6_2 nD3_1
...

*FREQUENCY RANGE
*===============
.freq fmin=100 fmax=100e6 ndec=1
.end
```



Source: M. Kamon 1996

$$\delta > \begin{cases} \dfrac{W}{2\sum_{i=0}^{nwinc/2-1} r^i} & \text{if } nwinc = \text{even}, \\ \dfrac{W}{r^{\frac{nwinc-1}{2}} + 2\sum_{i=0}^{(nwinc-1)/2-1} r^i} & \text{if } nwinc = \text{odd}. \end{cases}$$

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Method for Parasitic Extraction

Converter for FasterCap

Input

- Geometry of the *copper traces and PCB* in 3D using
  - Triangles or Squares
- Material properties of the PCB (relative permittivity)

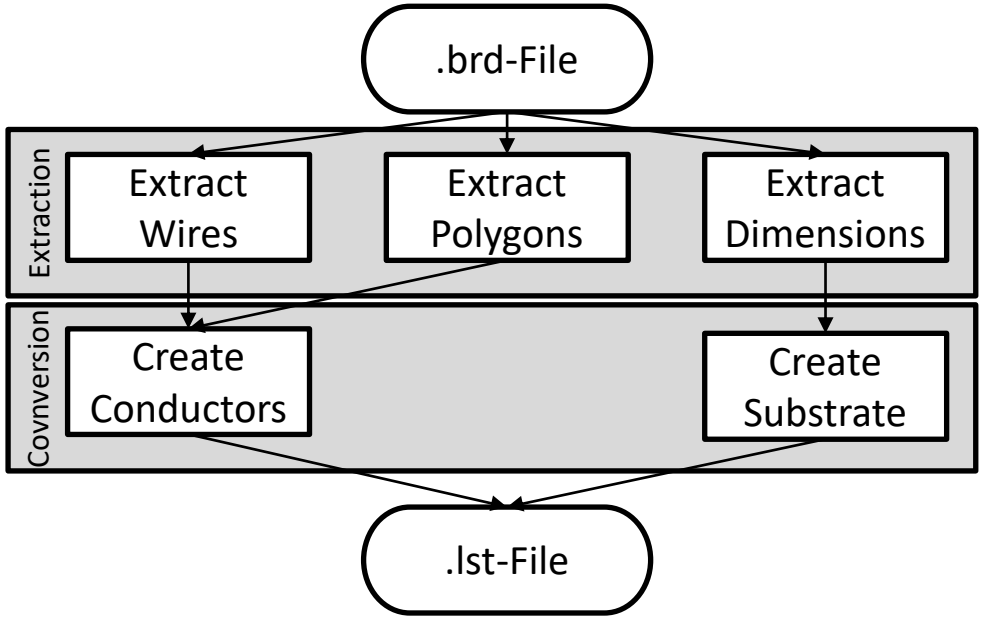
  → for FR4 approx. 4 (see datasheet)

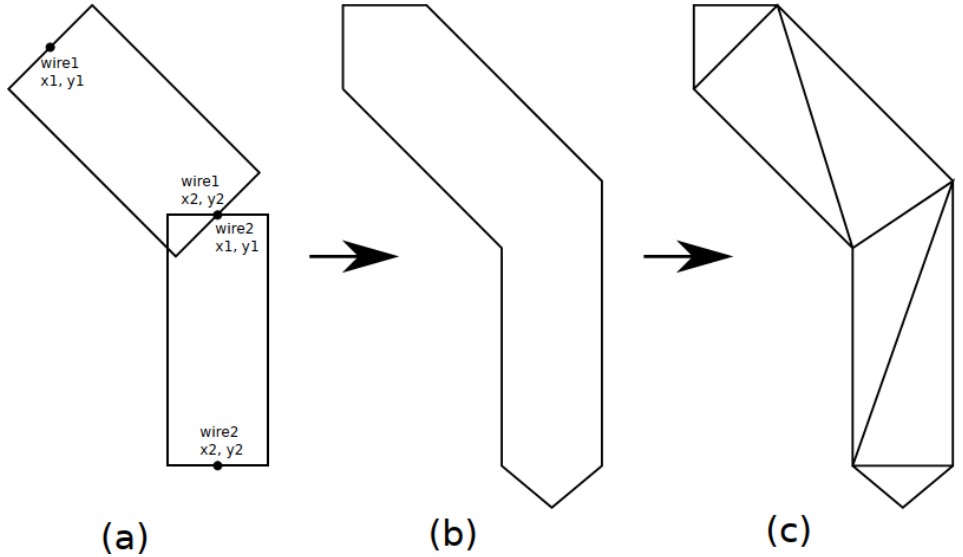
Output

- Maxwell matrix

Method for Parasitic Extraction

Converter for FasterCap



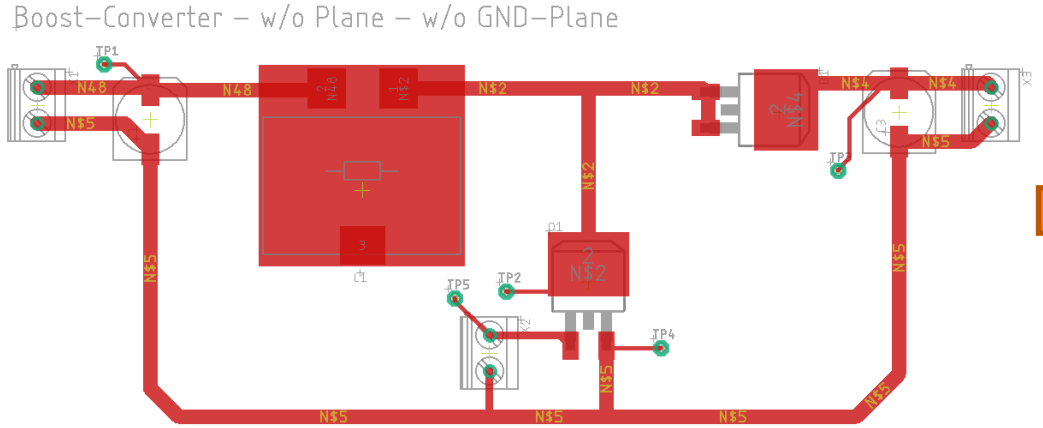


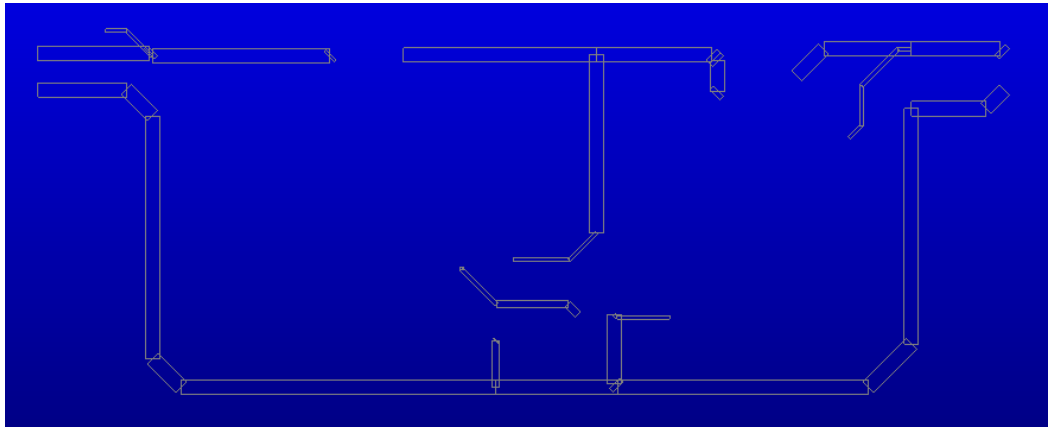
- For FasterCap only a rough mesh is needed → FasterCap does the mesh refinement (FastCap needs this to be done by hand)
- The meshing is done using **Gmsh**

www.gmsh.info

Method for Parasitic Extraction

Example FastHenry2 - Backend

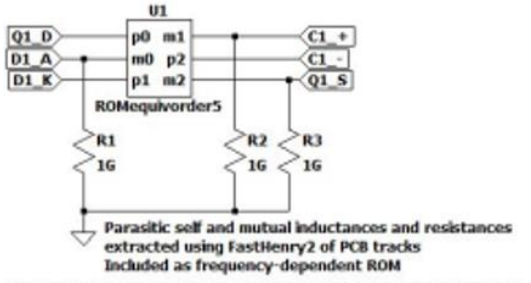




Maxwell-Matrix for each given frequency

```
Computed matrices (R+jL)
 Row 0:  n4 to n5       *C1_+ - L1_2
 Row 1:  n9 to n10      *L1_1 - Mittelpunkt
 Row 2:  n10 to n16     *Mittelpunkt - Q1_2
 Row 3:  n10 to n12     *Mittelpunkt - D1_1
 Row 4:  n25 to n26     *D1_2 - C3_+
 Row 5:  n45 to n46     *Q1_3 - Punkt zu GND
 Row 6:  n35 to n46     *C3_- - Punkt zu GND
 Row 7:  n46 to n42     *Punkt zu GND - C1_-
 Freq = 1e+06
  Row 0: 0.0075634+1.80117e-08j 1.35612e-06+2.03218e-09j 5.33902e-07-1.16422e-12j 1.03528e-06+7.08856e-10j 3.14947e-07+3.42858e-10j 2.31338e-07-1.70688e-12j -3.34644e-06-1.18411e-09j 7.25318e-07-3.00028e-09j
  Row 1: 1.3411e-06+2.03233e-09j 0.00812196+2.01008e-08j 9.88968e-08-1.15908e-12j 3.56848e-05+2.80854e-09j 3.69332e-07+6.55626e-10j 2.00173e-07-2.01634e-12j -5.90326e-06-1.86375e-09j -1.16568e-05-3.28489e-09j
  Row 2: 5.25811e-07-1.12886e-12j 9.68636e-08-1.11943e-12j 0.00748078+1.8141e-08j 2.45561e-06+5.13625e-11j 3.40801e-07-2.96845e-13j 1.78785e-06+8.99193e-10j -3.58937e-07+1.99873e-09j -2.23086e-06-1.40691e-09j
  Row 3: 1.05978e-06+7.22454e-10j 3.56755e-05+2.80852e-09j 2.4586e-06+5.1317e-11j 0.00507248+1.08617e-08j -1.25971e-06+7.13035e-10j 3.7836e-07+8.71661e-12j -4.08145e-06-1.31808e-09j -7.36468e-06-1.76729e-09j
  Row 4: 3.29958e-07+3.47244e-10j 3.59011e-07+6.5567e-10j 3.45459e-07-3.1816e-13j -1.26473e-06+7.1307e-10j 0.00367591+7.27724e-09j 4.13288e-08-3.5601e-13j -3.67522e-06-1.00109e-09j -3.35448e-06-9.59923e-10j
  Row 5: 2.16733e-07-1.73563e-12j 2.07737e-07-2.0763e-12j 1.79547e-06+8.99142e-10j 3.77779e-07+8.72701e-12j 4.05103e-08-3.55199e-13j 0.00293433+5.30378e-09j -6.51506e-05+7.08669e-10j 5.63014e-05-3.93222e-10j
  Row 6: -3.56666e-06-1.19742e-09j -6.05793e-06-1.86264e-09j -3.87833e-07+1.99894e-09j -4.17694e-06-1.31733e-09j -3.75499e-06-1.00048e-09j -6.51656e-05+7.08807e-10j 0.0233713+6.46531e-08j -0.000127451+5.44038e-09j
  Row 7: 5.48584e-07-2.99955e-09j -1.19656e-05-3.28263e-09j -2.34312e-06-1.40628e-09j -7.55533e-06-1.7827e-09j -3.49382e-06-9.53236e-10j 5.63034e-05-3.93169e-10j -0.000128158+5.44799e-09j 0.0307431+8.87394e-08j
```

SPICE model



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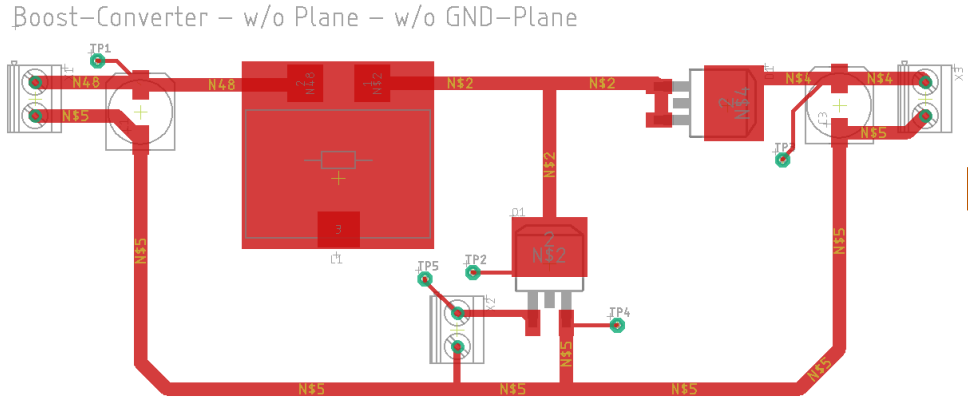
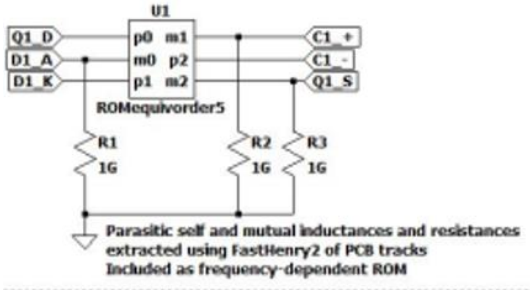
Method for Parasitic Extraction

Example FastHenry2 - Frontend



Name	L	R	ΔL	ΔR
Cond1	10 nH	1 mΩ	- 10 %	- 11 %
Cond2	15 nH	2 mΩ	+ 15 %	+ 16%
Cond3	20 nH	3 mΩ	- 10 %	- 11 %
…	…	…	…	…

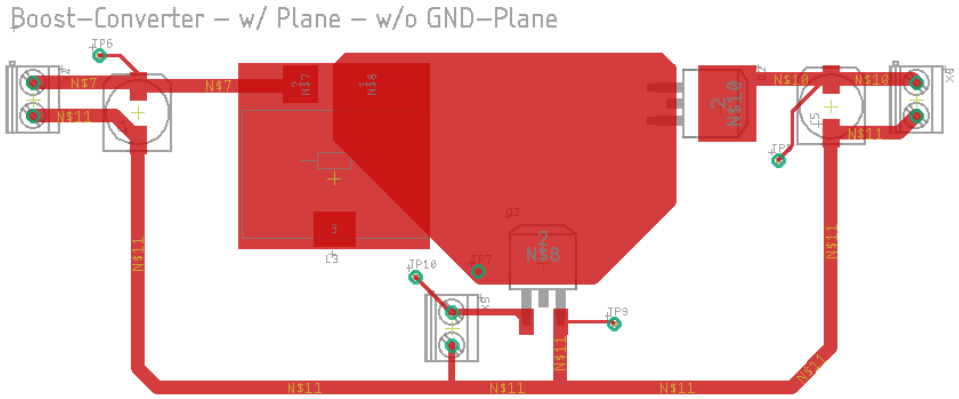
SPICE model

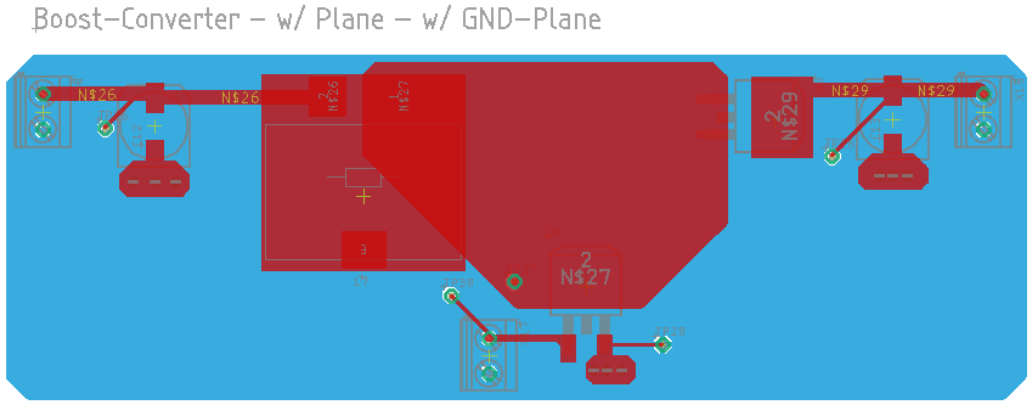


Extraction process for FasterCap is similar

Method for Parasitic Extraction

Optimization Process





Exemplary optimization by

1. Insertion of a plane in the critical path

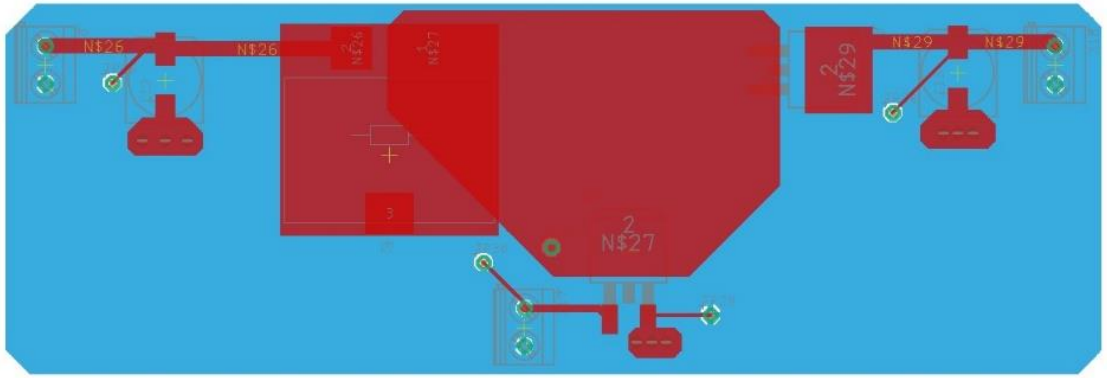
2. Insertion of a ground plane

→ Evaluation of the parasitic components and its influences

Verification

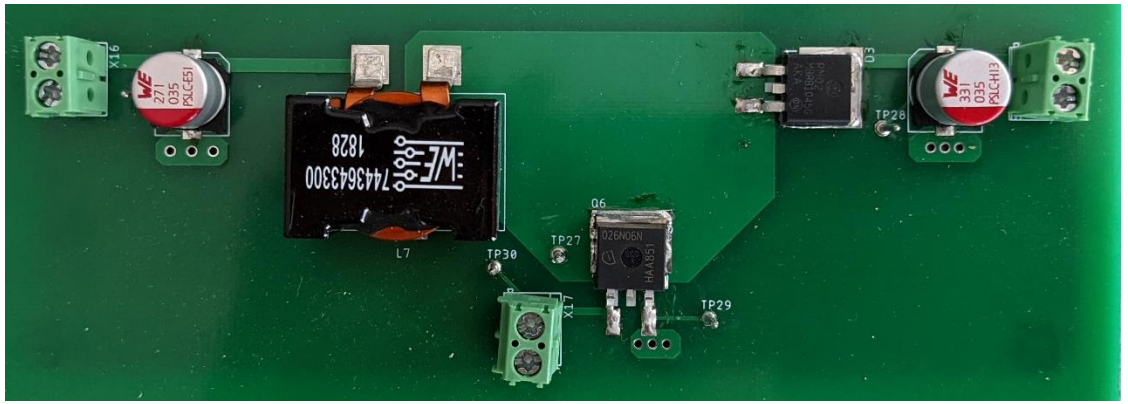
1. Autodesk EAGLE
2. RCL extraction from EAGLE

Boostconverter in EAGLE:



3. Boostconverter-PCB verification setup

Boostconverter-PCB for verification:



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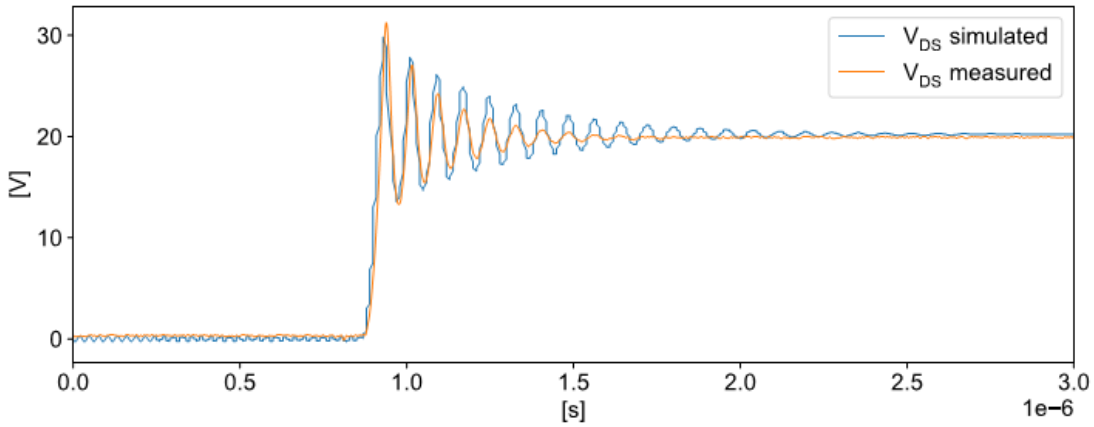
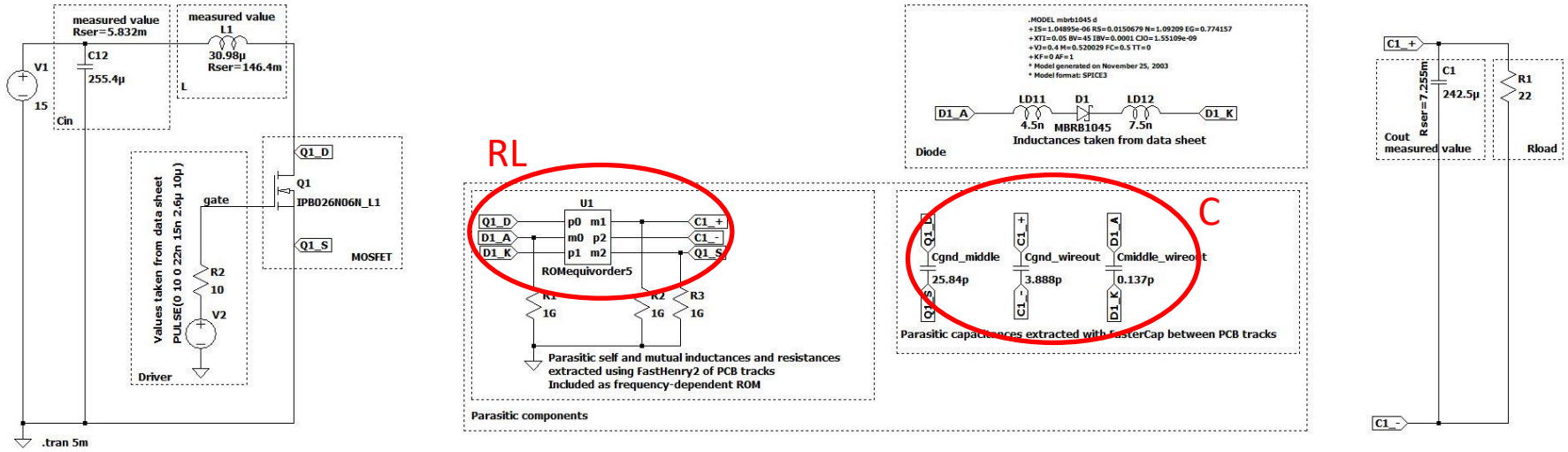
Verification

4. SPICE simulation
   a. Parasitic RCL included
   b. Switch/Diode models included
5. Comparison simulation and actual board

Comparison simulated and measured data:



SPICE simulation including PCB parasitics:



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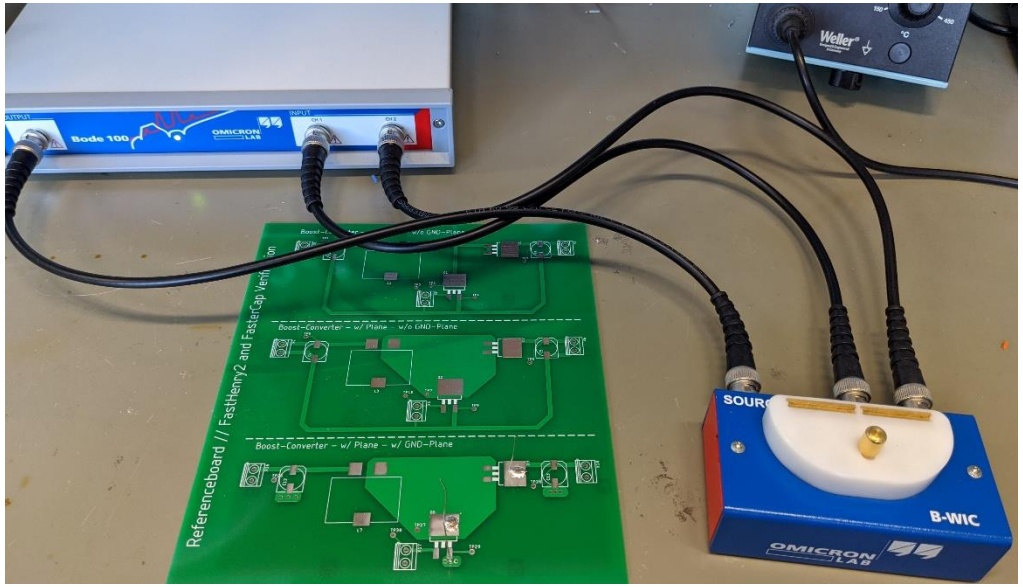
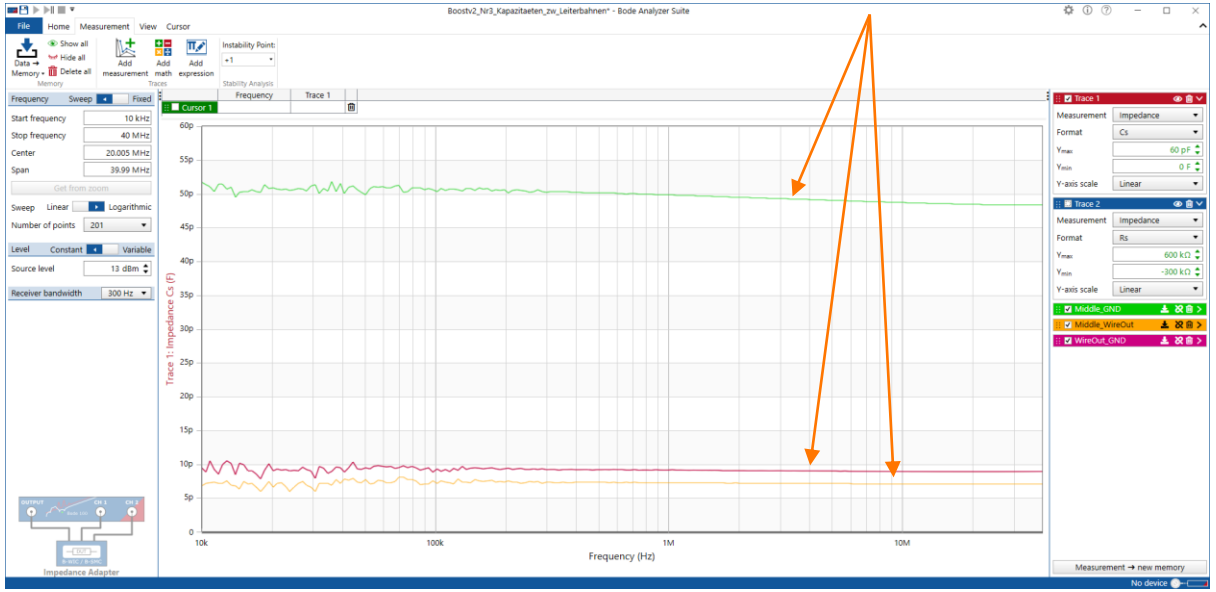
Verification

Measurement of the parasitic capacitances between the wires using the **Bode 100** from Omicron Lab.



Parasitic Capacitances between each conductor



→ Measured capacitances match quite the simulated values.

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Benefits

- Why go through so much trouble?
- Why not use the rule of thumb for inductance of PCB tracks? → *8 nH/cm*

Pro:

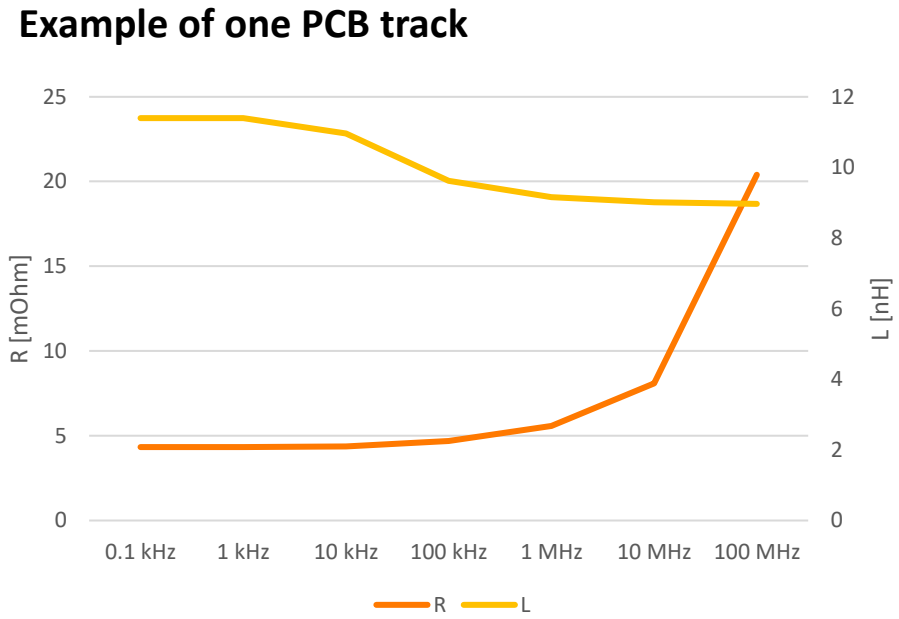
+ easy

Con:

- Width and height neglected
- No skin effect ($f_{ringing} > f_s$)
- No coupling effects (e. g. GND-planes)

→ Proper selection of switching components (V_{ds_max} and P_{v_max})

→ Proper dimensioning of snubber elements



Source: www.powersystemsdesign.com/articles/pcb-layout/22/5871

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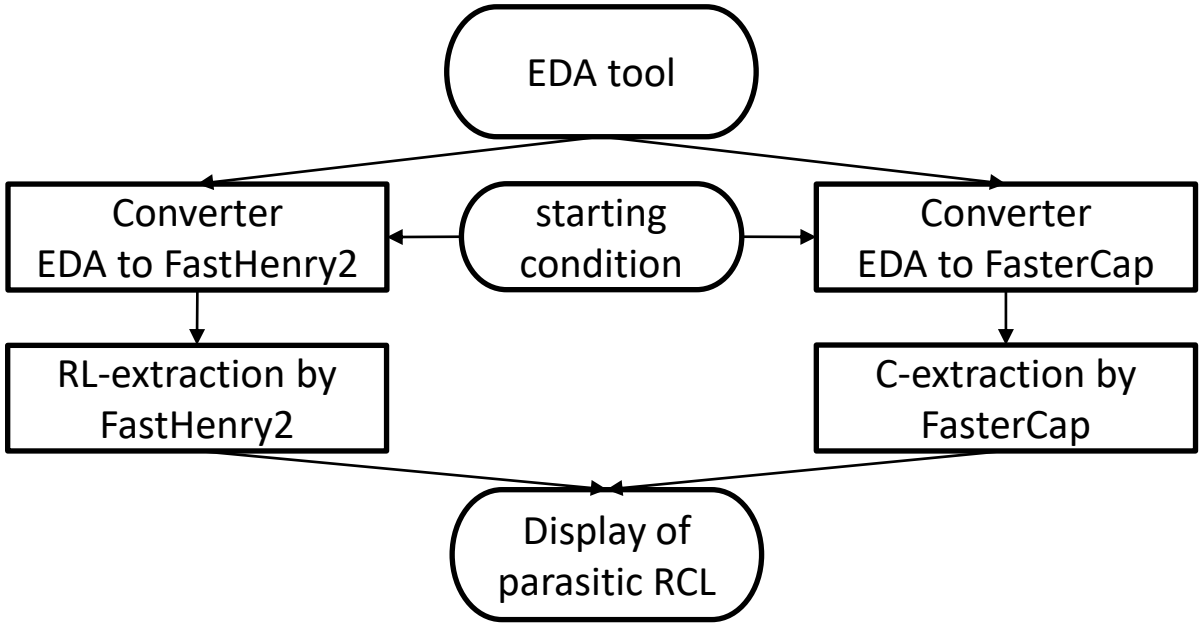
Automated Parasitic Extraction

Second program for continuous RCL extraction



Simplification by Critical Path Extraction

Problem so far: The converters convert *every* wire on the PCB

Solution: Tell the converters which wires to extract

→ only in the critical path

Not everyone knows where the critical path in every converter is

→ Calculate it

Simplification by Critical Path Extraction

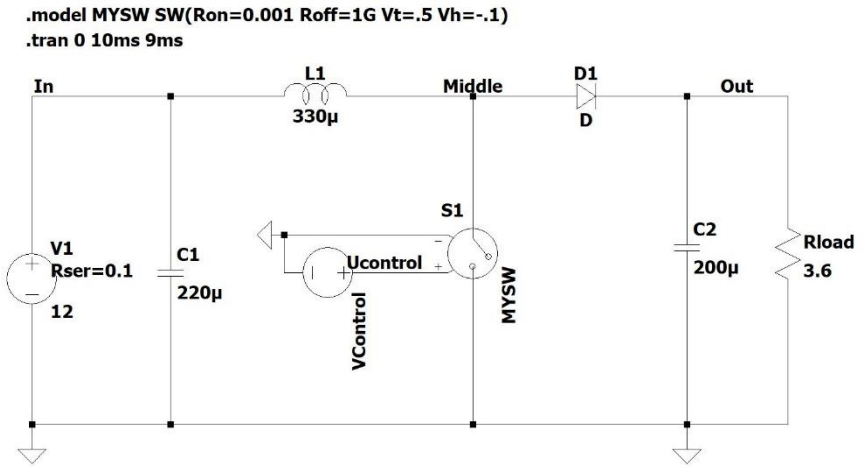
Extraction using SPICE

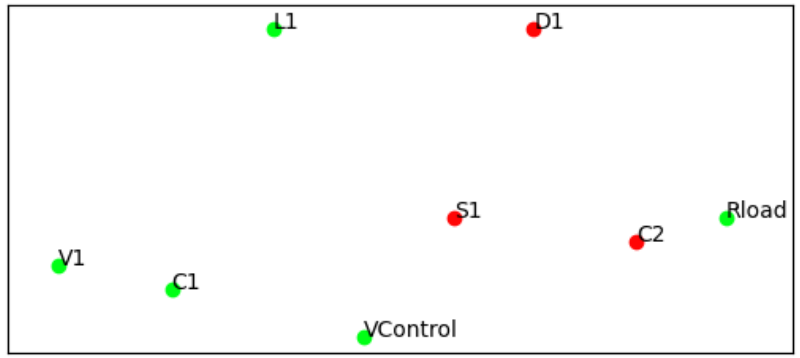
1) Creation of a (ideal) SPICE file.
2) Run the simulation and parse the waveform file.
3) Calculate *di/dt* and *du/dt* of every waveform according to equation 1.
4) Calculate the rms value of the differentiated waveforms according to equation 2. The highest values indicate the critical path.

$$\frac{\Delta x}{\Delta t} = x_{t+1} - x_t \qquad (1)$$

$$RMS\ of\ diff.\ waveform = \sqrt{\frac{\sum_i^n (\frac{\Delta x_i}{\Delta t_i})^2}{n}} \qquad (2)$$

Simplification by Critical Path Extraction





Ideal boost converter used for the critical path extraction

Graphical output of each element from the Simulation color-coded (red: critical path)

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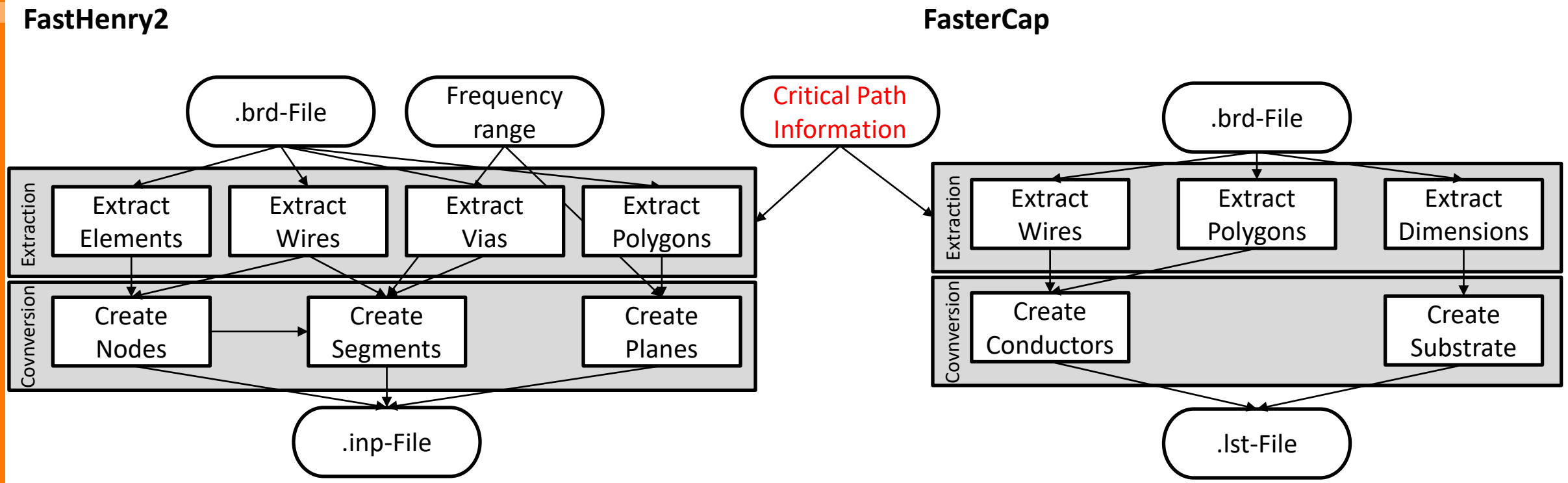
Simplification by Critical Path Extraction



Current and Future Works and Limitations

- Parasitic extraction works well with “easy” geometries
- Wires and planes on top of each other not supported yet

- How to prevent GIGO:
  - PCB must be modelled correctly
  - Correct SPICE models of switching elements
  - ESR/ESL of capacitances must be modelled correctly (→ e. g. with the Bode 100)

- Publication of the tool as soon as every bug is fixed

Conclusion

The critical path in any given power converter can be found.

The parasitic components can be simulated before the PCB is manufactured.

Especially in the high-frequency switching domain this evaluation comes in handy to shorten the PCB design process by reducing the design and testing iterations.

Contact

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