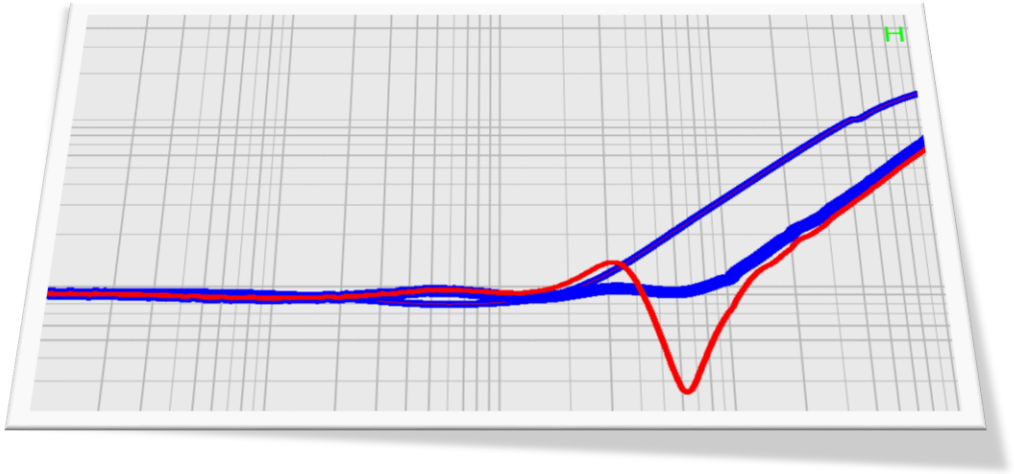


Flat Impedance in Voltage Regulator Modules

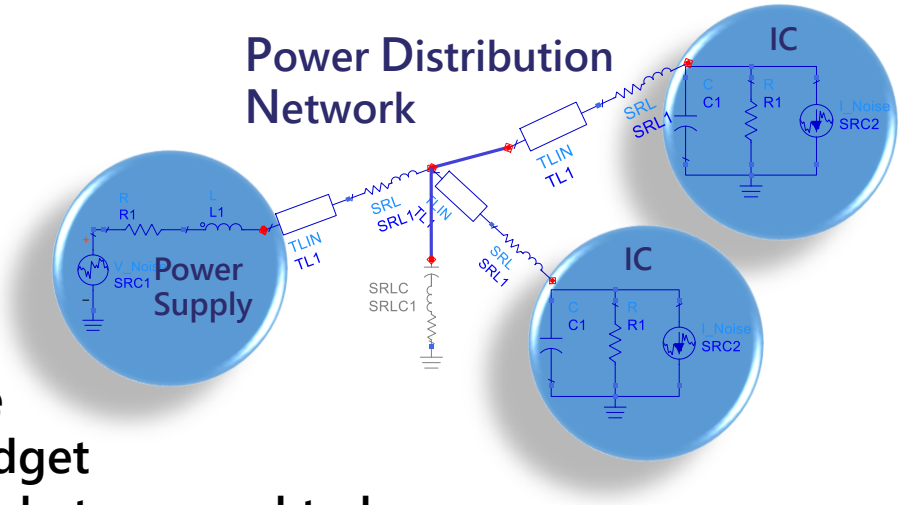
Why you need them and how to design them

Presented by Steve Sandler

OMICRON LAB

PICOTEST

Topics and Key Takeaways



Topics

- The <u>flatness</u> of the PDN impedance is critical to system performance
- The impedance magnitude is set as part of a power supply noise budget
- The data needed is often not published, but we can easily measure what we need to know
- Capacitor measurements (Touchstone/S1p) & co-simulation can expedite the process
- Demonstration of the process using a Picotest demo board as a case study

Key Takeaways

While counterintuitive, lower regulator impedance (better VRM regulation) can significantly <u>DEGRADE</u> system performance. Sometimes to the point that it cannot be corrected at the load.
As a rule, ceramic output capacitors lead to significantly increased system level noise.

Extras

- ADS Simulation Workspace available (Email me a request: Steve@picotest.com)
- The demo boards used are all commercially available if you want to try this process yourself
- There are lots of references related to this topic included at the end of this presentation

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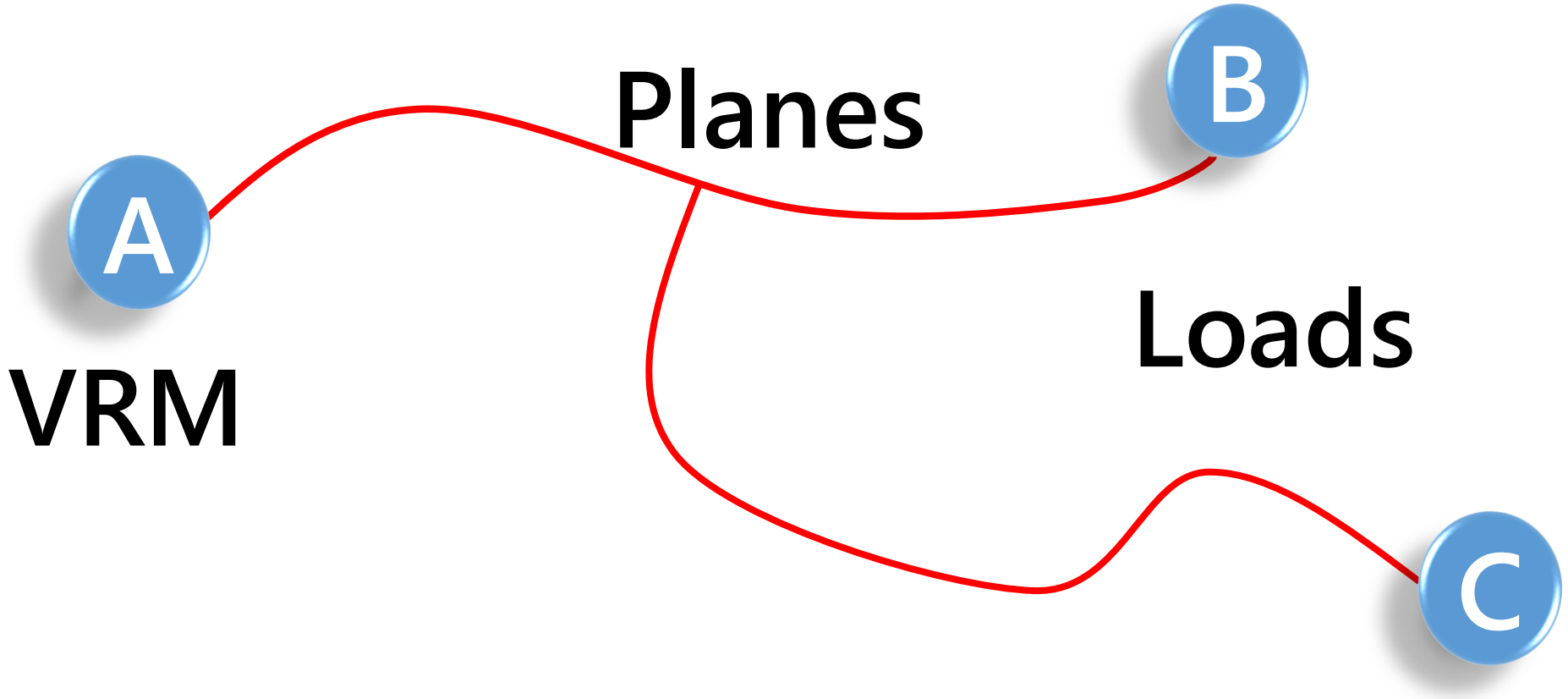
The A, B, Cs of the PDN



The role of the Power Distribution Network (PDN) is to deliver *appropriate* power from a voltage regulator module (VRM) to its associated loads. Focusing solely on the best VRM performance often results in poor performance at the loads.

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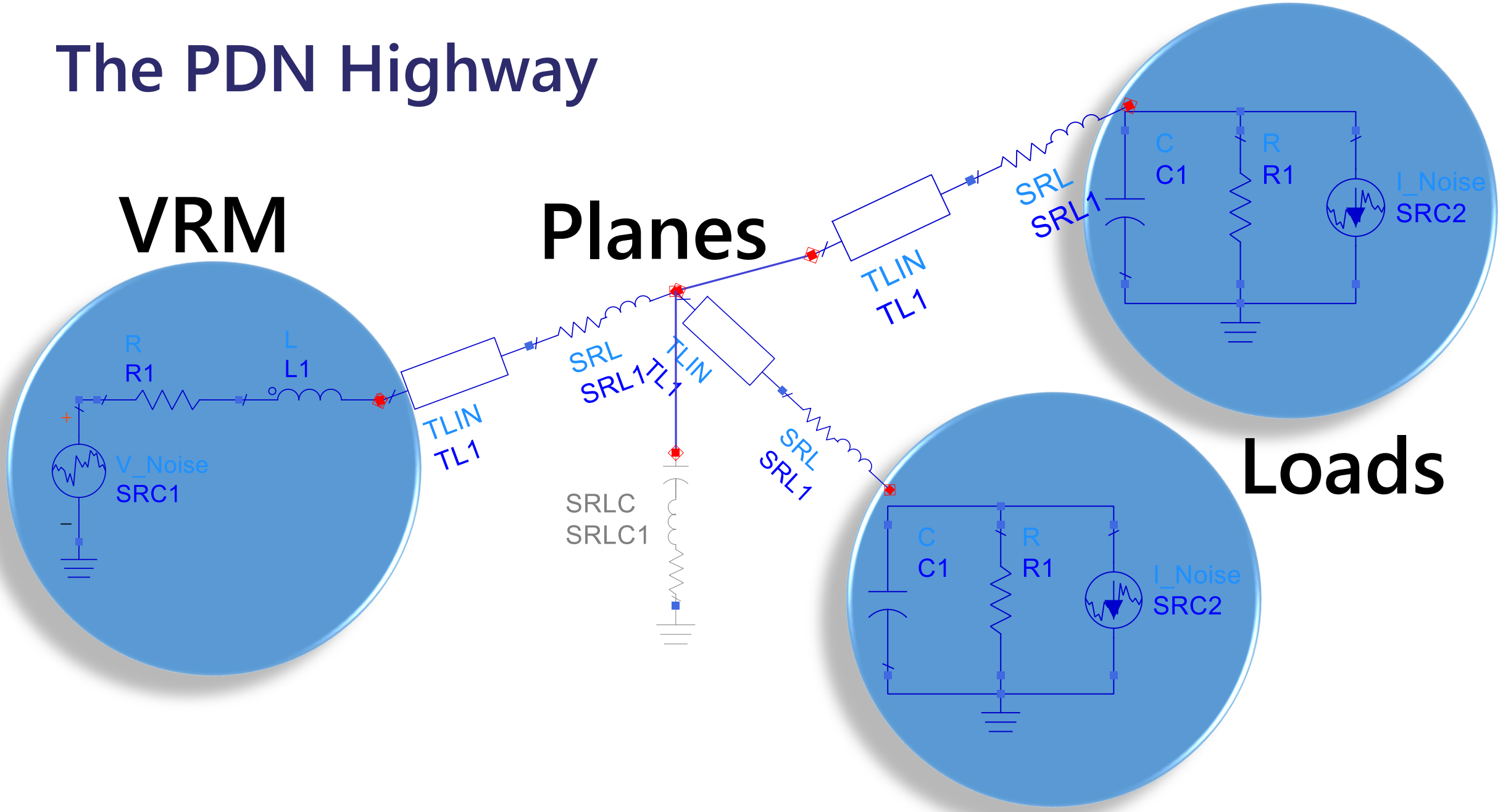
The PDN Highway



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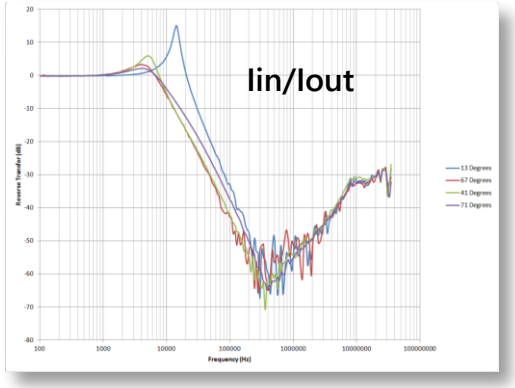
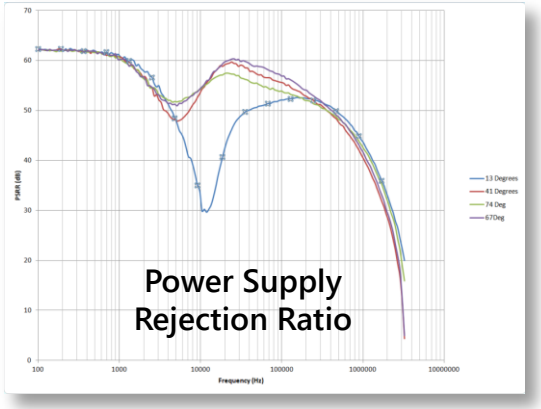
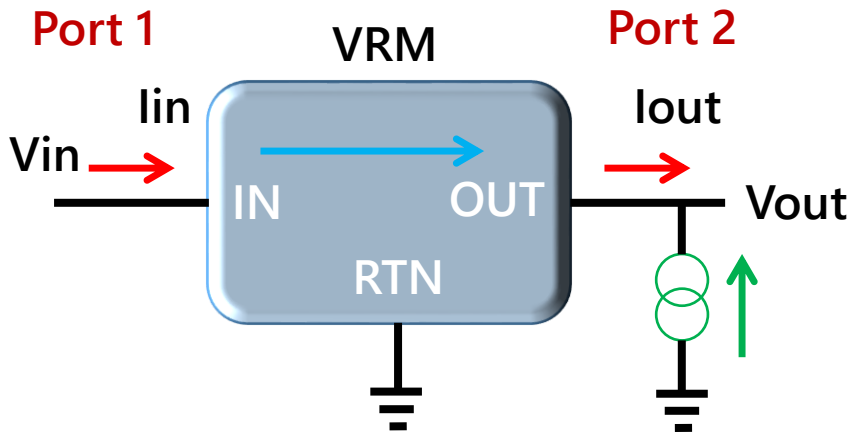
Resonances Degrade Performance

Reverse Transfer - (S12)



PSRR - (S21)

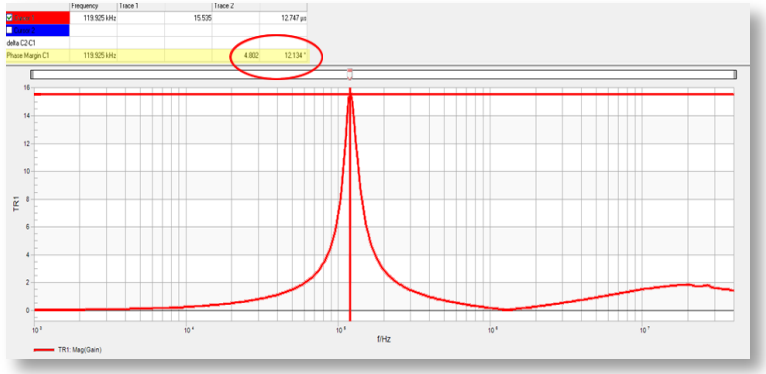




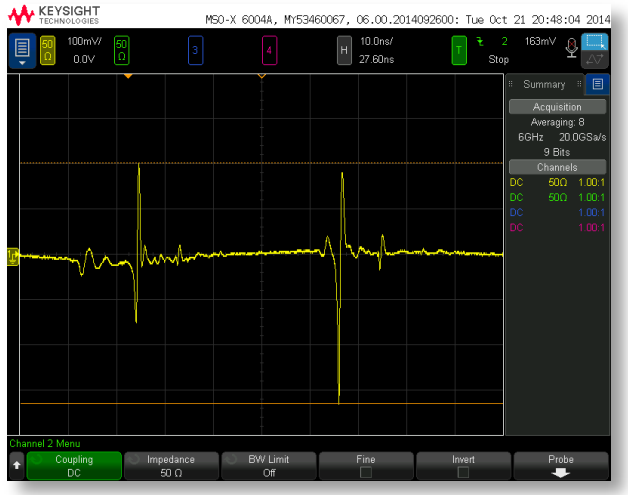
Input Impedance - (S11)

Input impedance can be NEGATIVE!

Output Impedance - (S22)



Output Noise/Spikes



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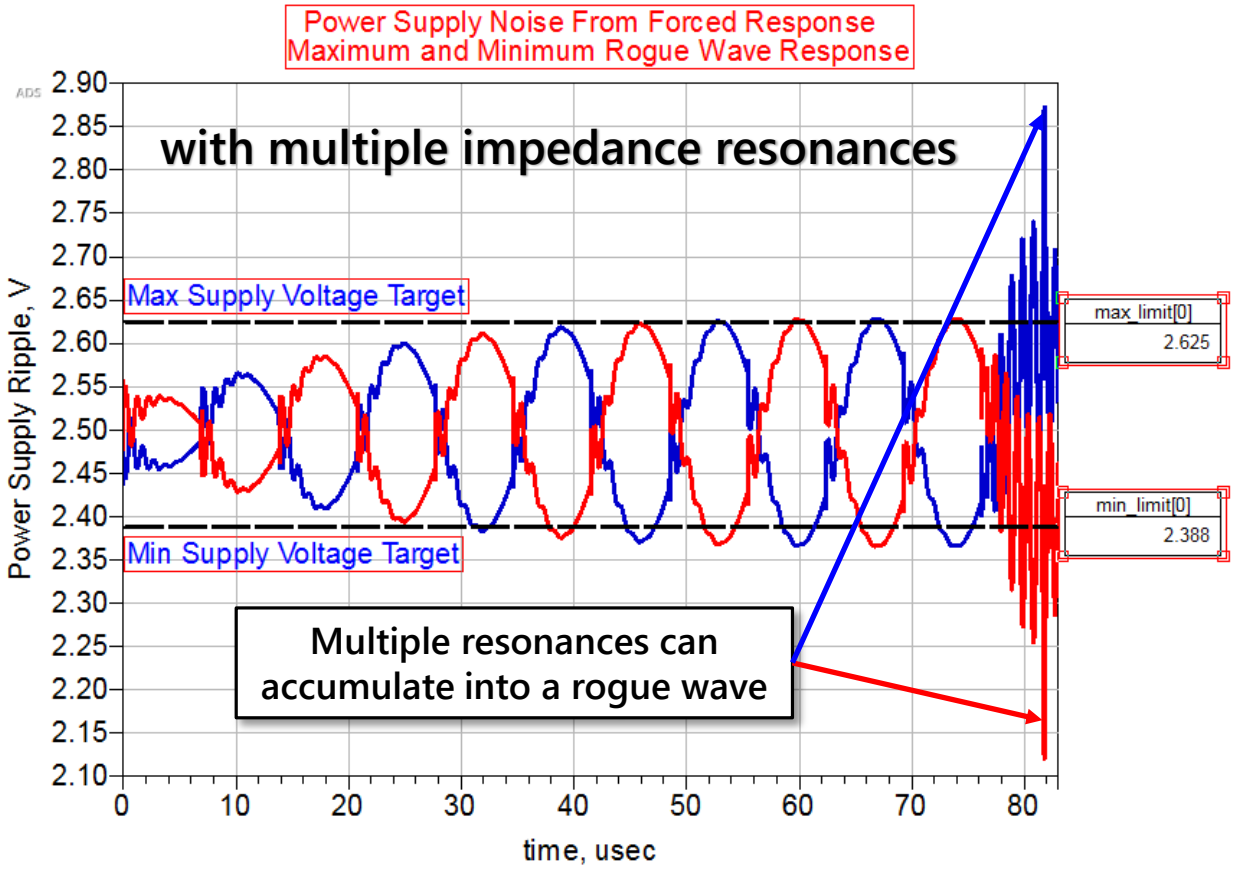
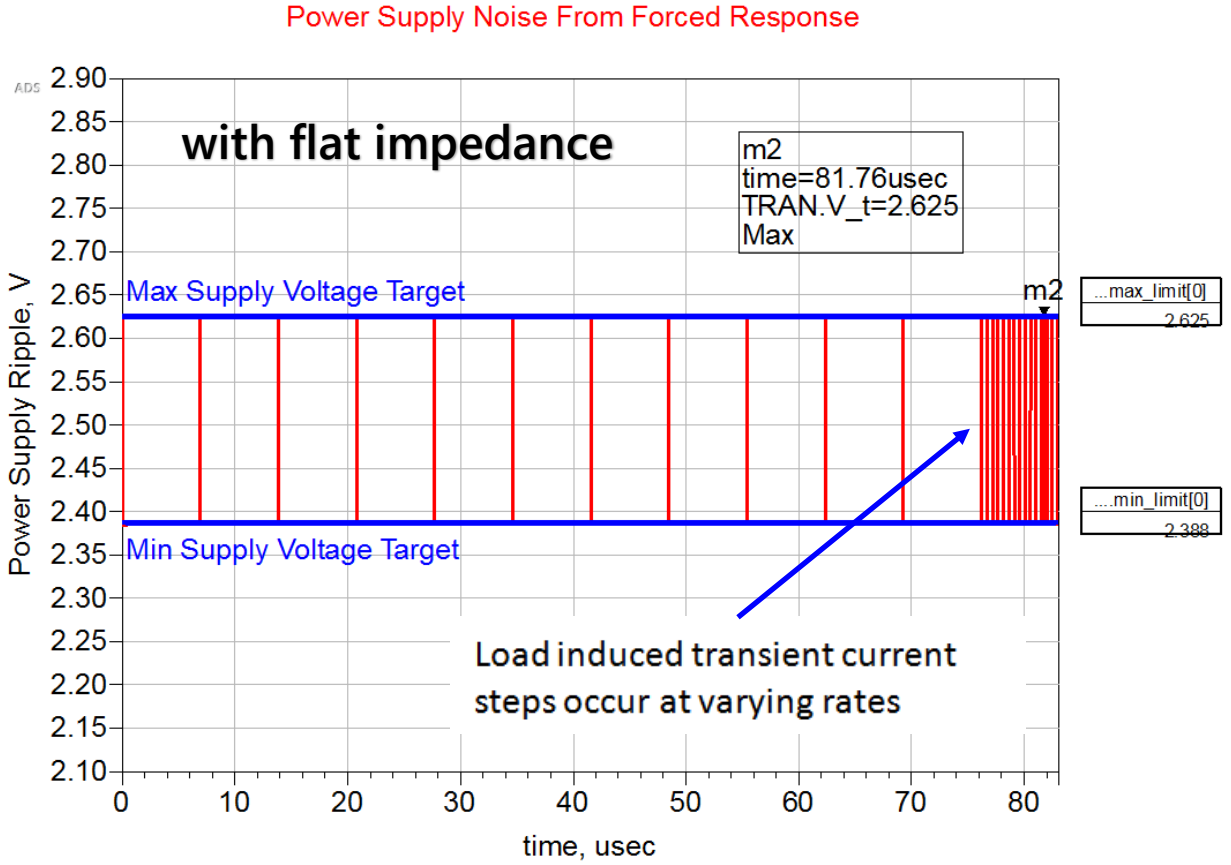
More Resonances Yield Even More Noise

The same transient load step stimulus…





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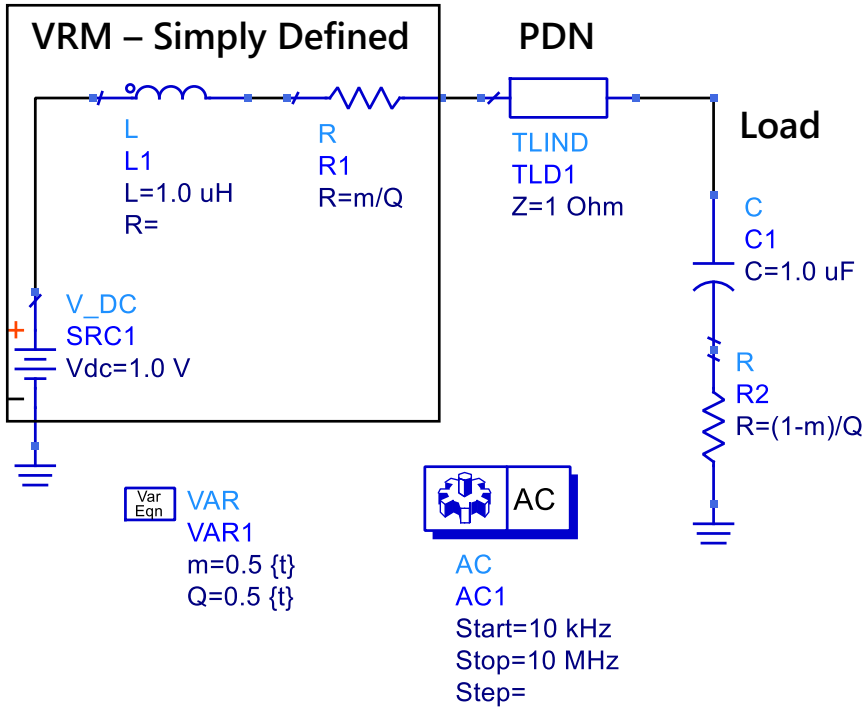
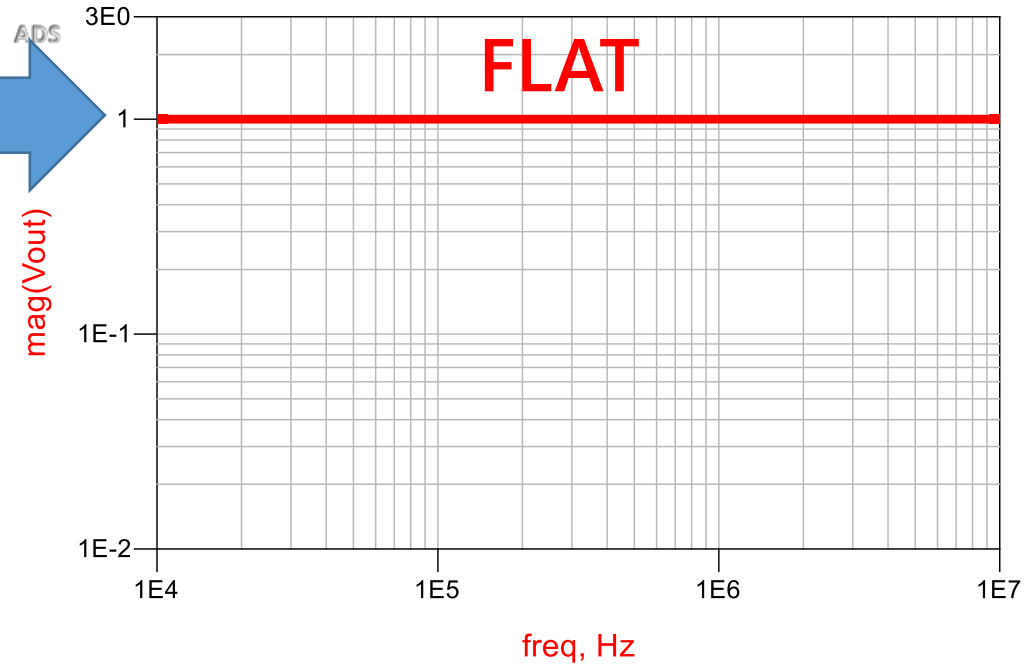
Source = Interconnect = Load



$$Z_o = \sqrt{\frac{L}{C}} = 1$$

$$R1 = R2 = Zo$$

$$Q = \frac{Z_o}{R1 + R2}$$



What happens when they DON'T match? and what does that have to do with PI?

This is why RF instruments are 50Ω source, 50Ω cable and 50Ω load

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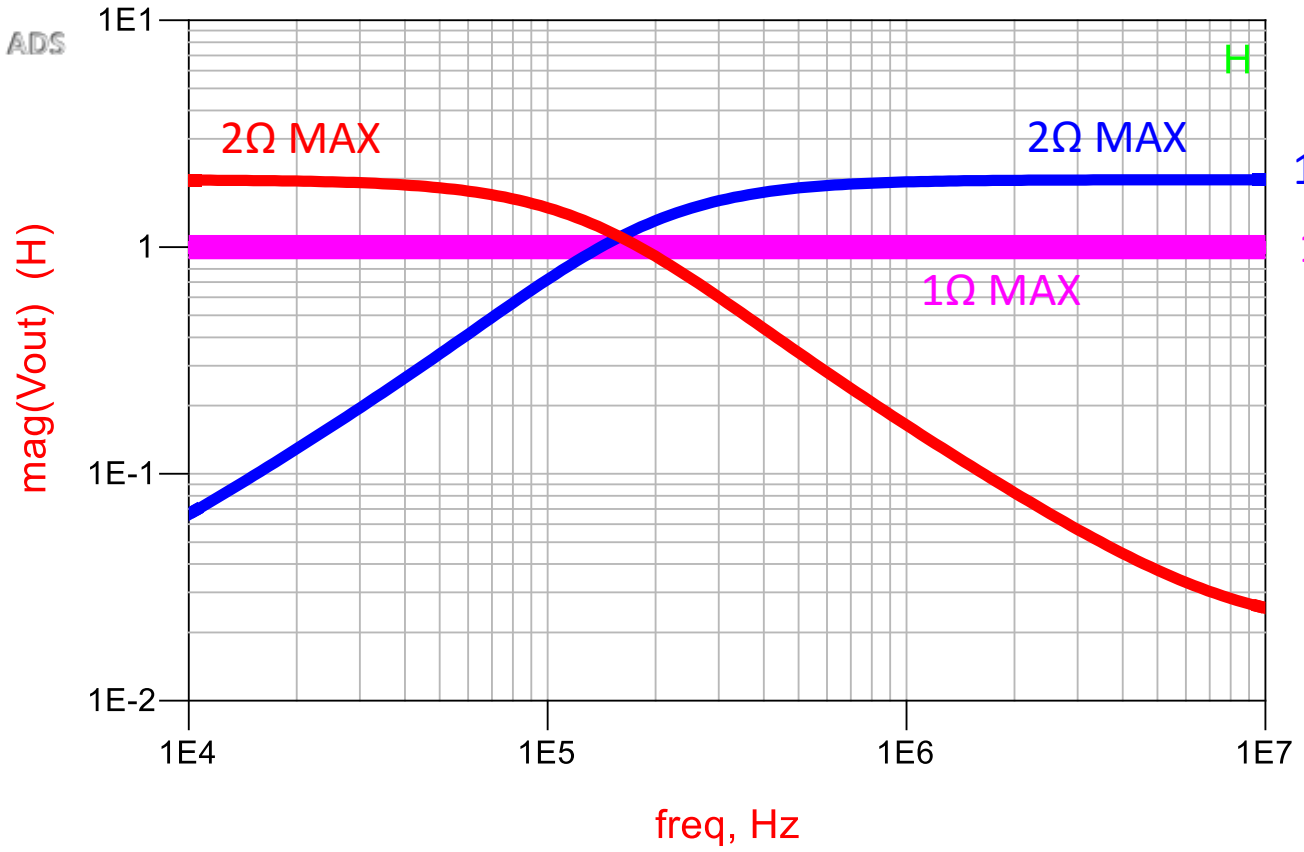
When They Don’t Match



1.99Ω Source and .01Ω LOAD

1Ω Source and 1Ω LOAD

1.99Ω Source and .01Ω LOAD

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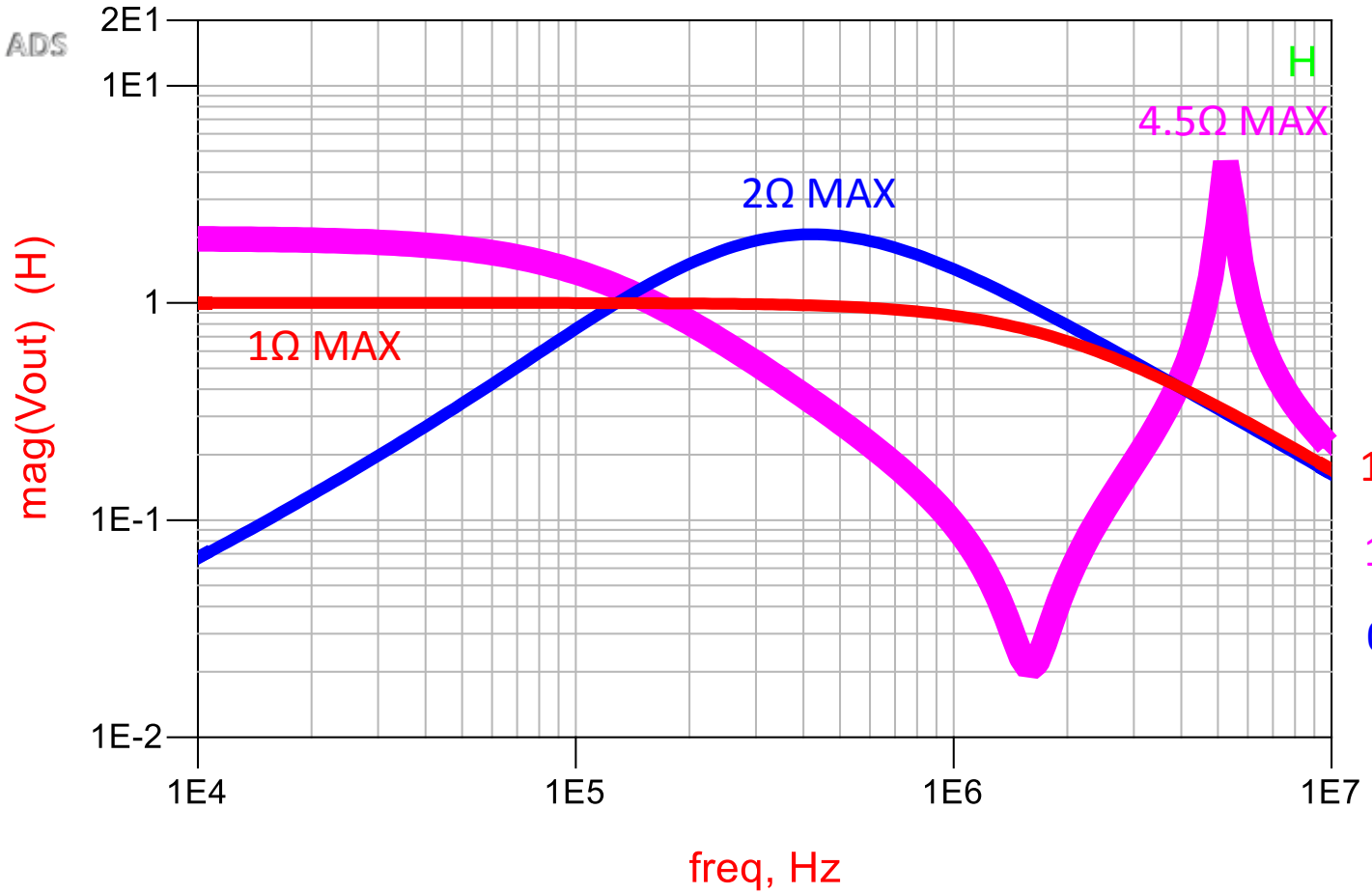
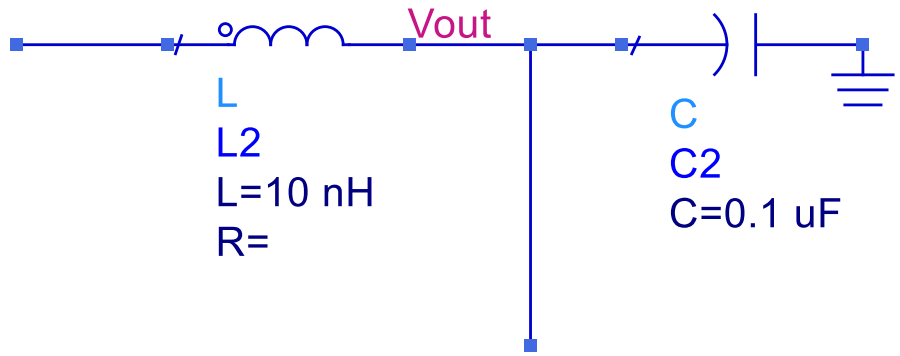
Adding Parasitic Inductance and Decoupling





1Ω Source and 1Ω LOAD

1.99Ω Source and 0.01Ω LOAD

0.01Ω Source and 1.99Ω LOAD

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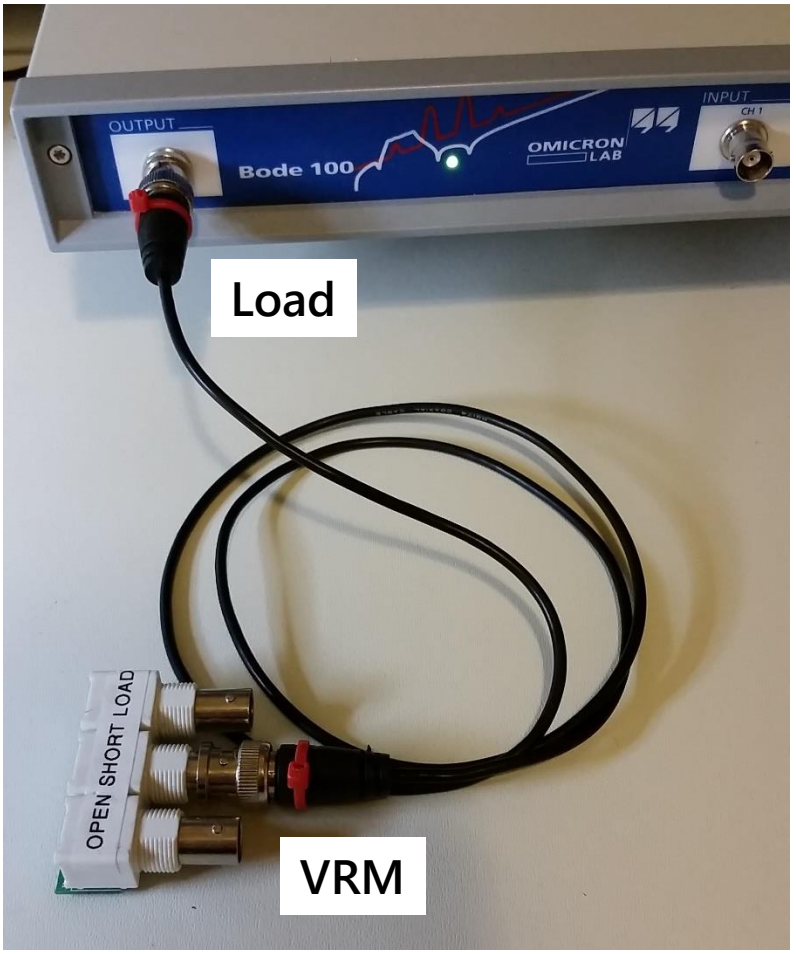
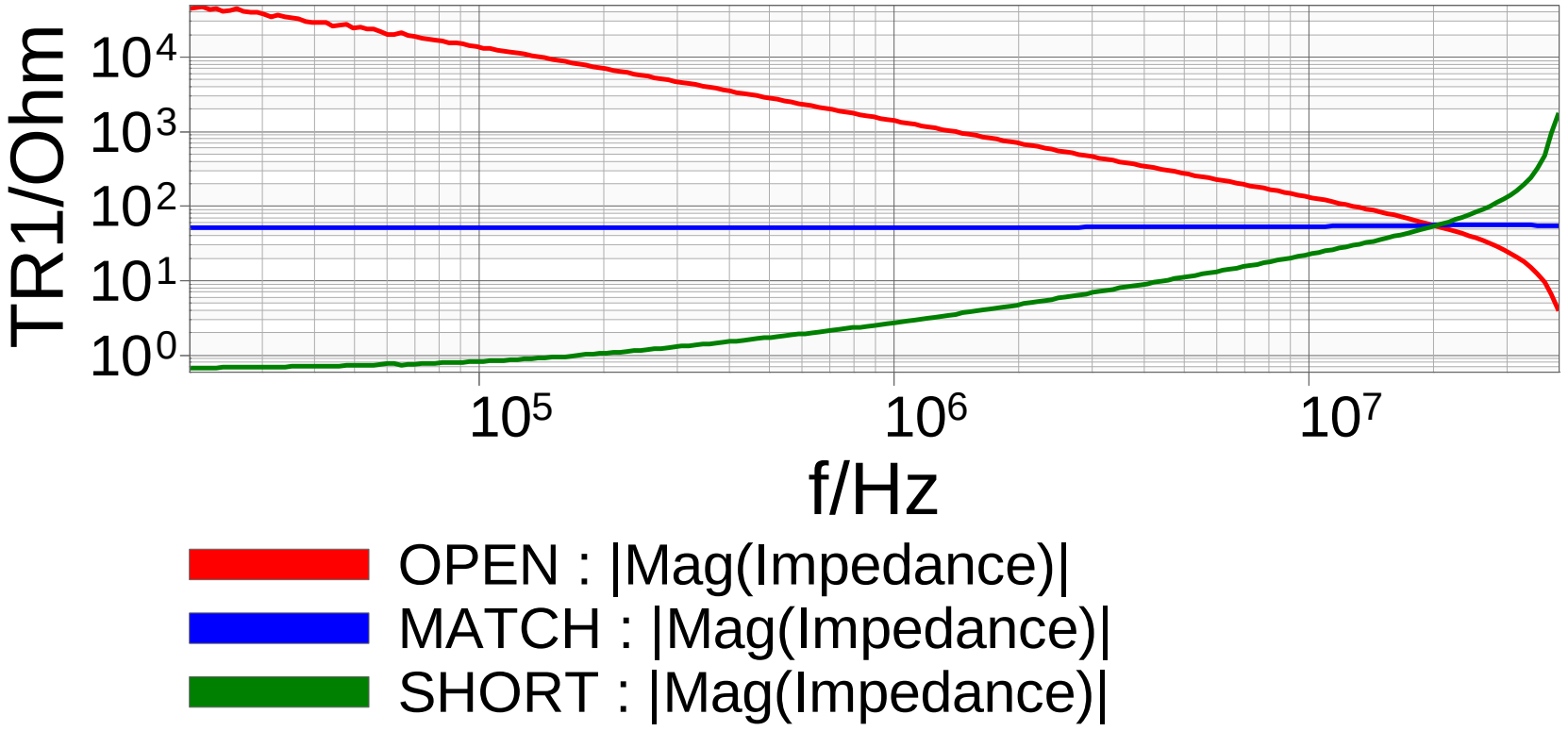
Really Simple Demonstration



1 meter 50Ω COAX cable



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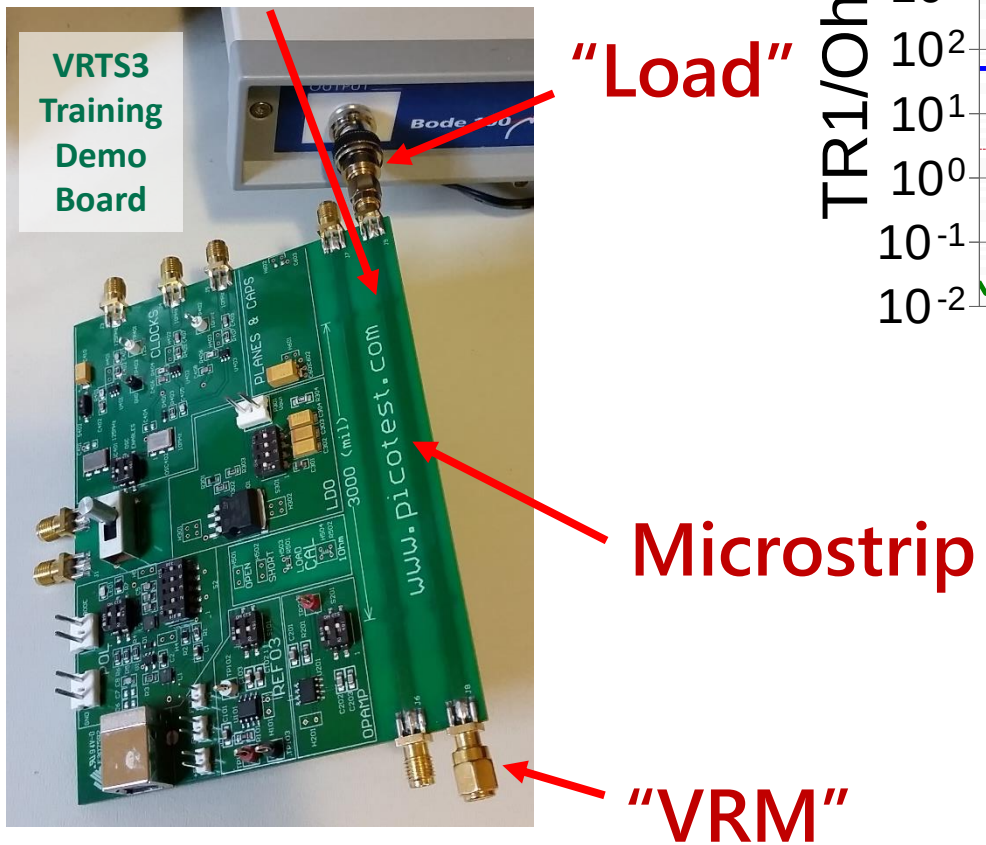
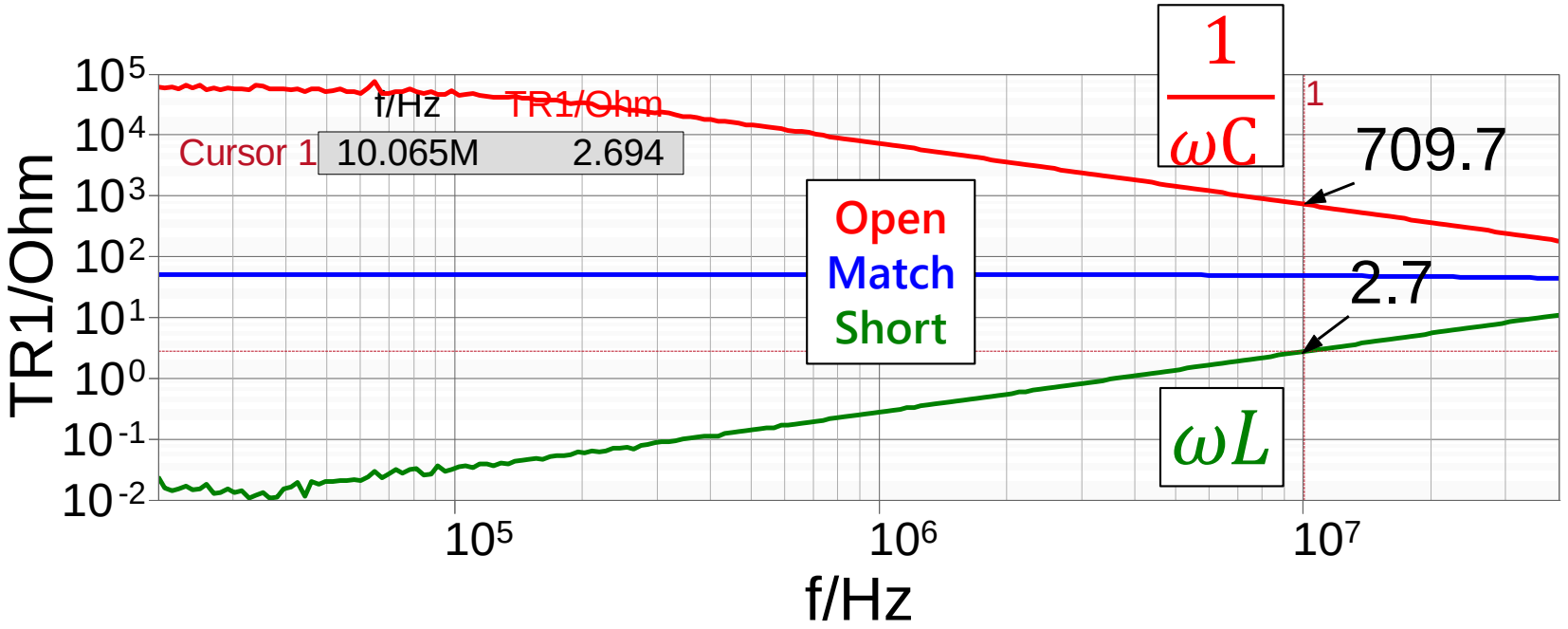
A Simple ADS-PCB Demonstration



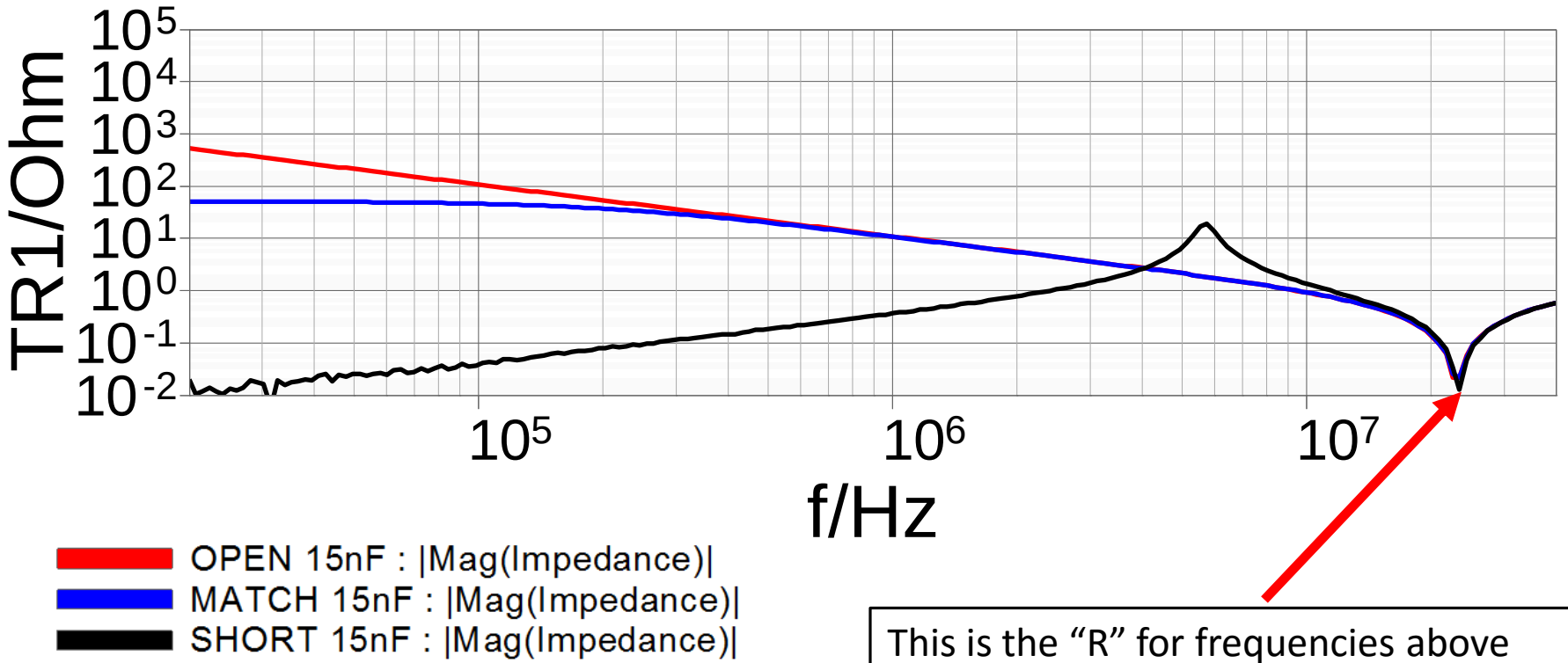


Quick Tip

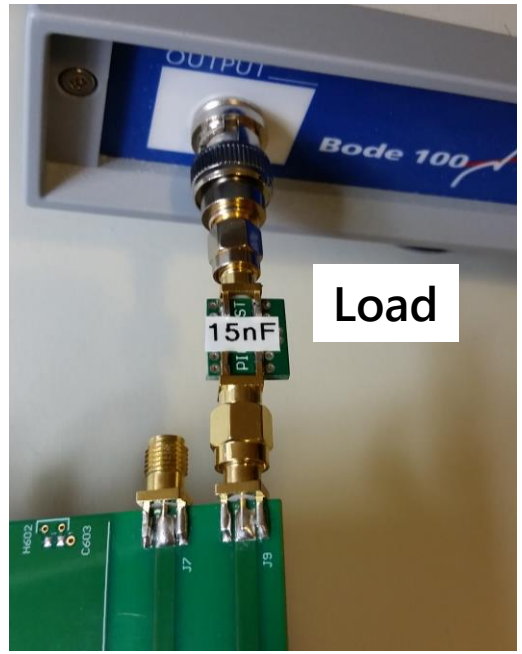
$$Z_o = \sqrt{709.7 * 2.7}\sqrt{\frac{1}{\omega C}\cdot \omega L} = \sqrt{\frac{L}{C}} = 43.8\Omega$$

PICOTEST

Adding Decoupling Capacitor at the Load



This is the “R” for frequencies above 21MHz. The “L” above 21MHz is the ESL of the decoupling capacitor PLUS PCB and interconnect inductance

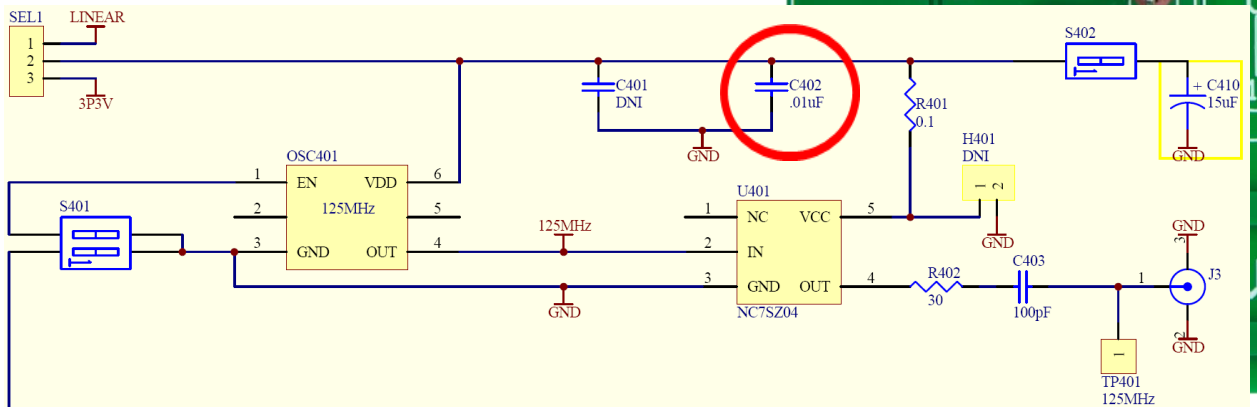


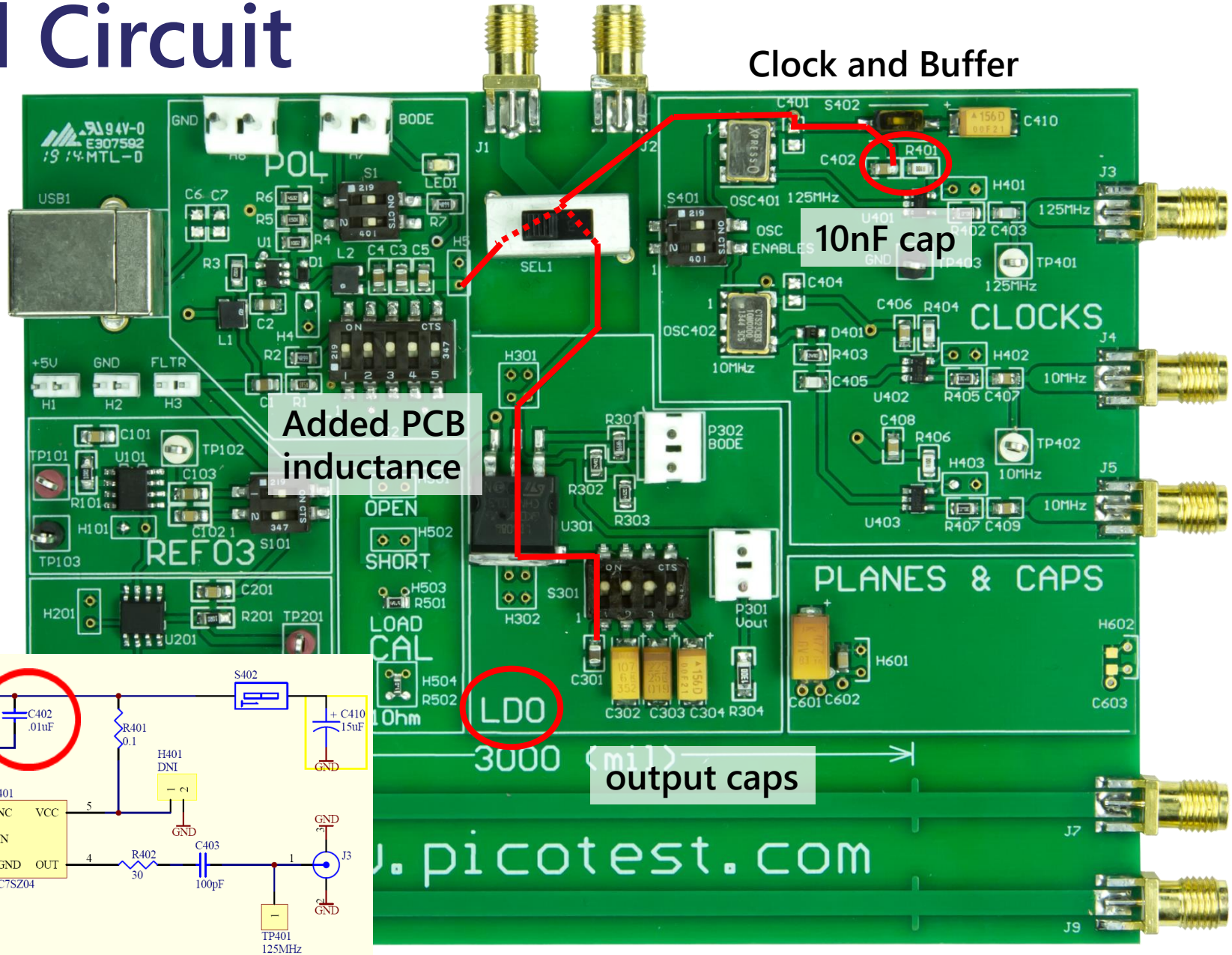
PICOTEST

An Actual Circuit

The Picotest VRTS3 training board includes an example with a VRM connected to a clock.

Several output capacitor choices are available to highlight the impedance issues





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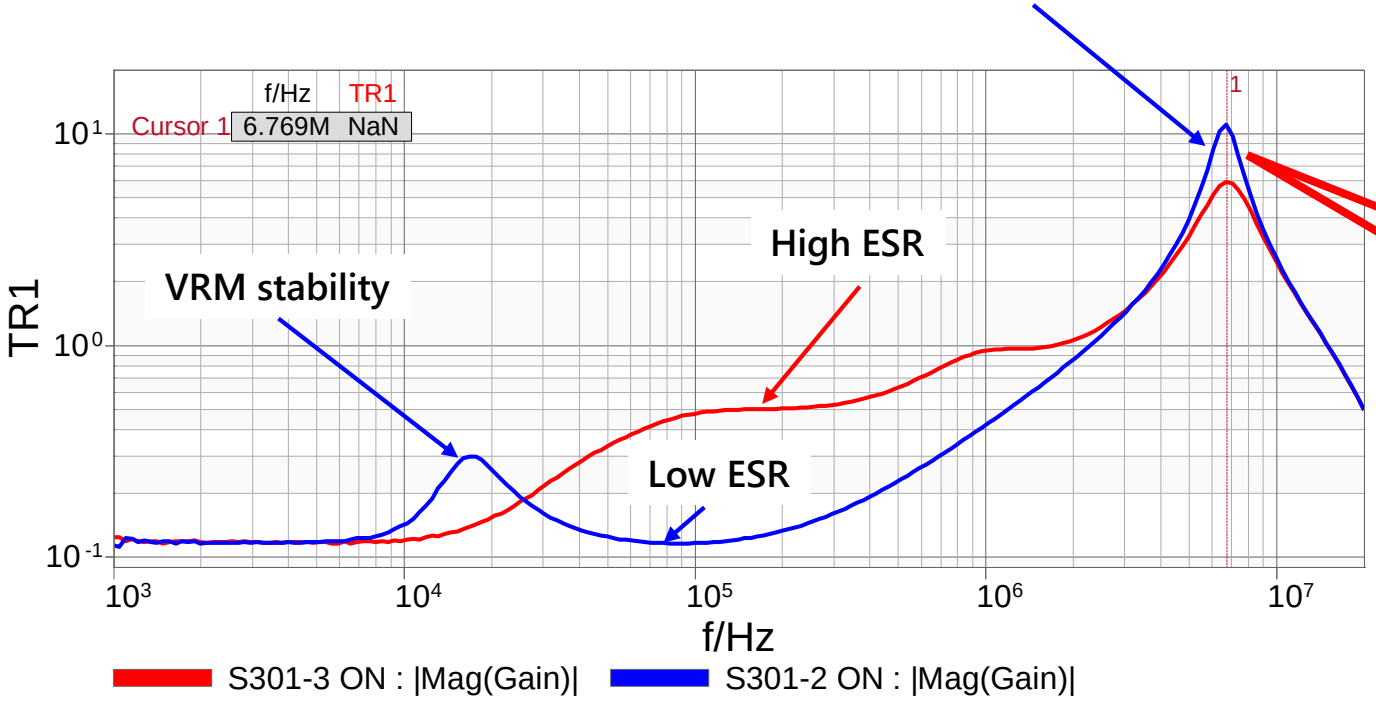
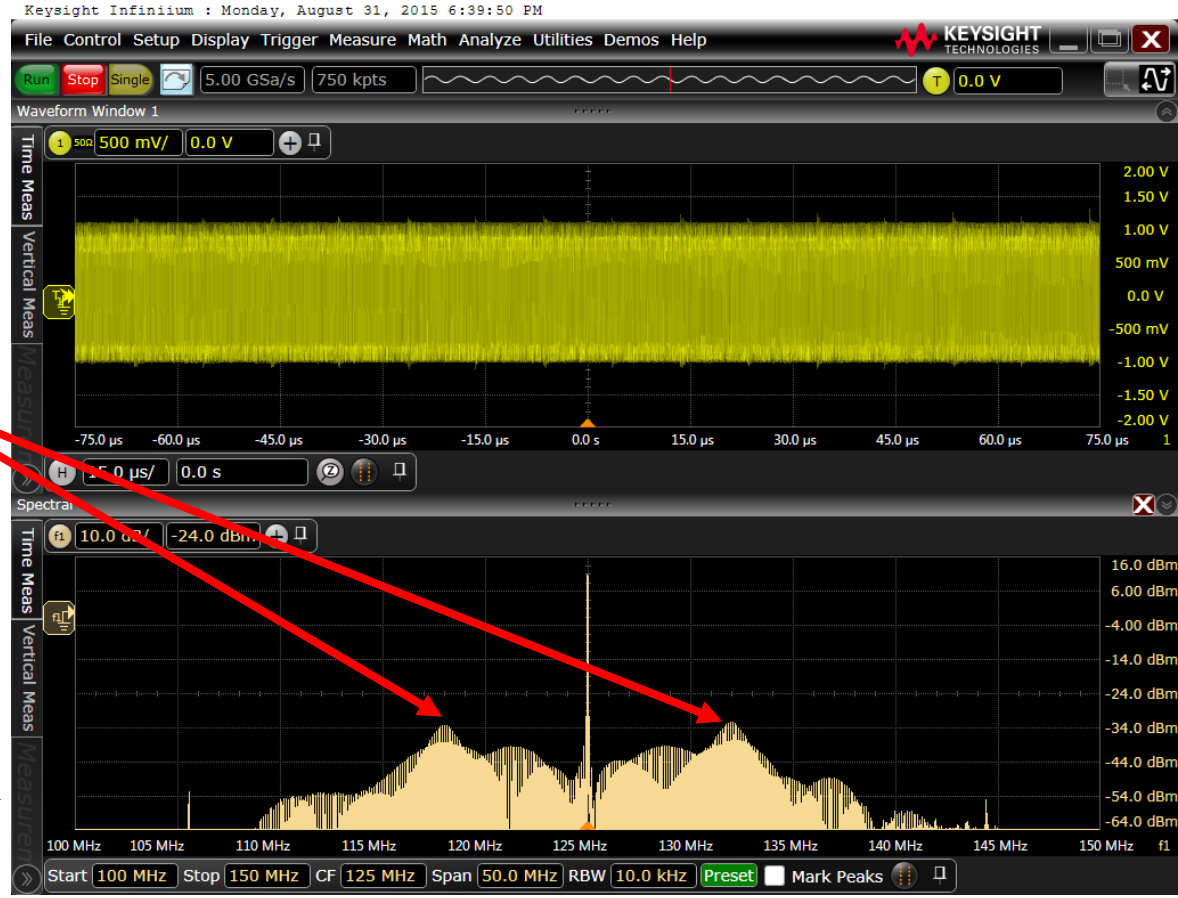
Focus on the Load NOT the VRM

In this example, a 7MHz resonance in the PDN shows up as clock jitter.

Reducing the VRM impedance increases jitter at 7MHz.

Trace resonance at 10nF cap





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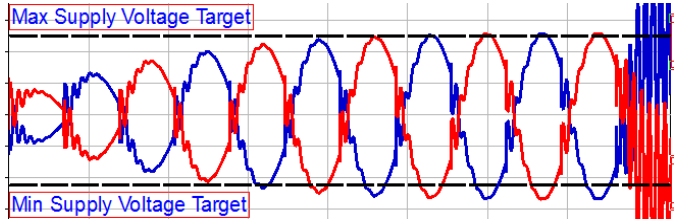
Four Step Design Process to Flat Impedance

1. Create a noise budget
2. Set impedance level using noise (rail voltage deviation) budget
3. Set the VRM output resistance equal to the desired impedance level (tolerances!)
4. At each node, cancel excess inductance with a capacitor. Capacitor ESR must be equal to the desired impedance

Noise Budget = DC regulation + Ripple + IR drop+ Step load excursion + Noise



$$C = \frac{L}{Z_{desired}^2}$$

Quick Tips

- Minimizing inductance reduces capacitor size
  - Higher bandwidth, locate regulator closer to the load, wide planes thinner PCB dielectric
- There's a lot of variation in voltage regulators, choose wisely – lower output inductance wins
- Ferrite beads are VERY inductive and as a rule should be avoided like the plague
- Linear regulator inductance varies inversely with load current - assess at the lowest operating current

PICOTEST

Creating the Noise Budget

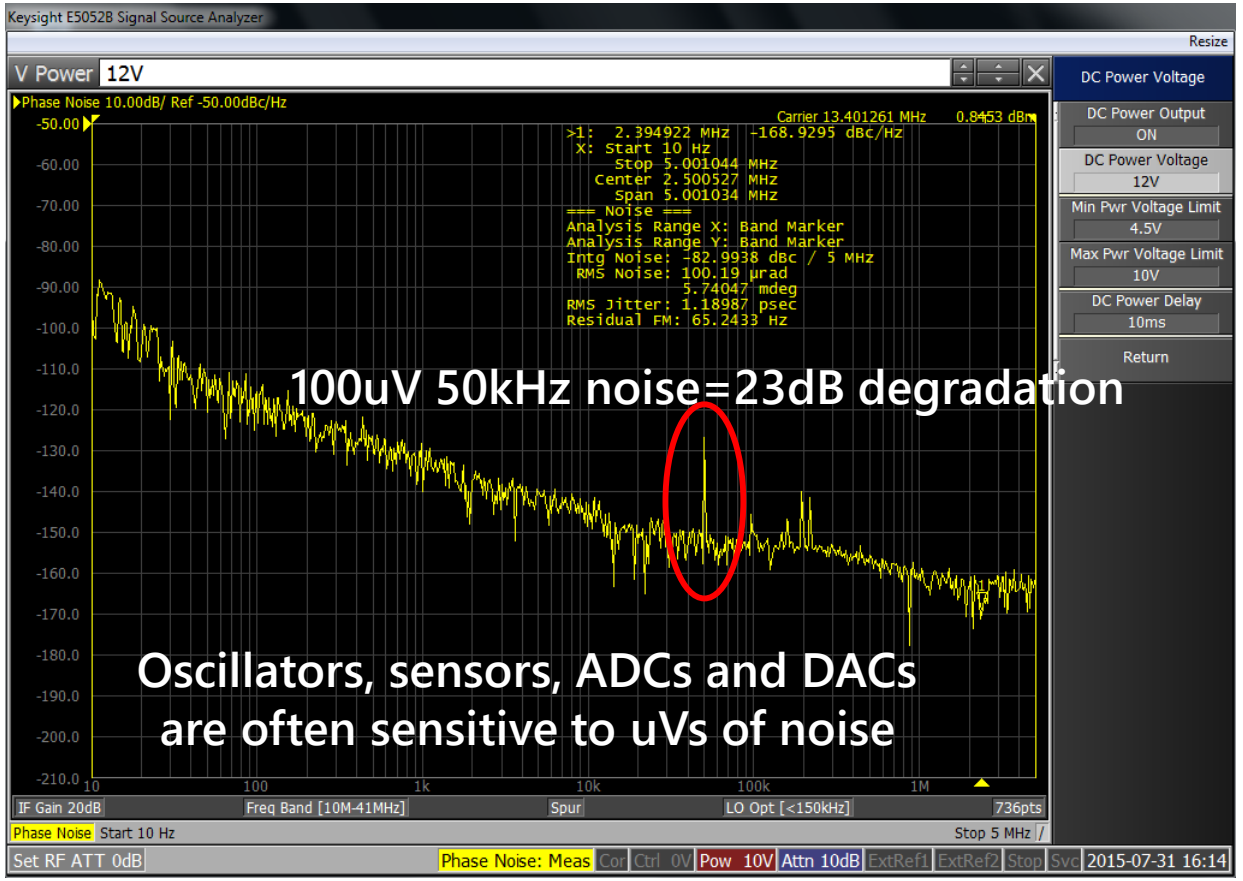
There are many sources of noise!

$$\Delta I_f \cdot \frac{4}{\pi} \sum_{f=0}^{\infty} Z_f \approx \Delta V - \sum_{n=0}^{\infty} V_n$$

The total noise budget for this FPGA is 30mVpk

Table 1. Example V_{CC} Core Voltage Power Supply Operating Conditions (1)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply (C1, C2, and 12 speed grades)	—	0.87	0.90	0.93	V
	Core voltage and periphery circuitry power supplier (C2L, C3, C4, I2L, 13, 13L, and 14 speed grades)	—	0.82	0.85	0.88	V



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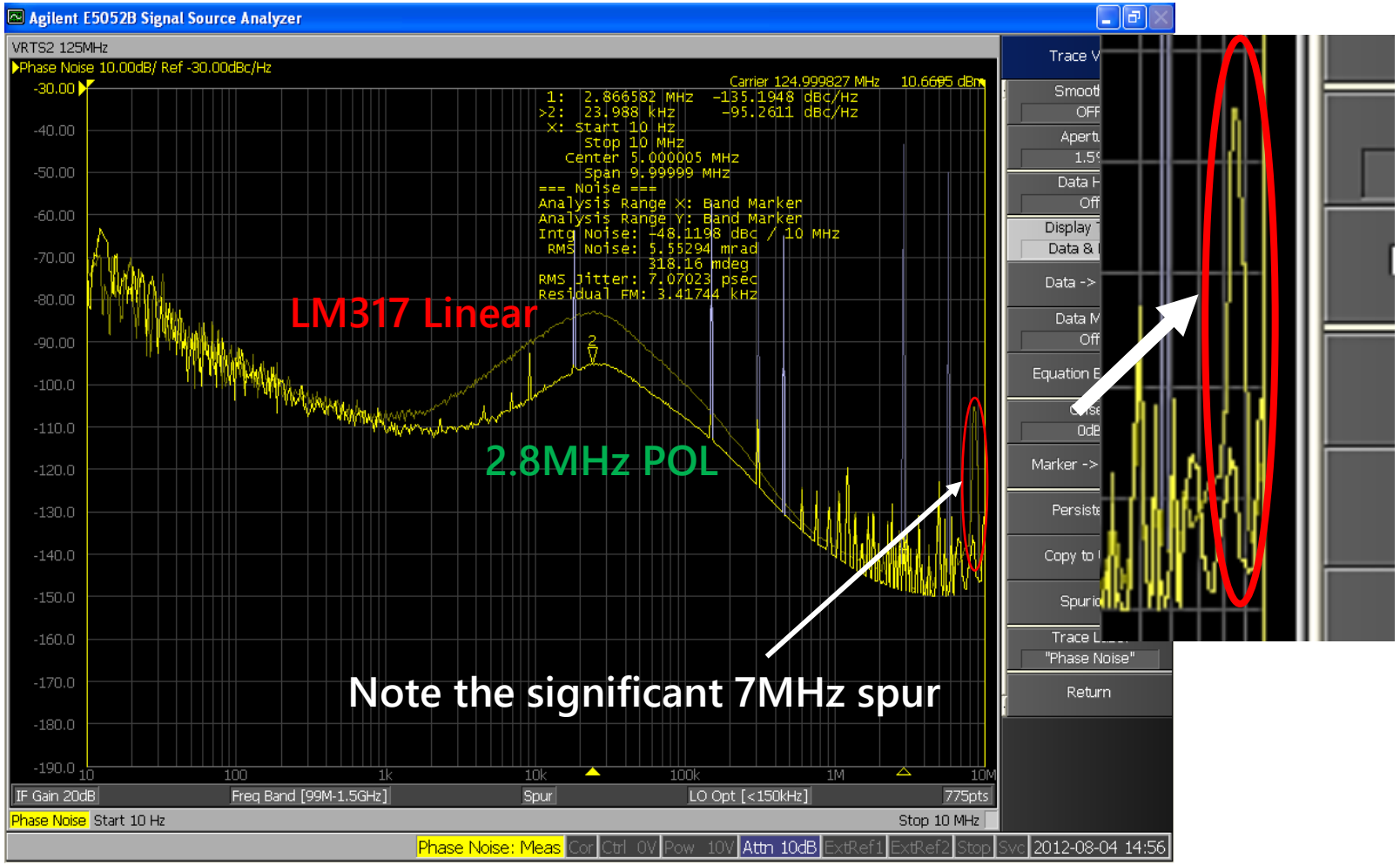
Target Z is NOT Related to Power Level



Set it wisely

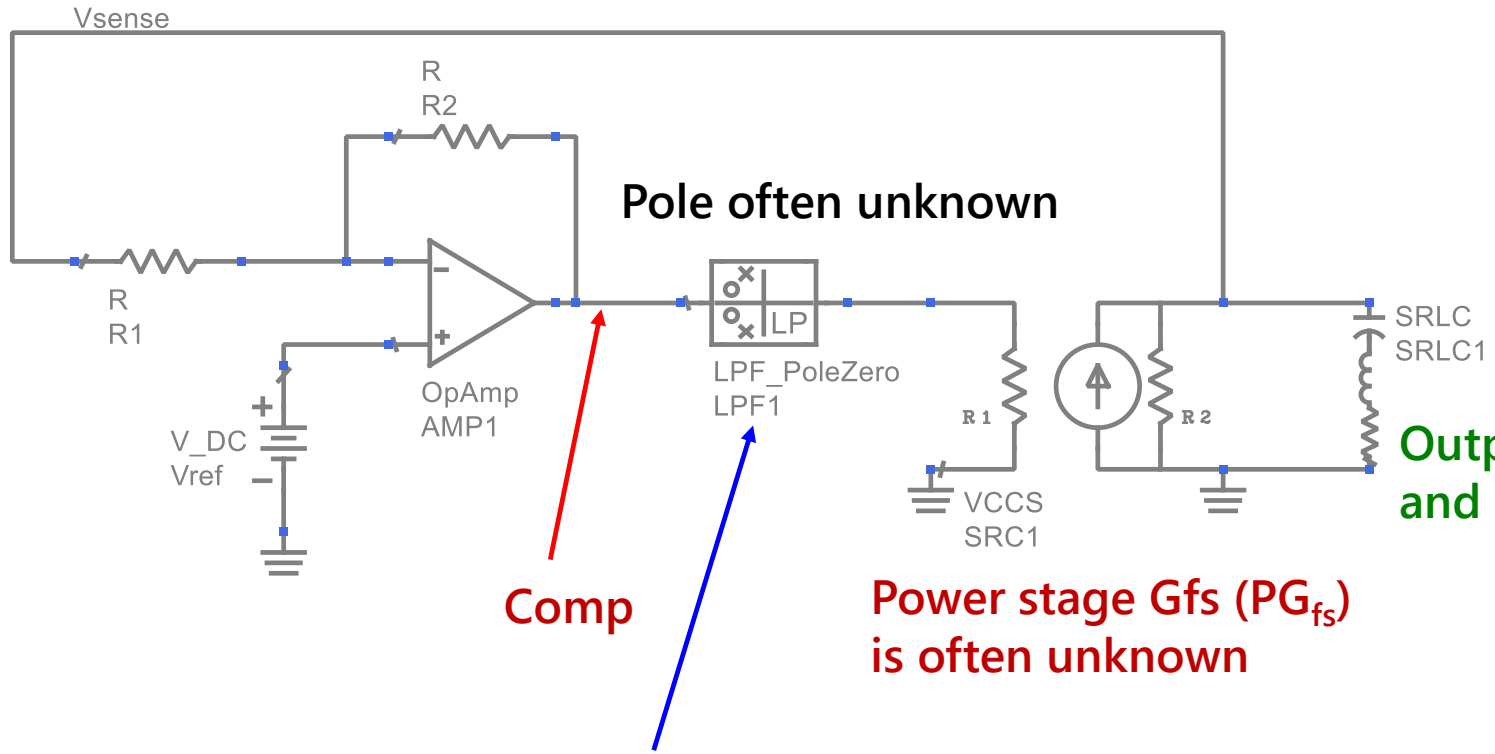
Determine the tolerable voltage deviation level (all sources) at the load

This level is related to the noise budget and helps establish the impedance and filter or local regulator requirements

PICOTEST

Designing the Flat Impedance VRM

Choose a controller with an external compensation pin



Pole often unknown

Comp

Power stage Gfs (PG_{fs}) is often unknown

Internal pole and slope compensation set effective inductance

Output capacitance and ESR are critical

Using a current mode switching VRM allows Rout to be easily set by controlling the DC gain

Not easy to control DC resistance in an LDO series resistor is often required

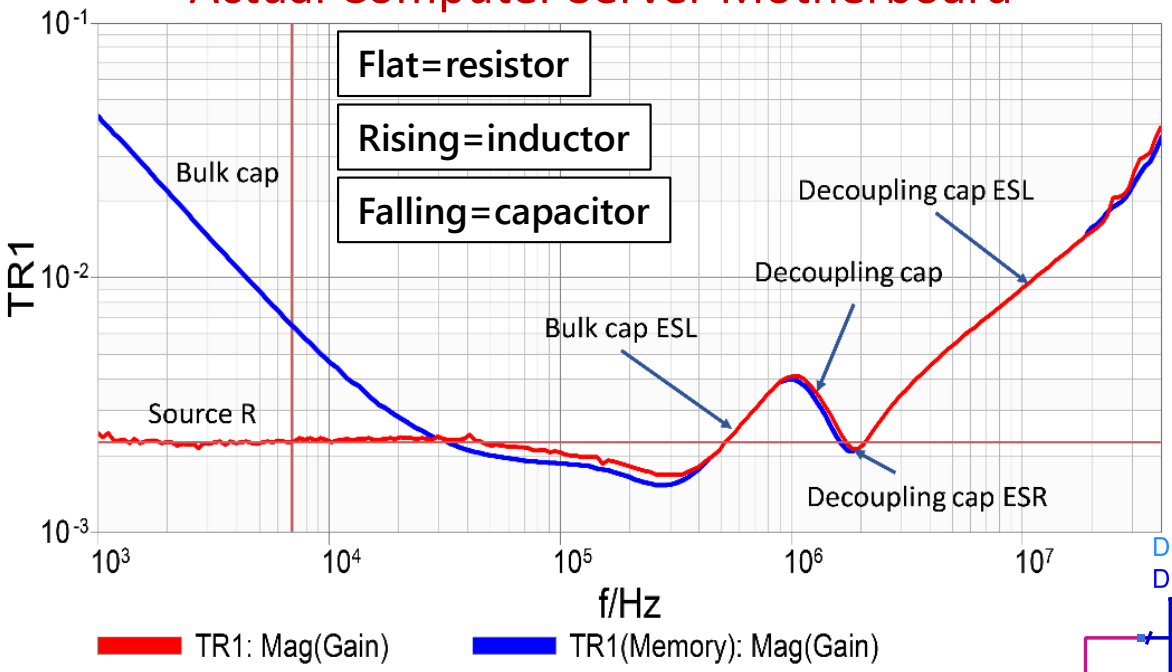
R1, R2 and PG_{fs} set Rout

$$R_{out} = \frac{R1}{R2 \cdot PG_{fs}}$$

PICOTEST

Reading the Impedance Measurement

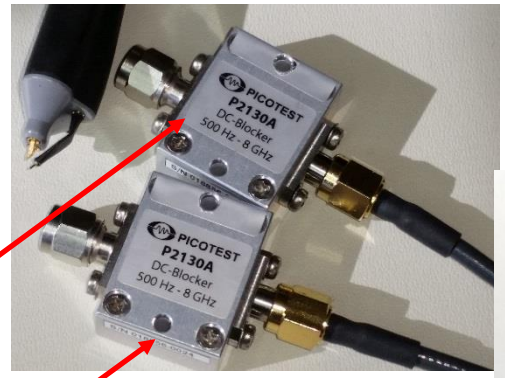
Actual Computer Server Motherboard



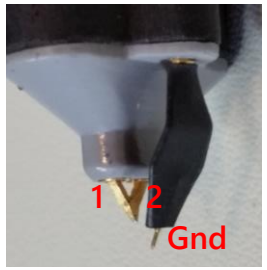
In some cases, a 2−port probe can be used, simplifying the connections and getting into small spaces

J2130A or P2130A

2-Port Probe

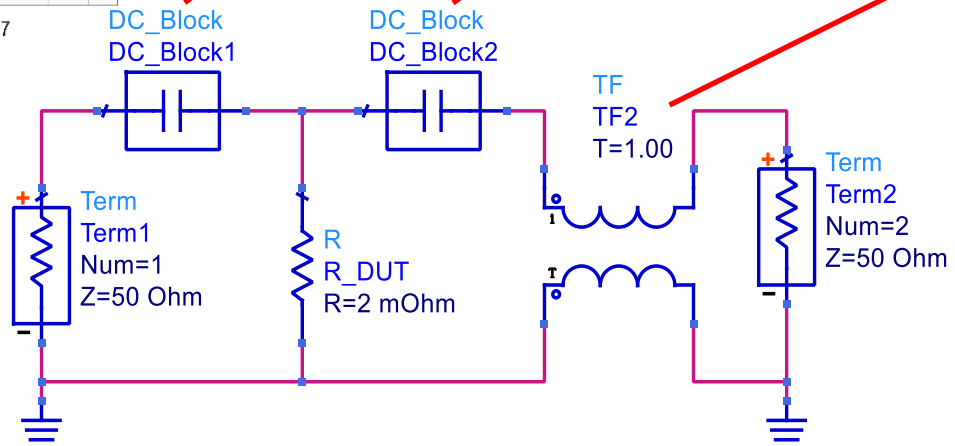


DC Blockers



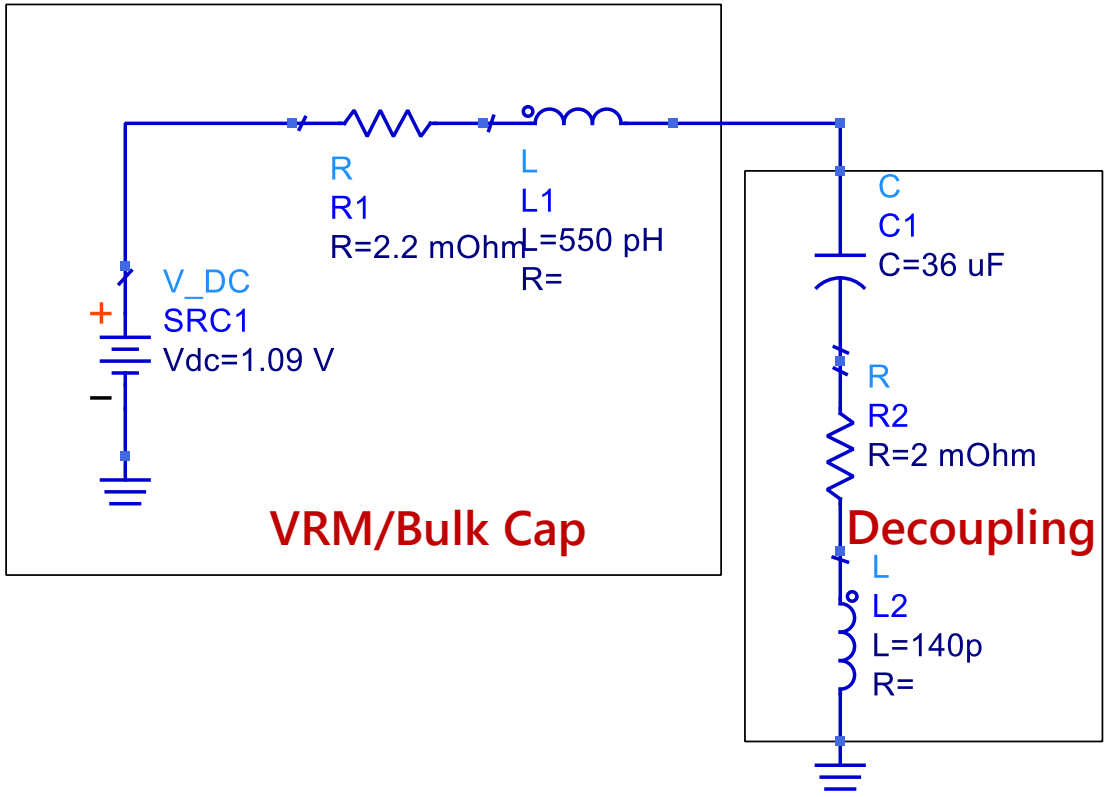
J2102A

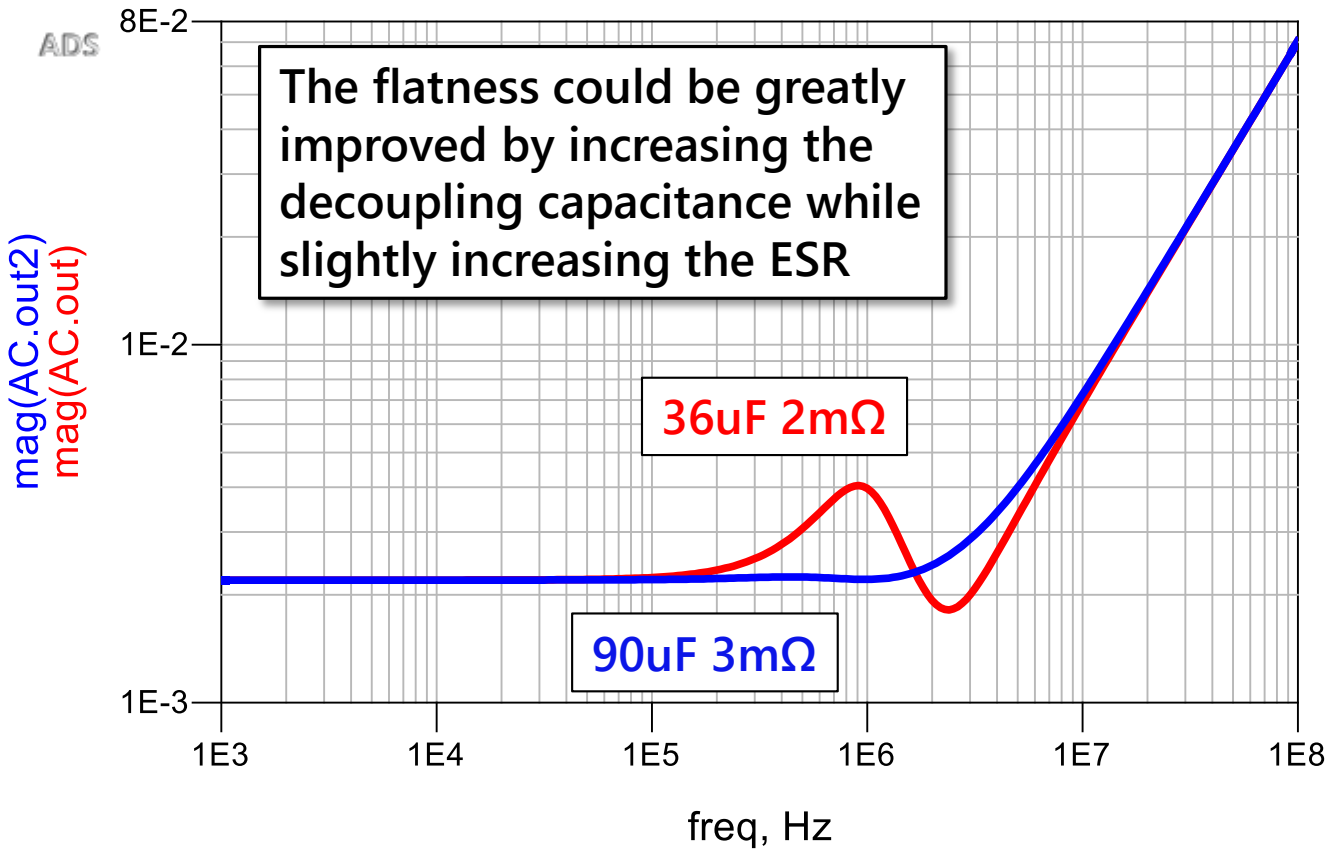
Common Mode Coaxial Transformer -- Ground Loops



PICOTEST

And Reconstructing It For Simulation



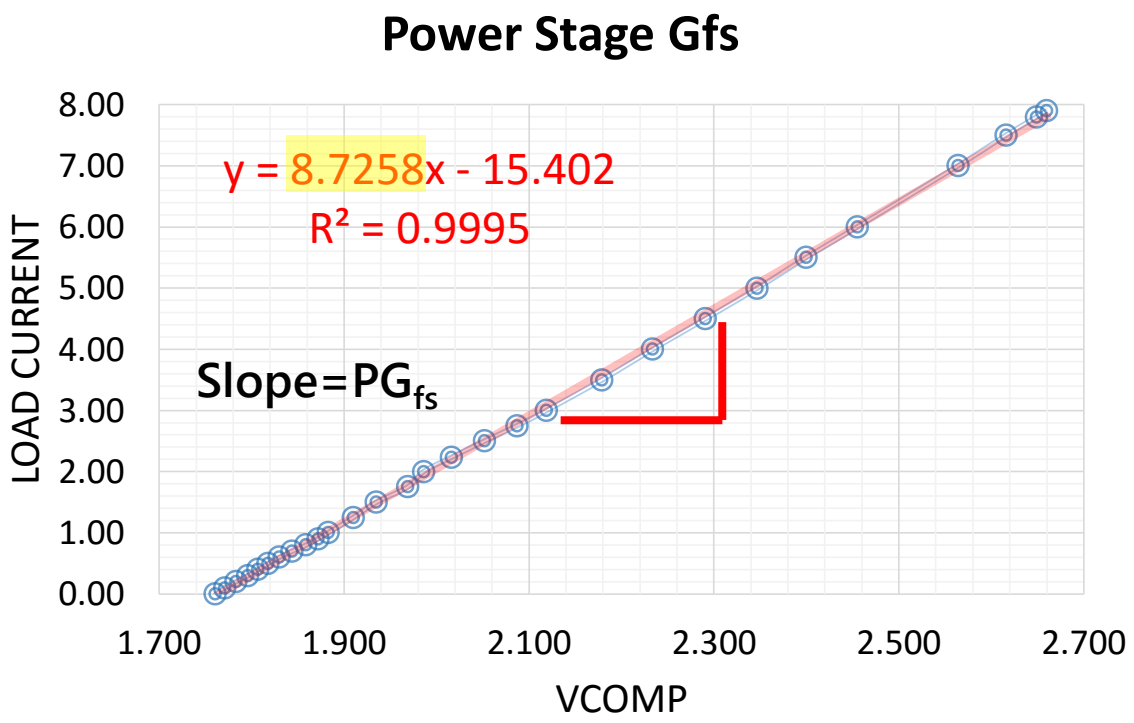


PICOTEST

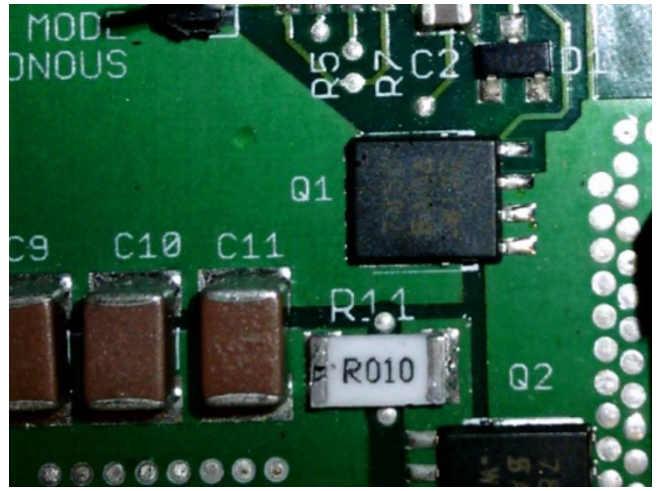
Determining Power Stage Transconductance

Vcomp (V)	Iout (A)
1.761	0.00
1.771	0.10
1.783	0.20
1.796	0.30
1.807	0.40
1.818	0.50
1.830	0.60
1.844	0.70
1.859	0.80
1.872	0.90
1.883	1.00
1.910	1.25
1.935	1.50
1.969	1.75
1.986	2.00
2.016	2.24
2.052	2.50
2.087	2.75
2.119	3.00
2.179	3.50
2.234	4.00
2.291	4.50
2.347	5.00
2.400	5.50
2.455	6.00
2.564	7.00
2.616	7.50
2.649	7.80
2.660	7.90

Measurements are often surprising. Using a 10mΩ resistor should result in PGfs of 10 and it does not ….



LM25116 Evaluation Board



PG_{fs} can also be computed from an Rout measurement

$$PG_{fs} = \frac{R1}{R2 \cdot R_{out}}$$

PICOTEST

Choosing the Output Capacitor

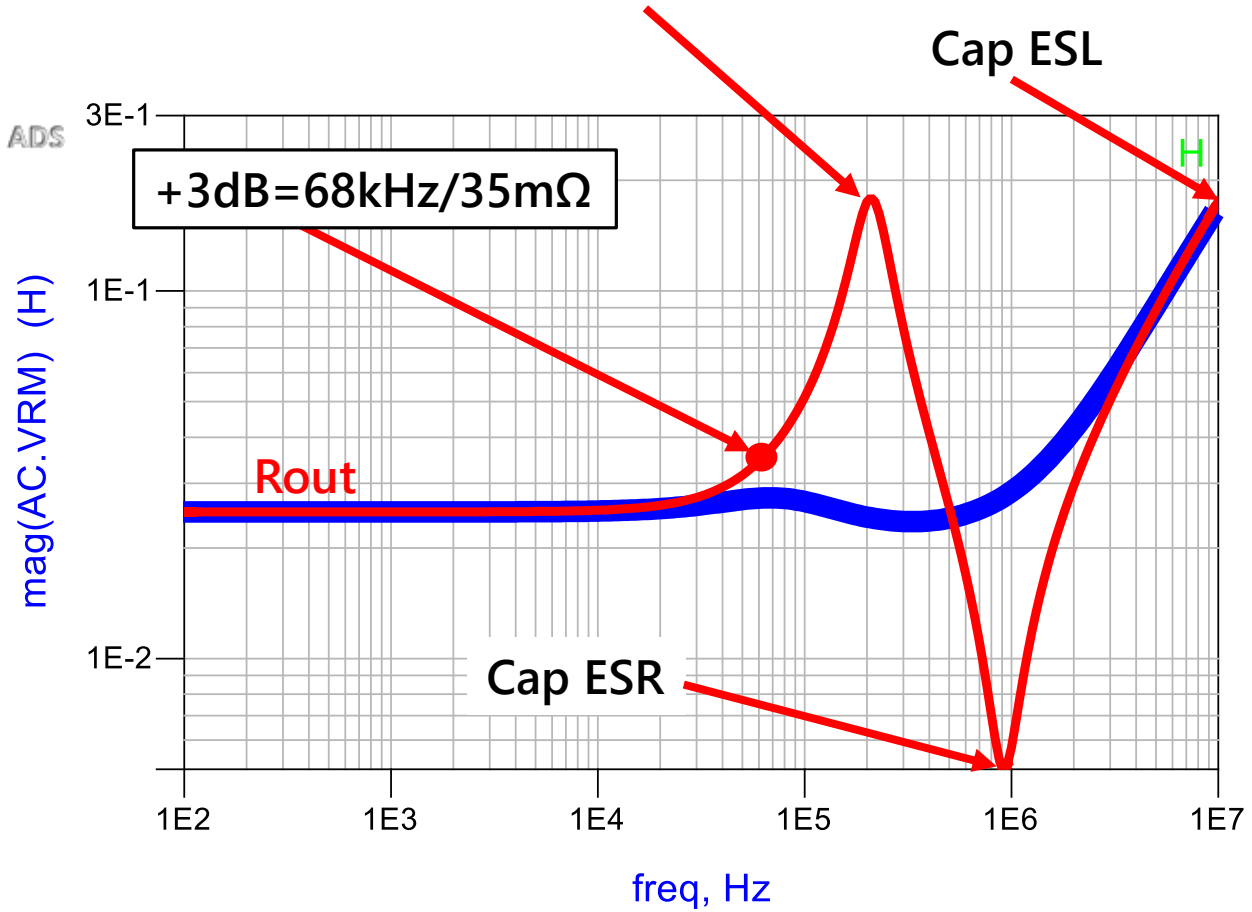
The capacitor is chosen to match the desired impedance and to counteract the inductor

$$C_{out} = \frac{1}{2\pi(68kHz)(35m\Omega)} = 72uF$$

$$C_{esr} = Rout = 25m\Omega$$

Polymer capacitors tend to have flat ESR vs. frequency which works best in these applications

Undersized output capacitor reveals the inductance resulting from the internal pole and slope compensation



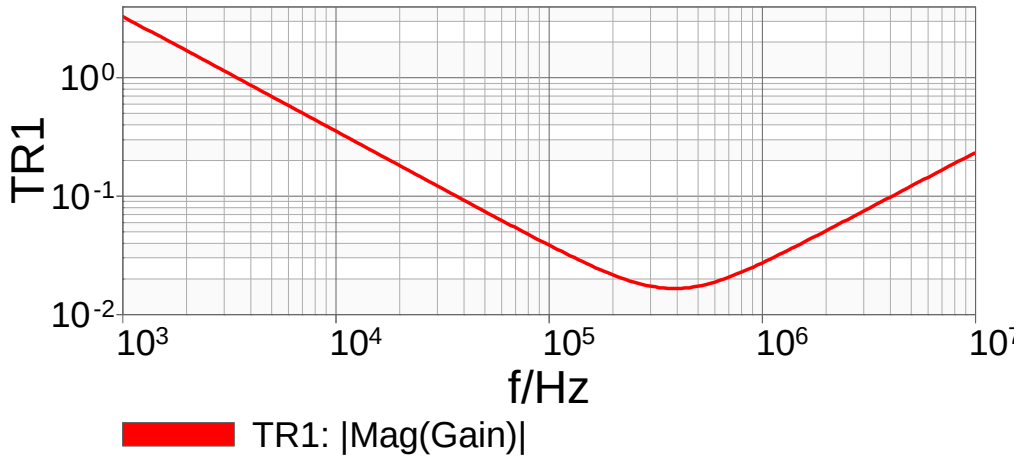
PICOTEST

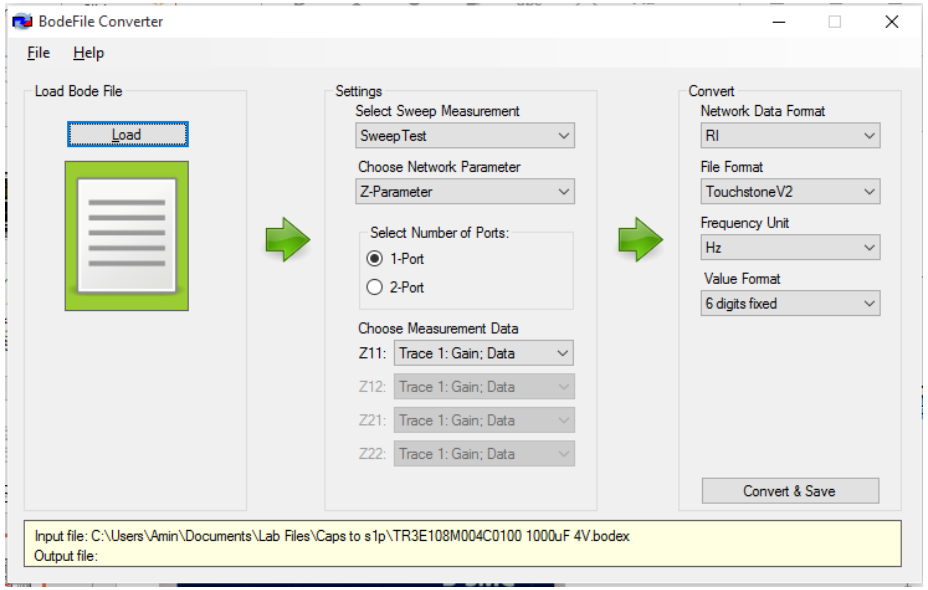
Measure Potential Output Capacitors

Low ESR caps must be mounted in a calibrated PCB for measurement

An impedance fixture can be used if ESR ≥ 100mΩ

The 2-port shunt thru method can easily measure capacitors with ESR as low as 1mΩ



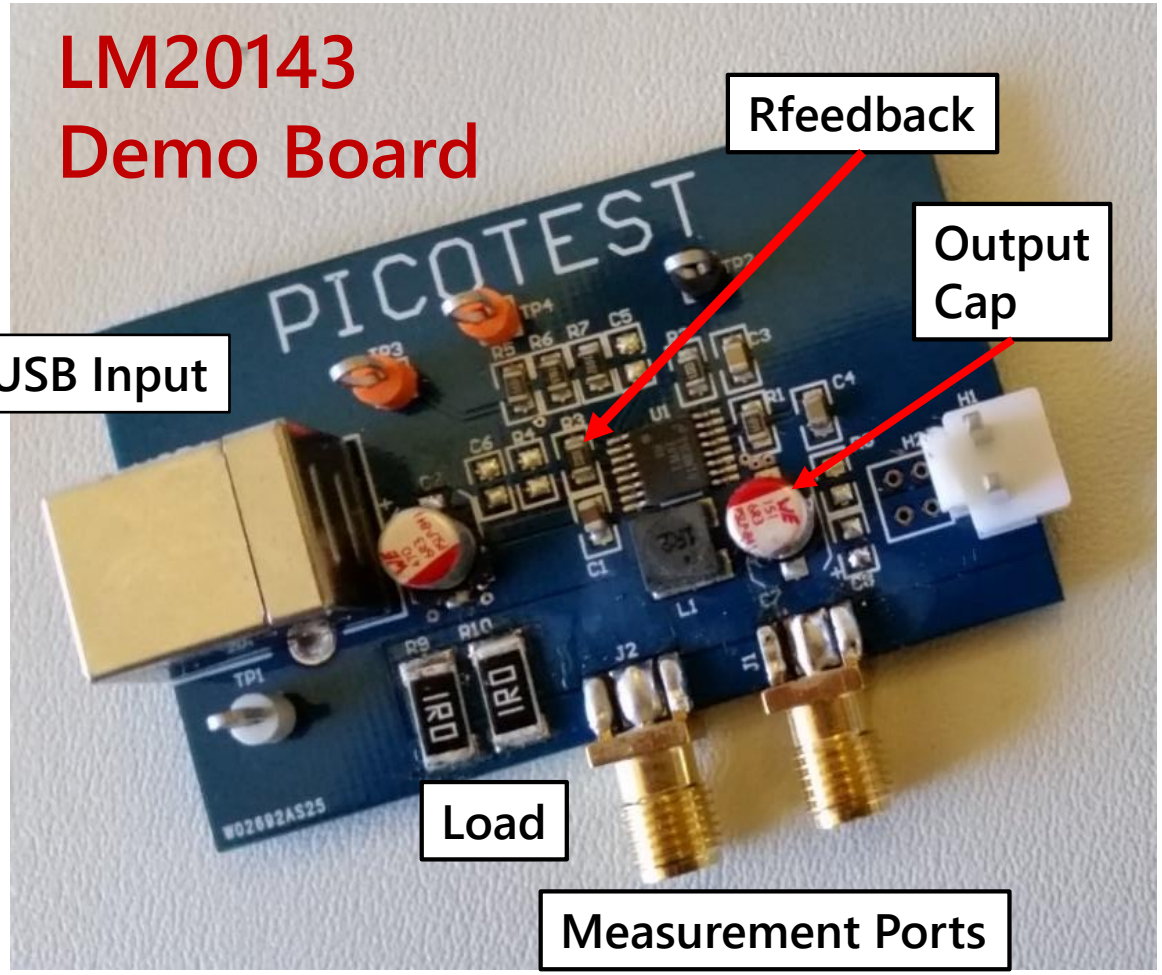


The BodeFile Converter can be used to convert the Bode 100 impedance measurements to a Touchstone file for co-simulation

PICOTEST

Case Study – Integrated Switch Step-Down

- A state space average model was constructed in ADS from several measurements.
- A number of potential output capacitors were selected and measured then converted to Touchstone files for co-simulation.
- Four capacitors were chosen to create 4 different flat resistance VRMs
- Each of the 3 solutions was constructed and measured. The TI LM20143 Evaluation board was also measured.
- The measured impedance results were converted to touchstone files using the BodeFile converter so that they can be displayed along with the simulation result



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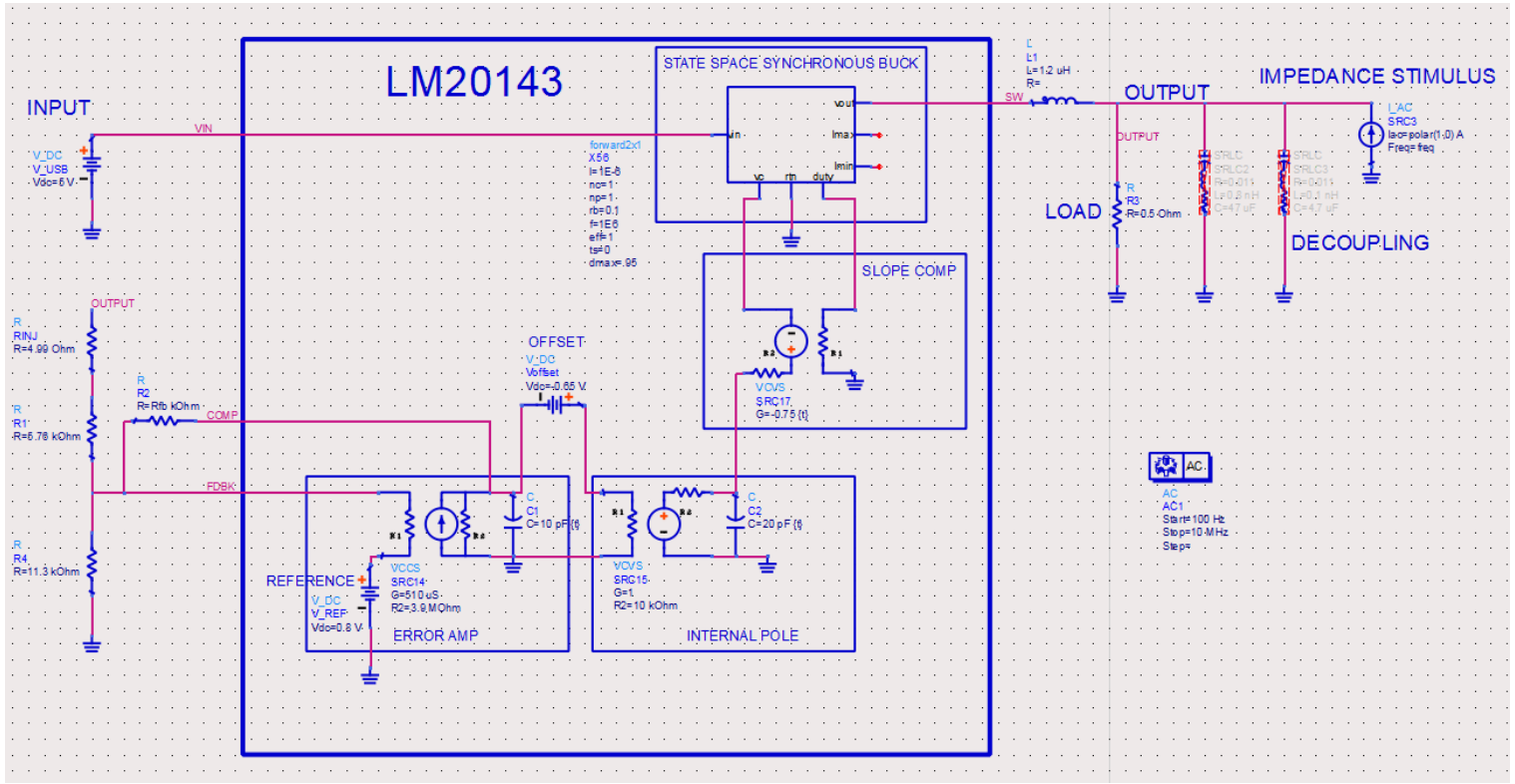
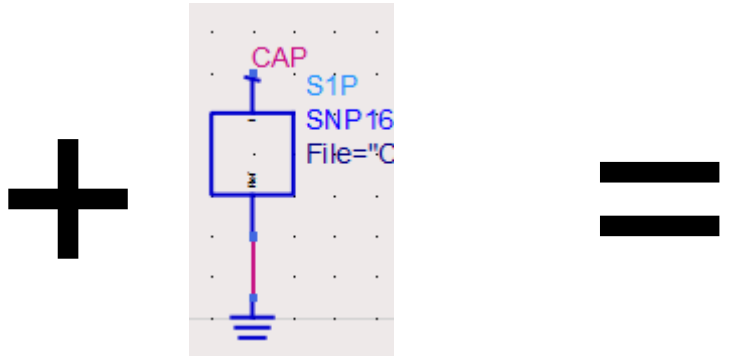
ADS Co-Simulation

A large signal simulation model combined with…



… measured capacitor impedance



Incredible Fidelity!

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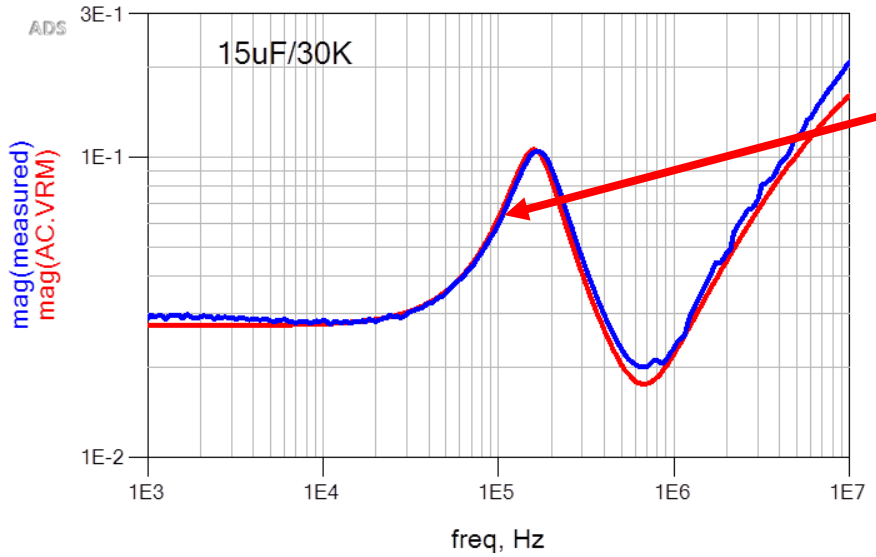
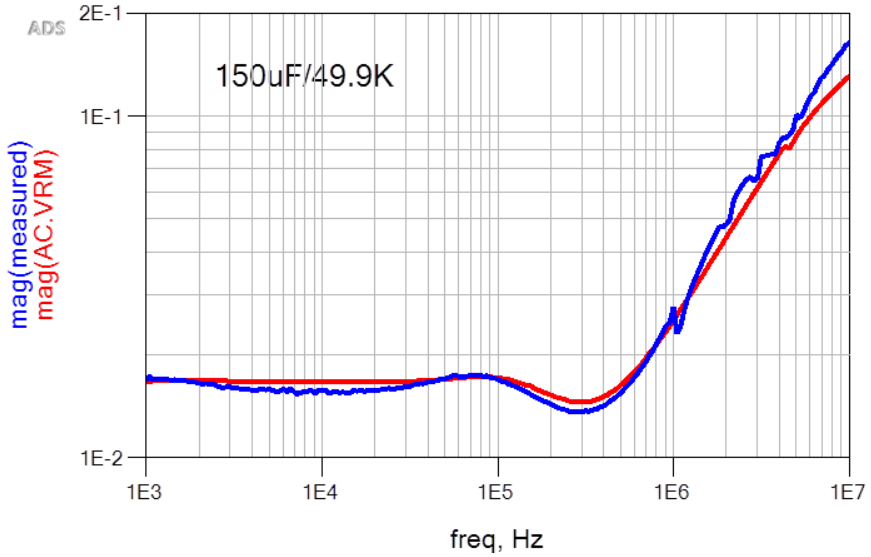
The Final Results

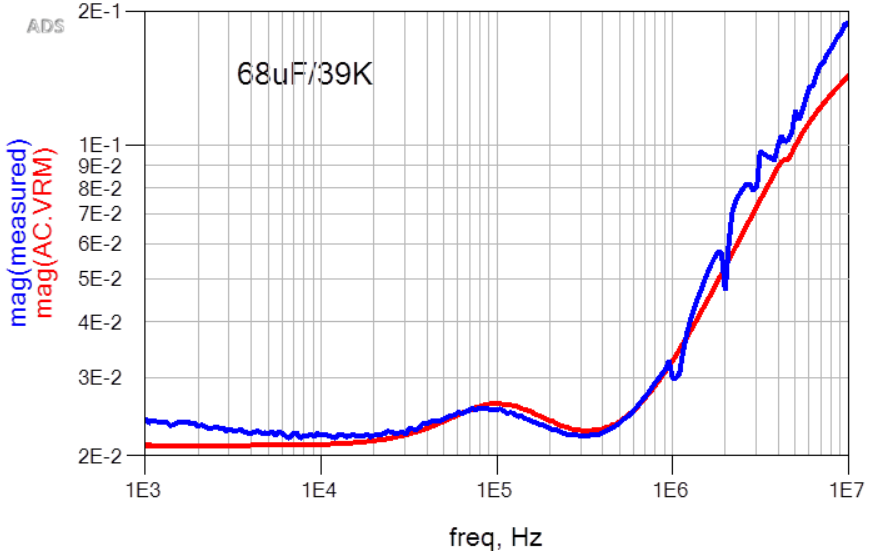


Undersized capacitor reveals the effective VRM inductance

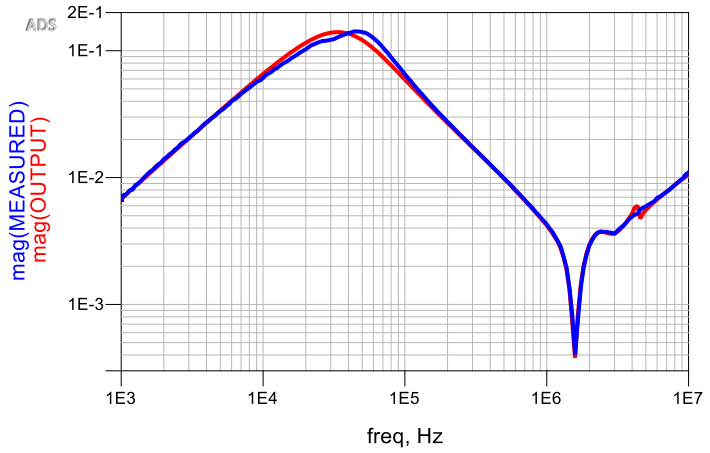
SIMULATED

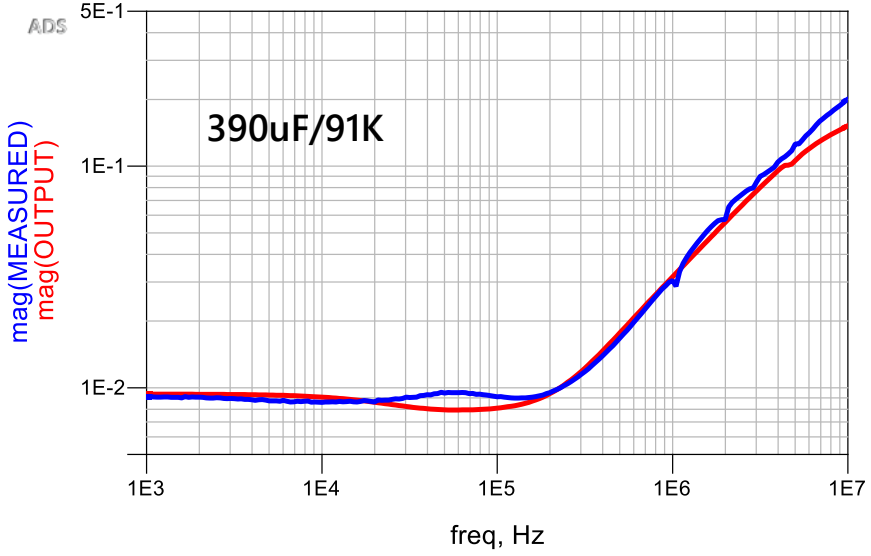
MEASURED





TI Evaluation Board





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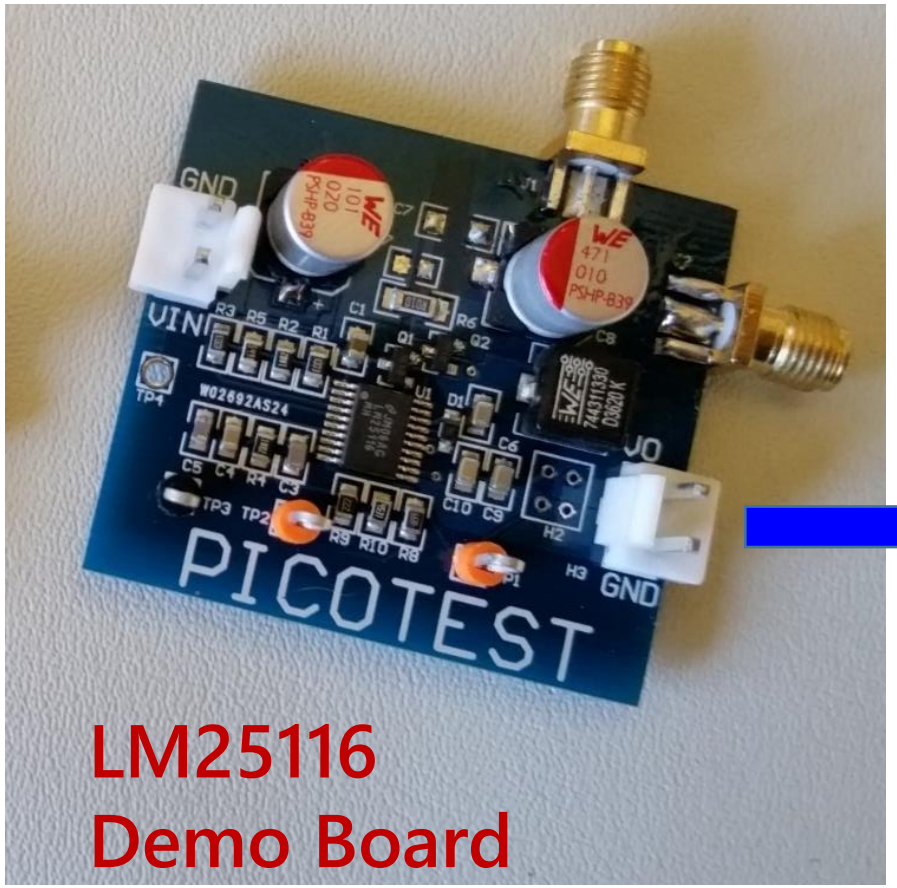
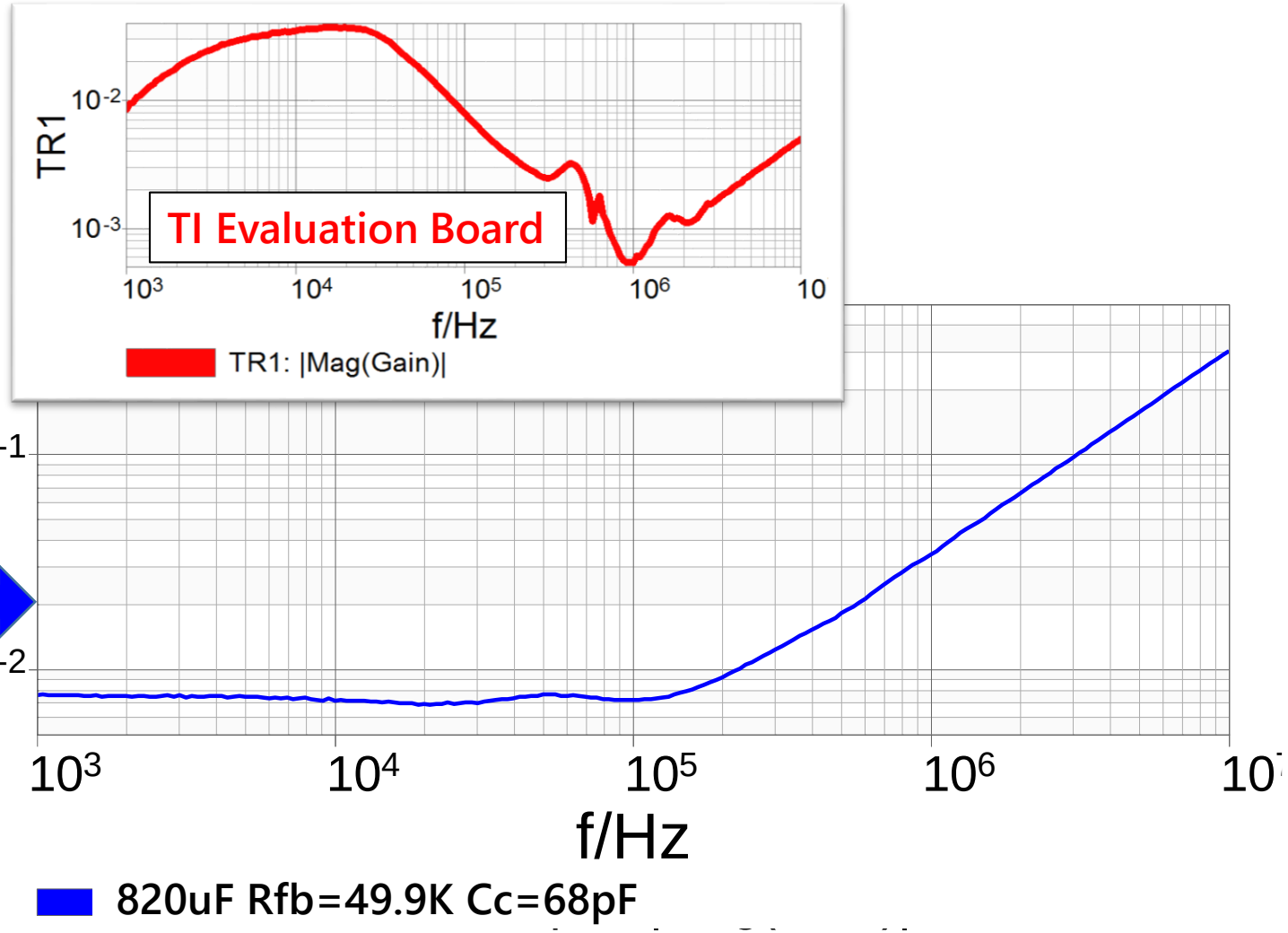
This Works with Other Controllers Too



LM25116
Demo Board



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Ceramic Decoupling Capacitors

TDK

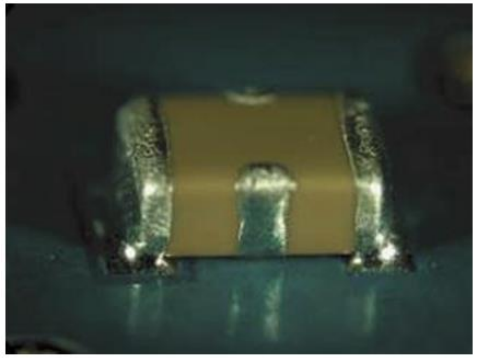
Noise Absorber

Controlled ESR Type

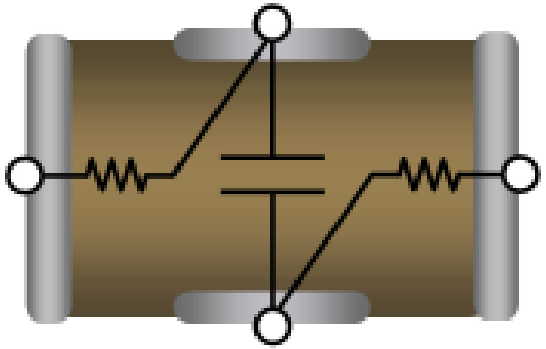
YNA Series

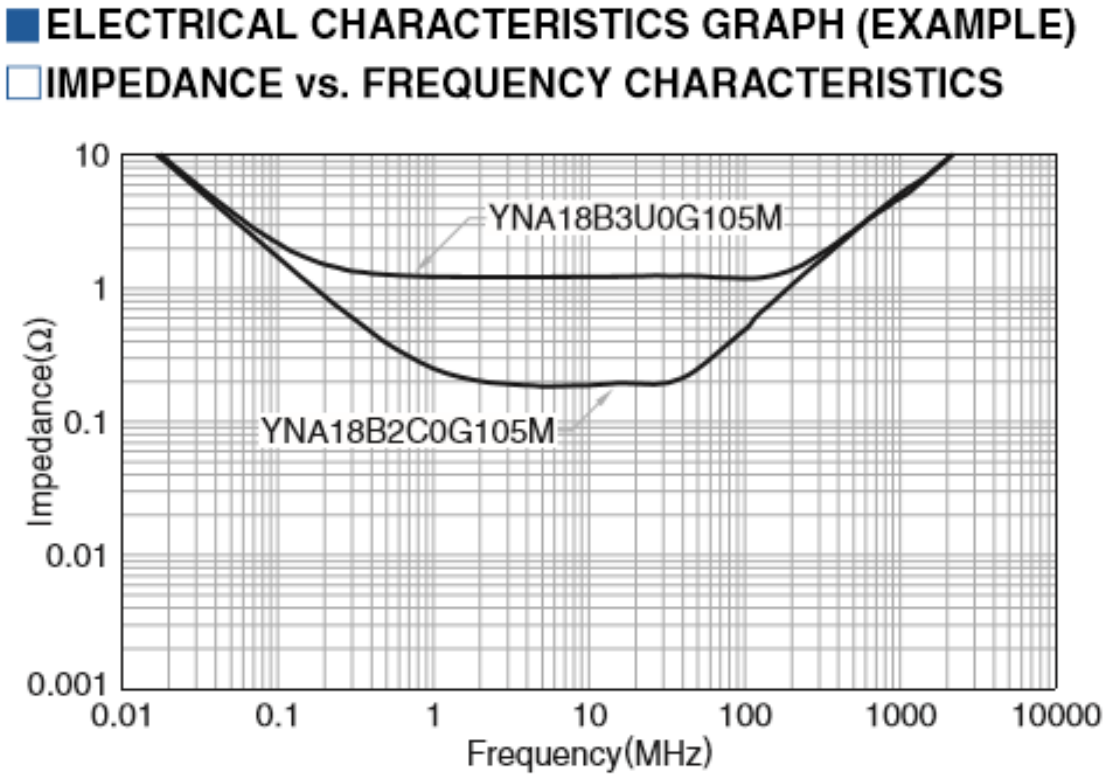
Type:	YNA15	1005 [0402 inch]
	YNA18	1608 [0603 inch]
	YNA21	2012 [0805 inch]

* Dimensions Code JIS[EIA]



ESR controlled ceramic capacitors such as TDK's YNA series can be used, though the selection is quite limited and the cost is typically high





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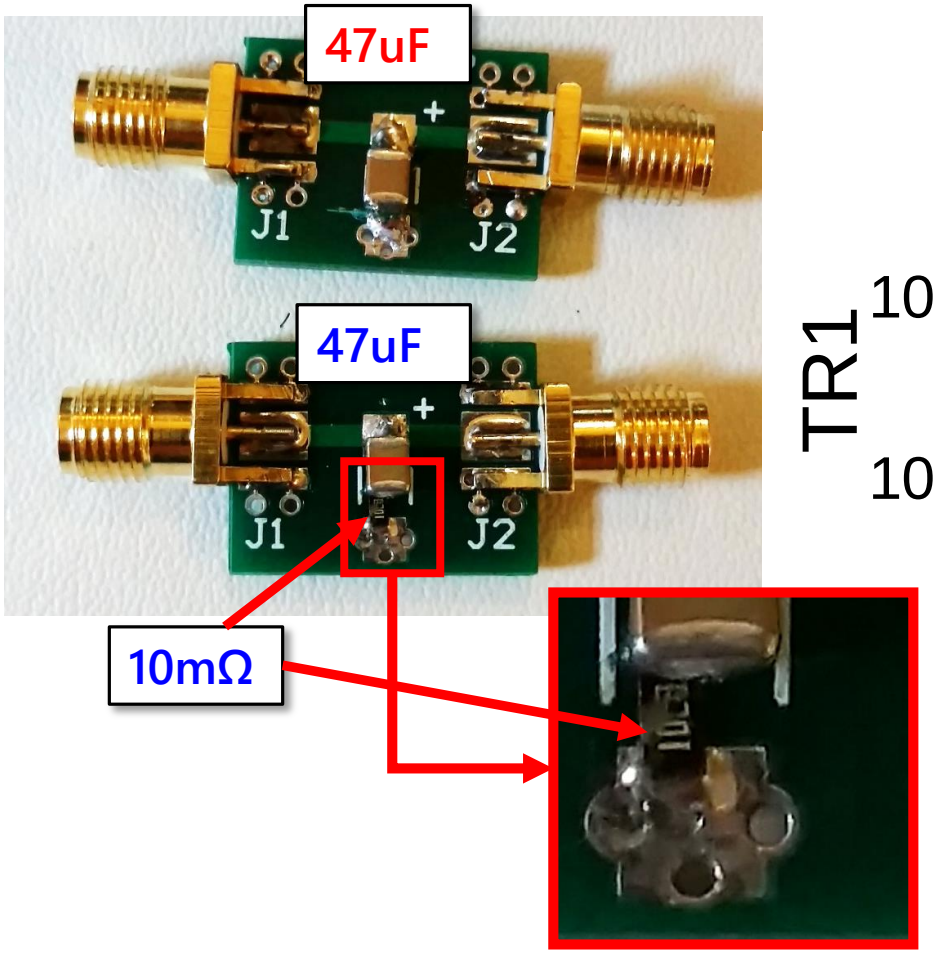
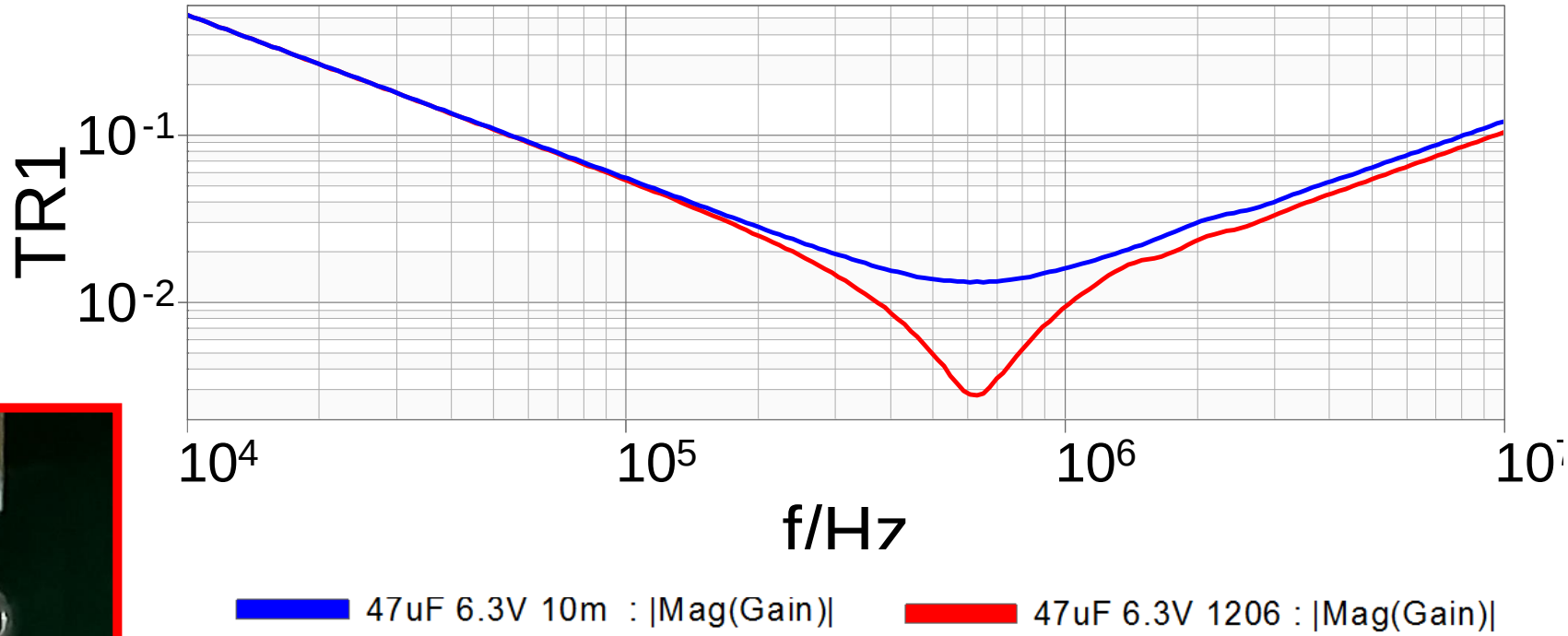
Ceramic Decoupling Capacitors

External resistors can be used with standard ceramic capacitors with slightly higher inductance but much better selection and lower cost





Convert measurement to Touchstone or RLC

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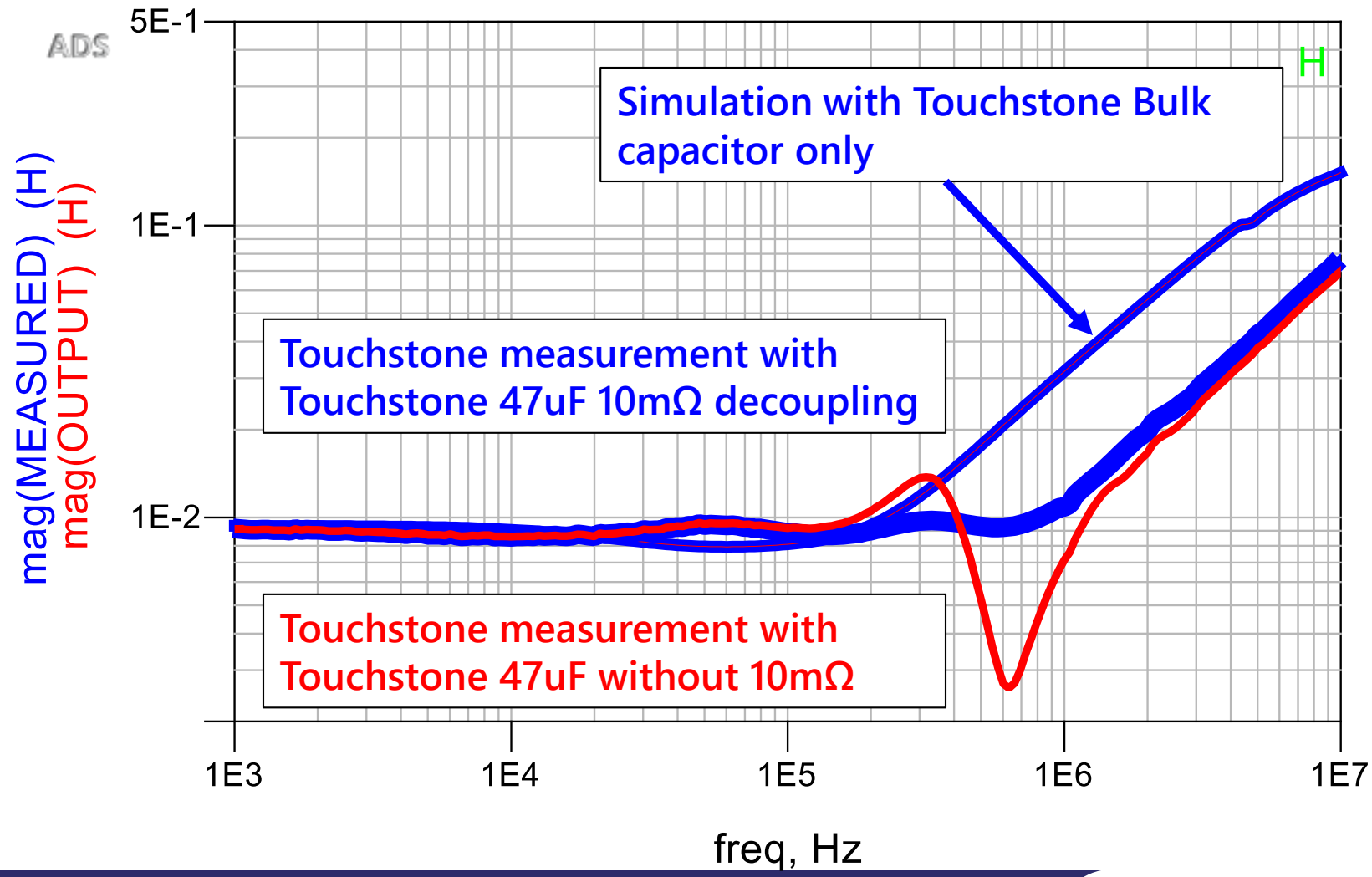
Co-Simulated Results With Decoupling Capacitors

The decoupling capacitors can then be converted to RLC models or the Touchstone files can be combined directly in a mix and match selection.

Here we are showing a large signal simulation combined with a Touchstone capacitor on one trace. The measured Touchstone result is then combined with touchstone decoupling capacitors to see the flatness with and without the external 10mΩ external resistor.



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Thanks for Attending Today's Webinar

Steven M. Sandler
Managing Director
www.picotest.com
(480) 375-0075

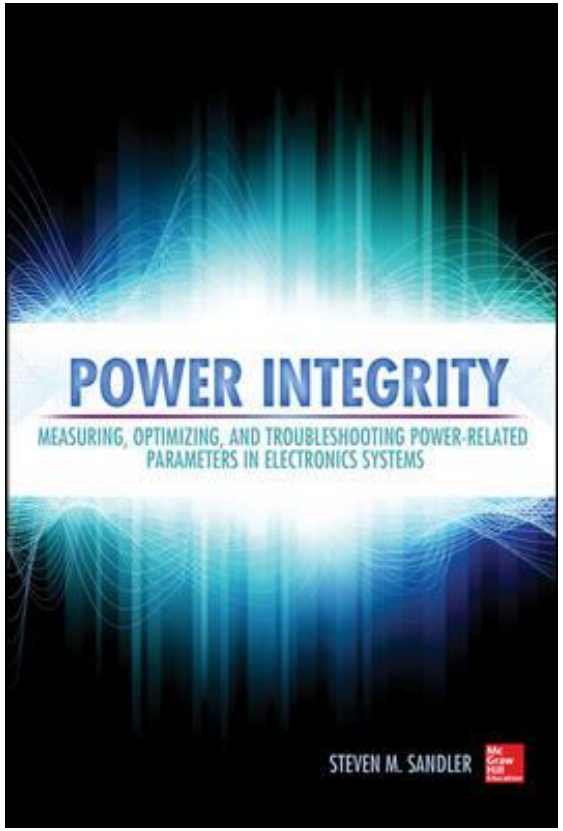
Want to try a Bode 100 and signal injectors to perform this impedance measurement?

Want to try these simulations yourself? Email me for links to ADS, the reference hyperlinks and the workspace files I used today.

steve@picotest.com

Want this flat impedance demo board? It's available at www.picotest.com under the training tab.

Want to learn more about Power Integrity?



Definitions

VRM – Voltage Regulator Module - Either a linear or switching regulator, supplies power to a system

PDN - Power Distribution Network - How power gets from VRMs to ICs

Resonance – A peak in the PDN impedance profile

PSRR – Power Supply Rejection Ratio

Rogue Wave – Changes in the power required by the load are not DC, they occur in steps. Those steps can line up and reinforce one another resulting in large voltage excursions

ADS – Keysight (formerly Agilent) simulator

Noise Budget – the voltage deviation as determined by the needs of the loads (usually must be less than the absolute maximum for the ICs being driven but other performance factors (e.g. frequency content) are important too)

Gfs – The ratio of the change in output current resulting from a change in input voltage

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