FUTURE ELECTRONICS

An Introduction to Power Supply Simulations with SIMPLIS

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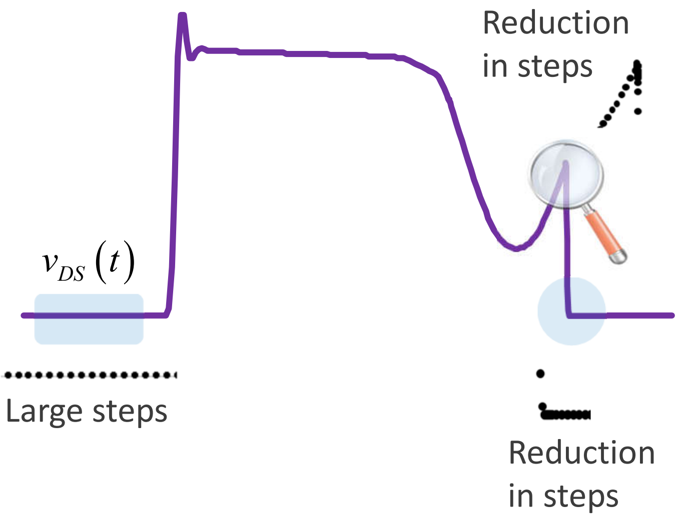
Agenda

- SPICE and Power Converters
- The SIMPLIS Approach
- Transfer Functions
- Power Factor Correction
- Interactions with EMI Filter
- Monte Carlo Analysis
- Design Example of a Flyback Converter

The SPICE Engine

- SPICE is a linear solver in essence: any nonlinear behavior must be linearized
- SPICE samples at a variable timestep: it adjusts its course based on signals shapes
  - Flat type of waveform: large timesteps are taken
  - Change occurs: timestep reduction until enough precision is obtained

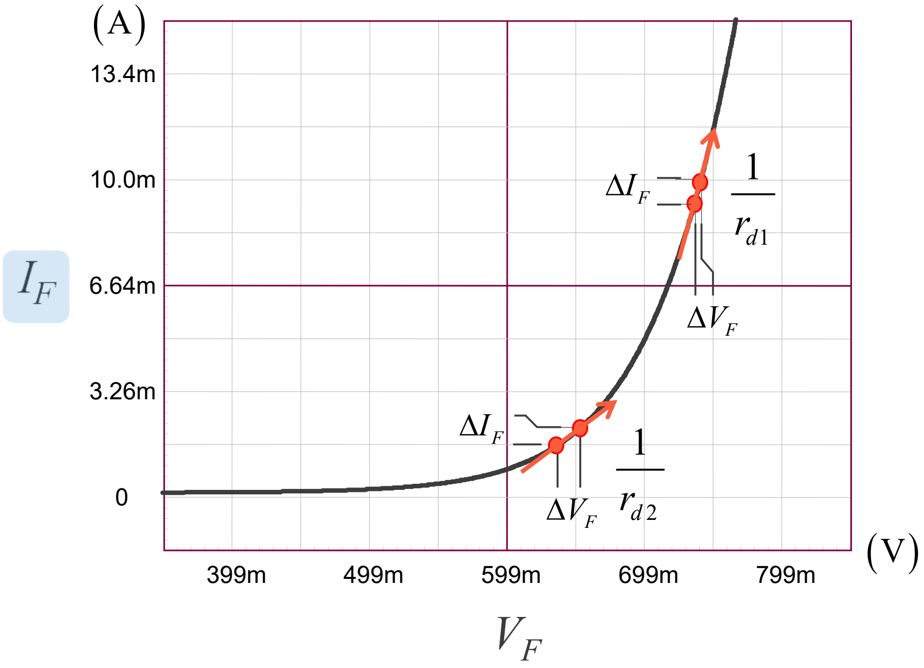


- Timestep control algorithm is an essential part of the engine:
  - ✓ It controls the number of iterations to find a solution
  - ✓ It checks that timestep reduction brings a precise solution – jump to next point or fail!

Highly time-consuming process!

A Piece-Wise Linear Approach – Diode Example

- A diode is a nonlinear device affected by a variable dynamic resistance r_d
- SPICE will have to linearize the component at every change in operating point



$$r_{d1} = \left.\frac{\Delta V_F}{\Delta I_F}\right|_{I_{F1}}$$

$$r_{d2} = \left.\frac{\Delta V_F}{\Delta I_F}\right|_{I_{F2}}$$

Operating points

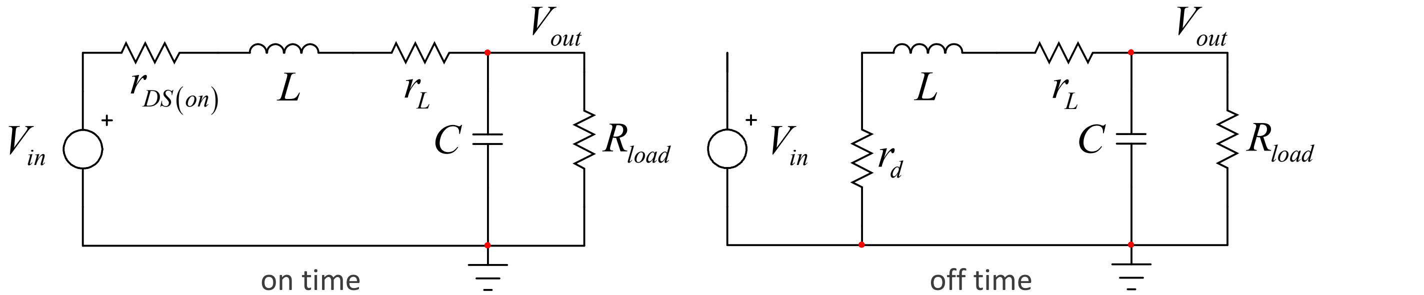
$$I_F = I_s\left(e^{\frac{v_F}{nV_T}} - 1\right)$$

$$\hat{i}_F \approx I_F \frac{\hat{v}_F}{nV_T}$$

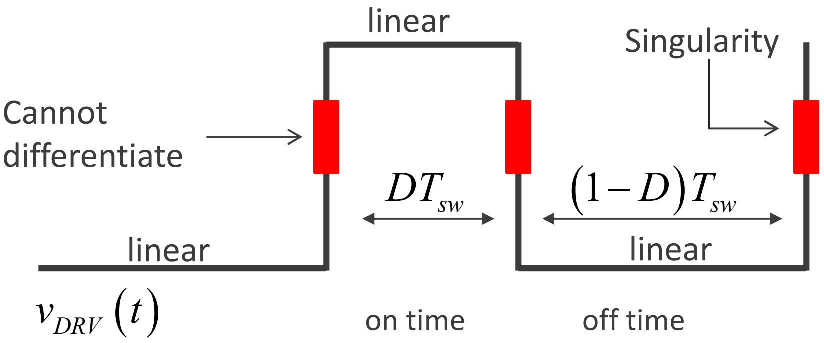
$$r_d \approx \frac{nV_T}{I_F}$$

A Switching Converter is a Nonlinear System

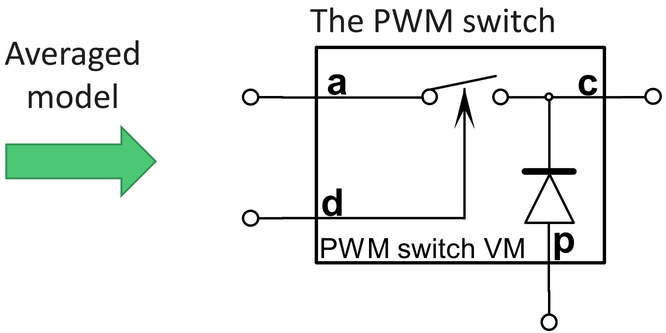
- A switching converter is exhibiting linear characteristics during t_{on} and t_{off}



- The toggling event between the two networks introduces a discontinuity

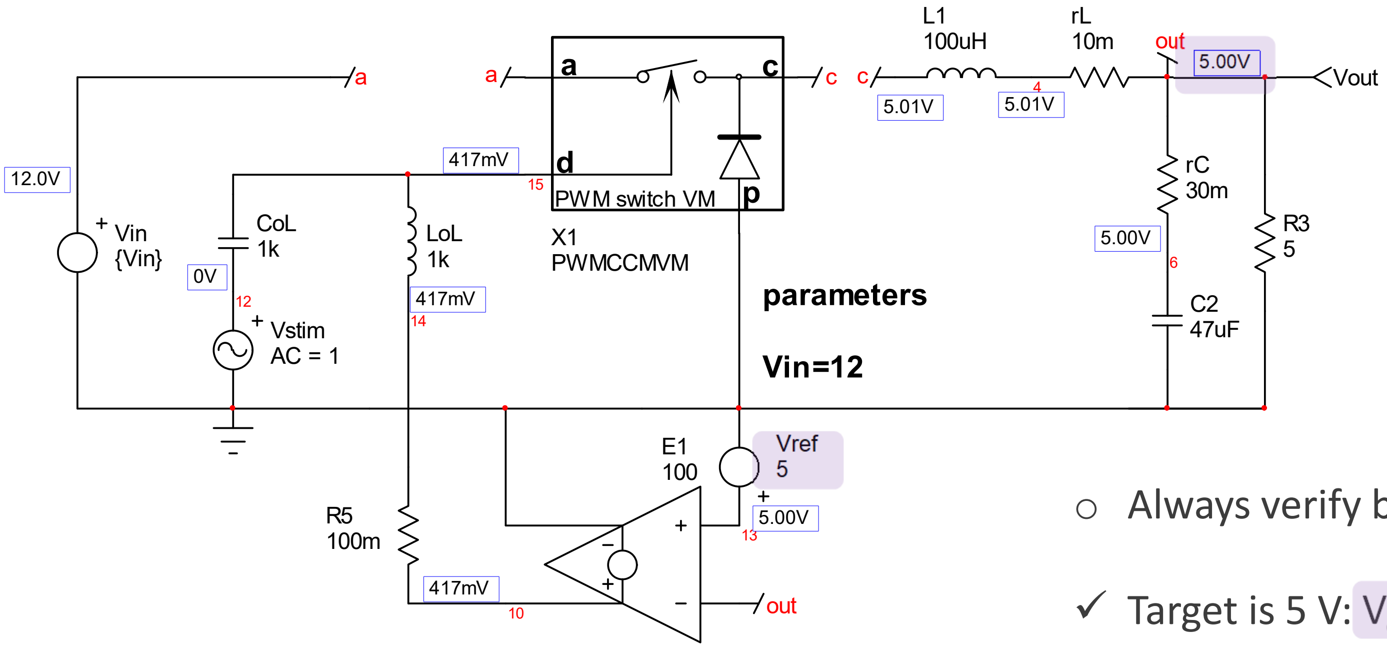


Averaged model



The Need for an Averaged Model

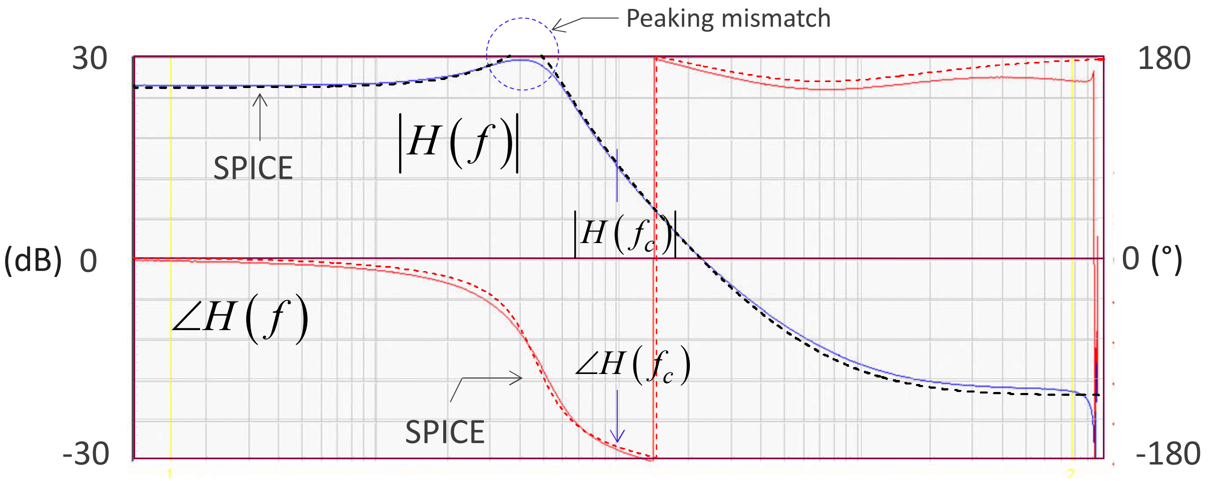
- An averaged model excludes the switching component by construction
- The simulation time is flashing and some models operate in ac and transient analyses
- ➢ What if I don't have an averaged model for my particular converter?



- ○ Always verify bias point!
- ✓ Target is 5 V: $V_{out} = 5$ V

An Accurate Bode Plot

- When the simulation is fine-tuned, matching with laboratory experiments is excellent
- One of the keys for success is to precisely extract parasitics such as capacitors ESRs



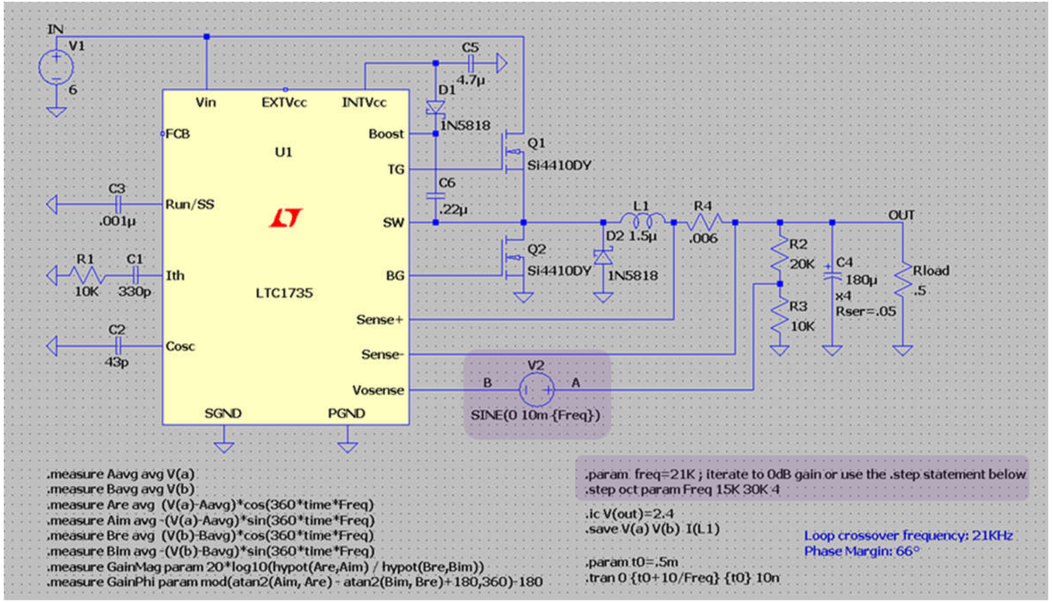
Control-to-output transfer function of the voltage-mode buck converter

- ✓ Tweak your model until it reflects hardware measurements for high-fidelity simulations
- ✓ With a validated model, you can explore stability margins on the computer

ESR: equivalent series resistance

A Frequency Response Analyzer with SPICE

- Some SPICE packages such as LTspice offer a means to measure the loop
- The circuit is switching and a signal is injected for ac-modulating the converter
  - ➢ The source must be of sufficiently-low amplitude to avoid saturation



- ✓ Works ok for a narrow analysis band around crossover – starts at 15 kHz up to 30 kHz in this example
- ✓ Simulation time can be long, especially if one wants to reveal sharp resonances
- ✓ How to simulate PFC stages with sweep starting below 1 Hz and a 10-Hz crossover?

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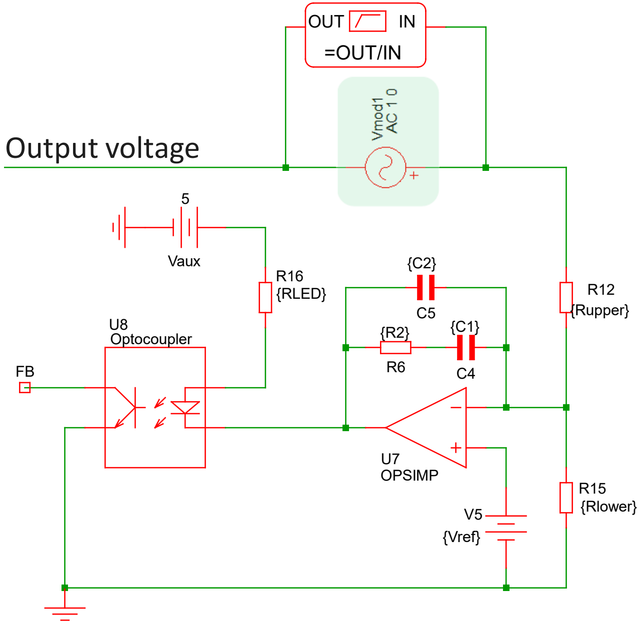
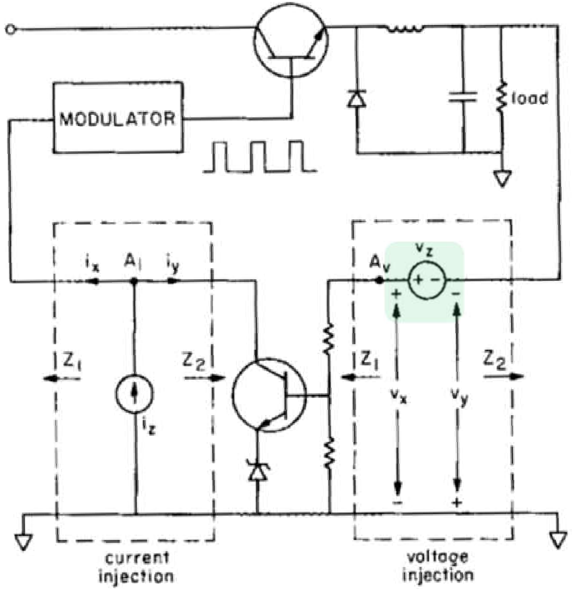
A Time-Domain Simulator

- SIMPLIS is a time-domain simulator and operates with switching components
- Ac analysis is carried over a switching converter: no need for an averaged model
- Frequency response is revealed the same way as if it were carried in the laboratory





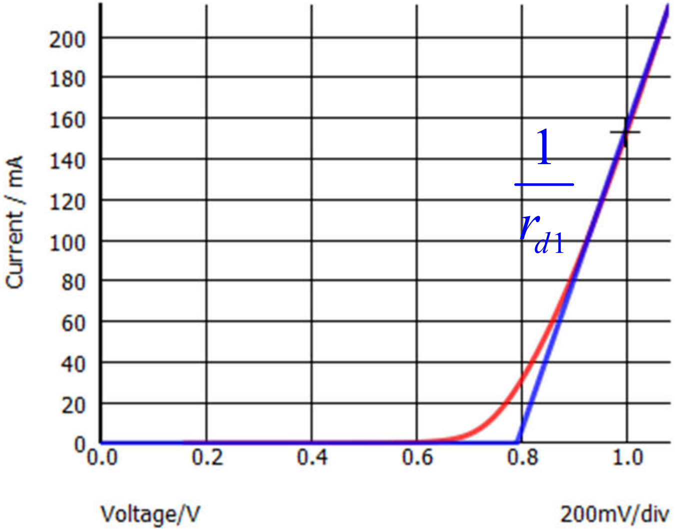
Ac source

Injection transformer

R.D. Middlebrook, *Measurement of Loop Gain in Feedback Systems*, Int. J. Electronics, 1975, vol. 38, No. 4, 485-512

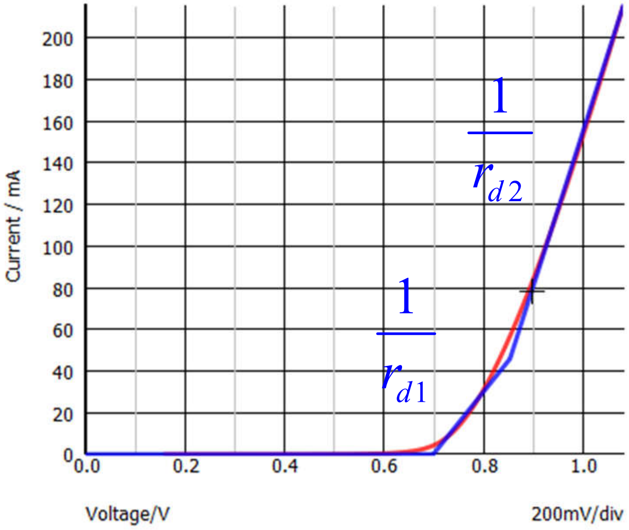
Two Segments are Enough for a Diode

- SIMPLIS uses a PWL approach where a component is modeled through segments
  - Any change in operating point is modeled as a transition to another segment
  - At any instant in simulation time, the system is always linear!



A two-segment model

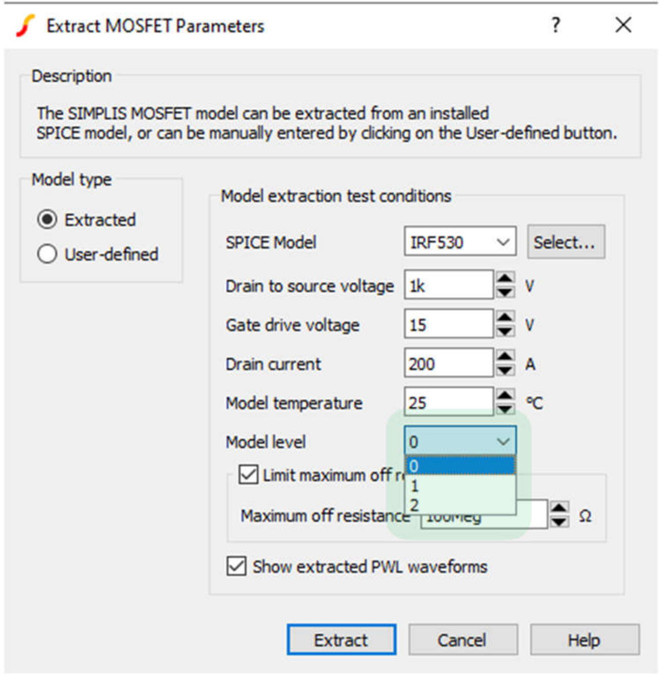
More segments

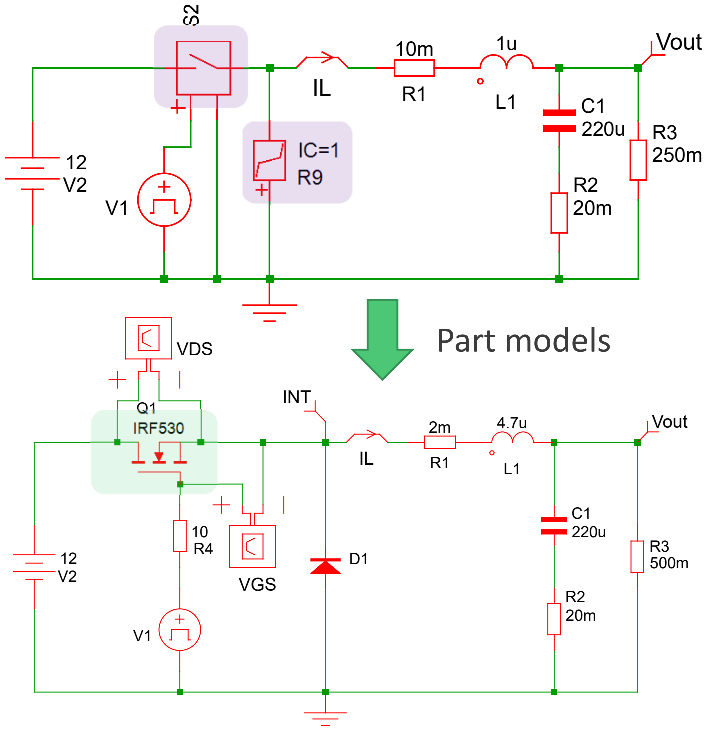


A three-segment model

Piece-Wise Linear Modeling of all Components

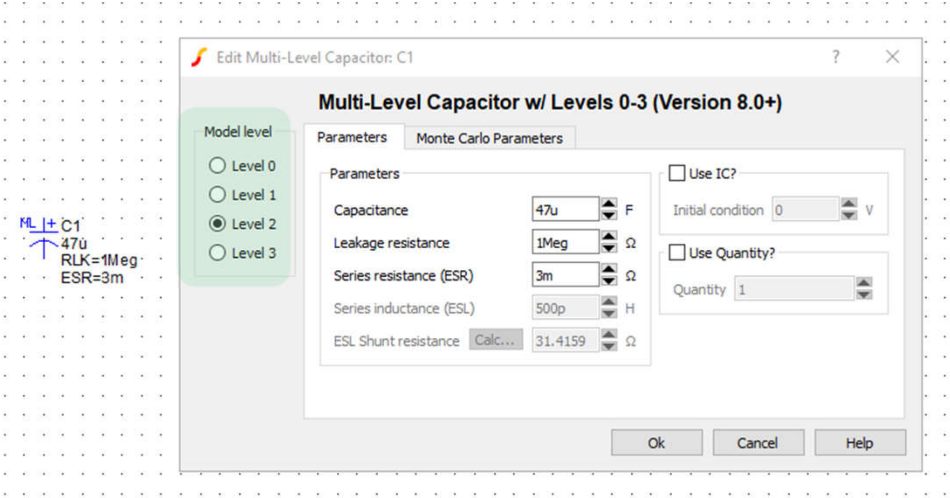
- Components can be modeled with accuracy to reflect real operating waveforms
- By selecting different levels, it is possible to gradually improve precision

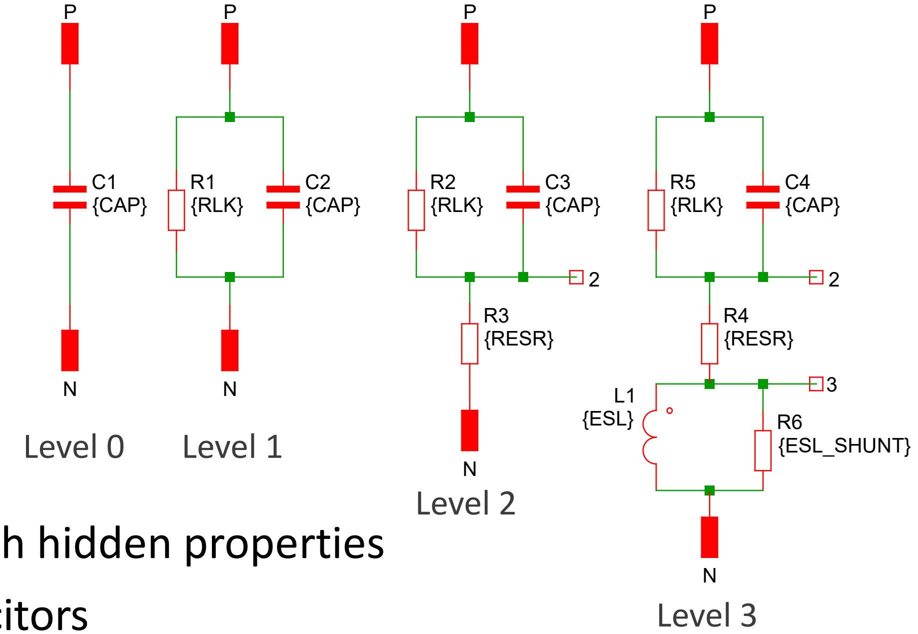




Passive Elements include Parasitics

- Typical elements such as capacitors can embark parasitics such as ESR or ESL
- Select the model level between 0 (the simplest) and 3 (the most comprehensive)

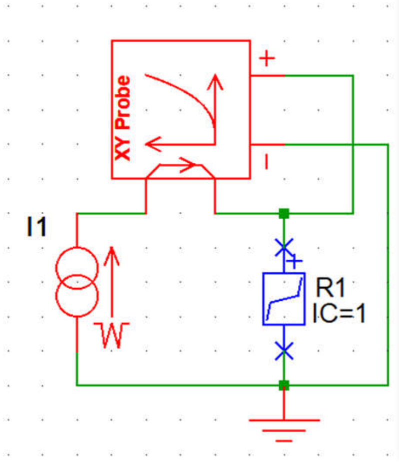


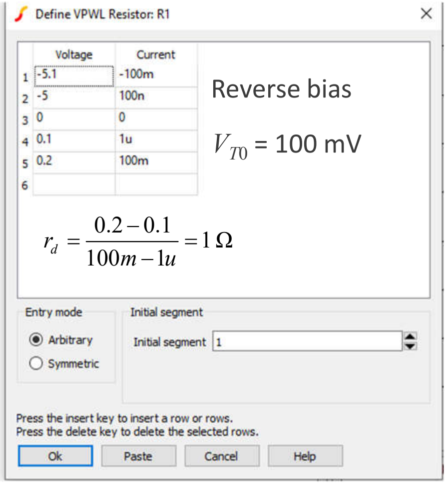


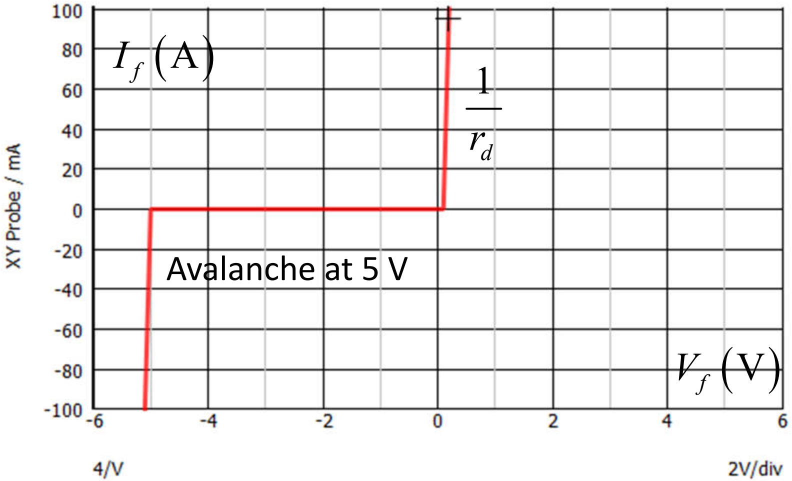
- ✓ Avoid over-populating your schematic with hidden properties
- ✓ You can also model bias-dependent capacitors

Voltage- or Current-Dependent Passive Elements

- You can model any sort of behavior with a PWL element: resistor, capacitor or inductor
- ➢ A PWL resistor models a diode with a specific threshold and a dynamic resistance r_d
- ➢ A saturating inductor showing the effects of too high a peak current
- ✓ Use realistic numbers for slopes, e.g. 10-100 mΩ not 1 pΩ!

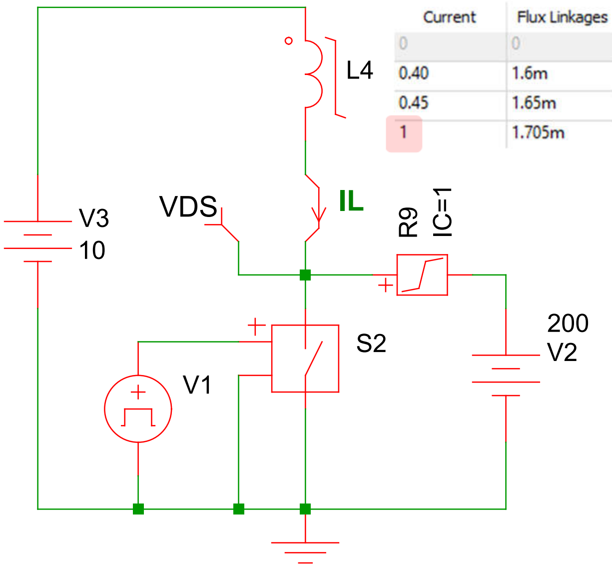




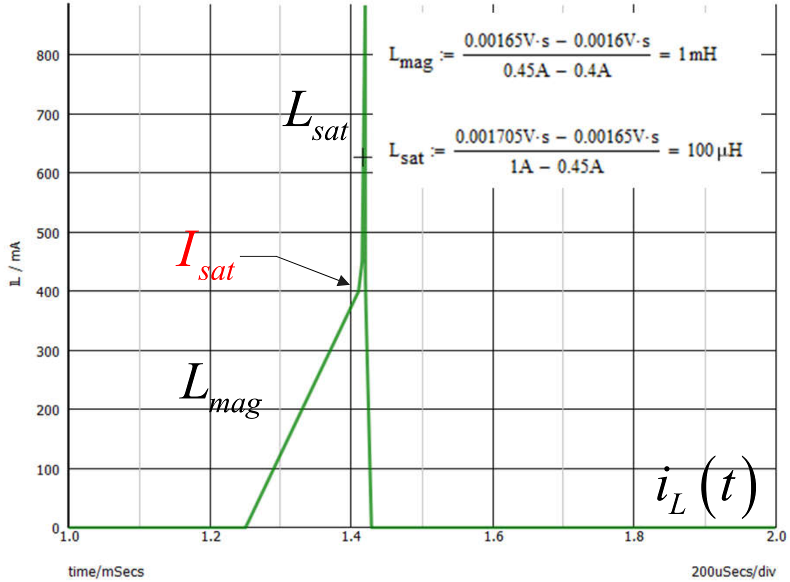


A Saturating Inductor is Easy to Model

- It is important to visualize the effects of core saturation in a simple way
- SPICE models featuring hysteresis effects like Jiles-Atherton are complicated to handle
- ✓ A few PWL lines and you have the shape of a saturating inductor

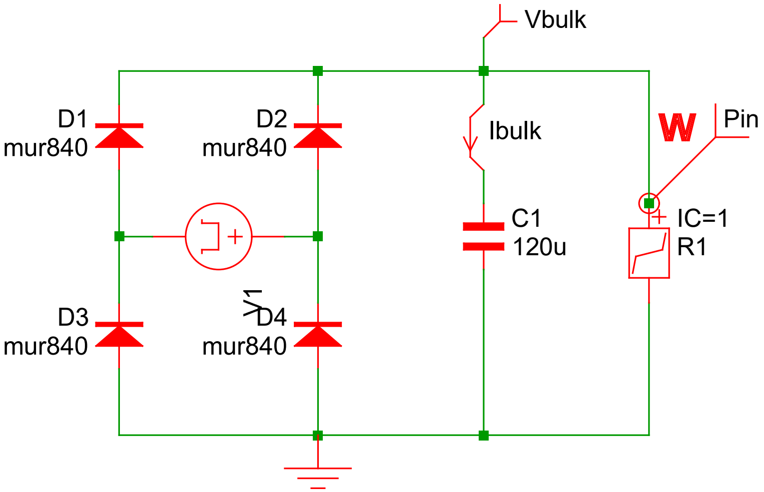


Current (A)	Flux Linkages (V.s)
0	0
0.40	1.6m
0.45	1.65m
1	1.705m



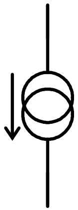
Constant-Power Current Source

- A constant-power source is useful to determine the ripple current in a bulk capacitor
- Using Excel, it is possible to determine the absorbed current based on the on-going bias



constant

Absorbed power	90	W	
Input voltage	50	1.8	amps
	60	1.5	
	70	1.285714	
	80	1.125	
	90	1	
	100	0.9	
	110	0.818182	
	120	0.75	
	130	0.692308	
	140	0.642857	
	150	0.6	
	160	0.5625	
	170	0.529412	
	180	0.5	
	190	0.473684	
	200	0.45	
	210	0.428571	
	220	0.409091	
	230	0.391304	
	240	0.375	
	250	0.36	
	260	0.346154	
	270	0.333333	



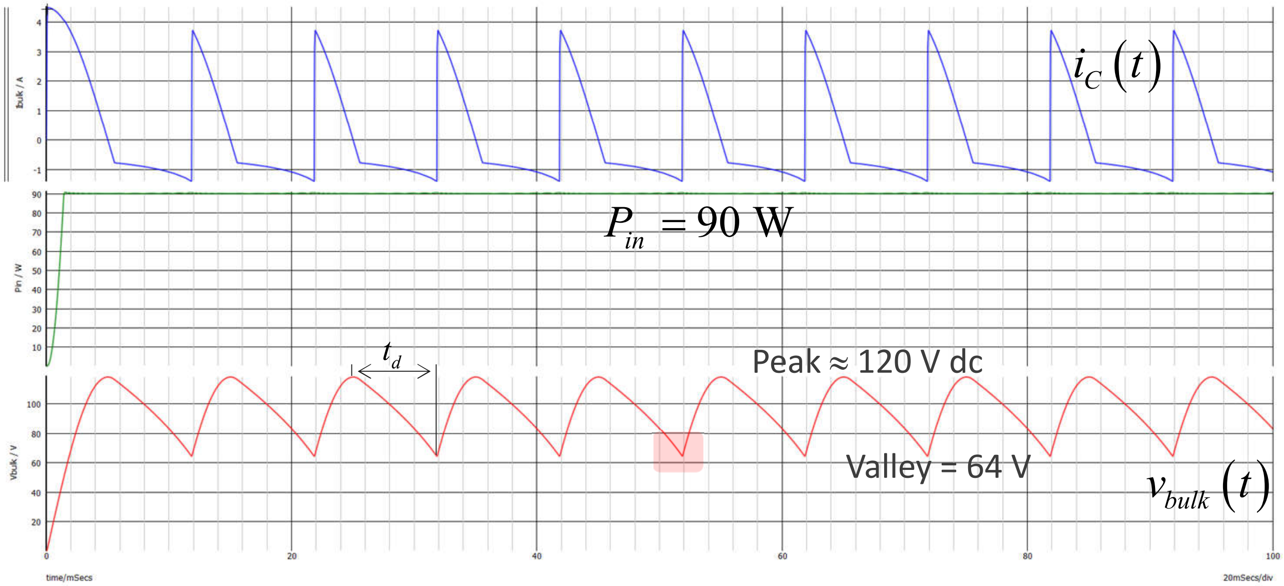
$$i(t) = \frac{P_{out}}{v_{bulk}(t)}$$

variable

- ✓ You can assess the rms current in the capacitor in worst-case situations
- ✓ Check the valley voltage corresponding to the minimum rectified dc input voltage

Peak and Valley Voltages

- The valley voltage at the lowest input mains (85 V rms) is 64 V dc



Ripple current in the capacitor: $I_{C,rms}$ = 1.6 A

Constant power absorbed by the dc-dc converter

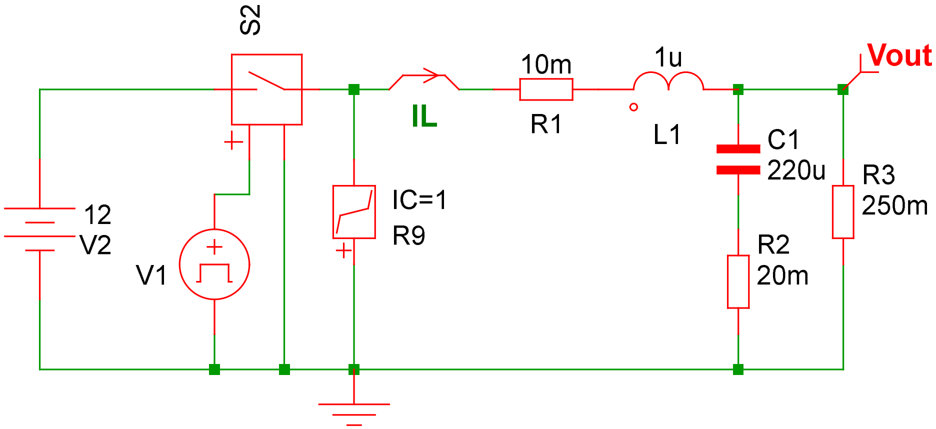
Rectified ripple voltage

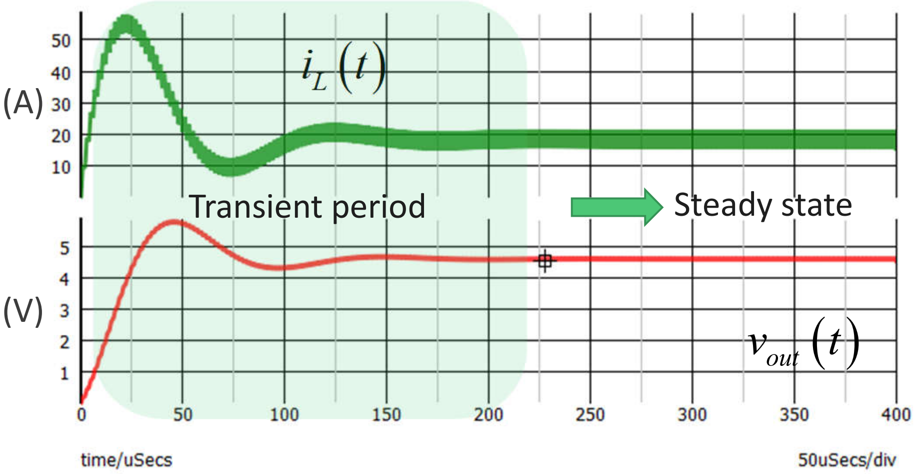
- Design the converter for operating down to 64 V (≈ 55 V with margins)

➢ Failure to do so: output ripple, loss of regulation, protection latch

Transient Time and Steady-State Operations

- A converter needs time to reach its steady-state regulated output
  - Depending on compensation, the op-amp rails up and takes time to recover
  - There can be a large overshoot which may need hundred of millisecond to damp



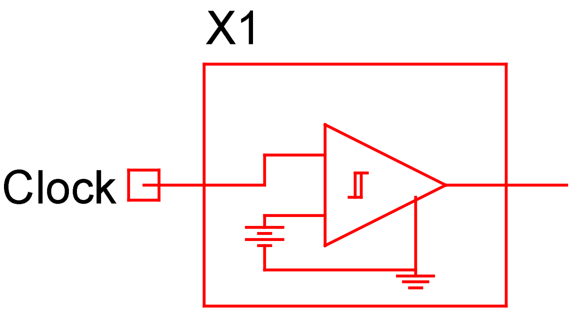


- Analysis should take place once the transient period is over: how long can it take?

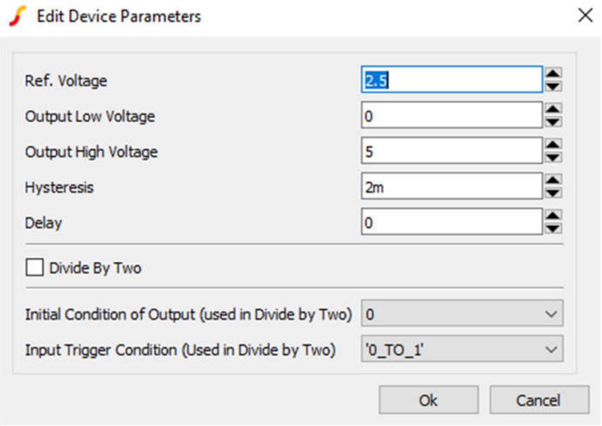
Periodic Operating Point or POP

- SIMPLIS uses a unique algorithm to meet the steady-state point in a record time
- The POP determines with the highest precision when the circuit is stabilized:

✓ Average voltage across inductors is 0 V and average current in capacitors is 0 A



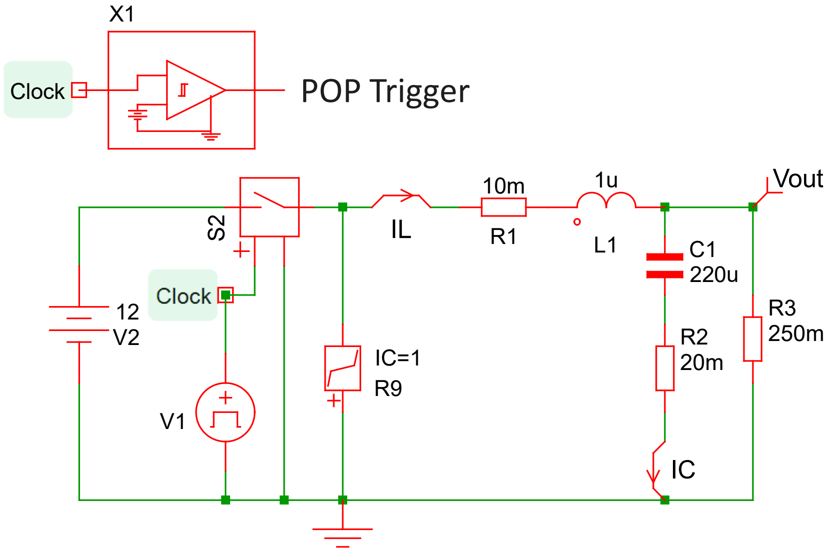
Place the pop trigger
on the schematic

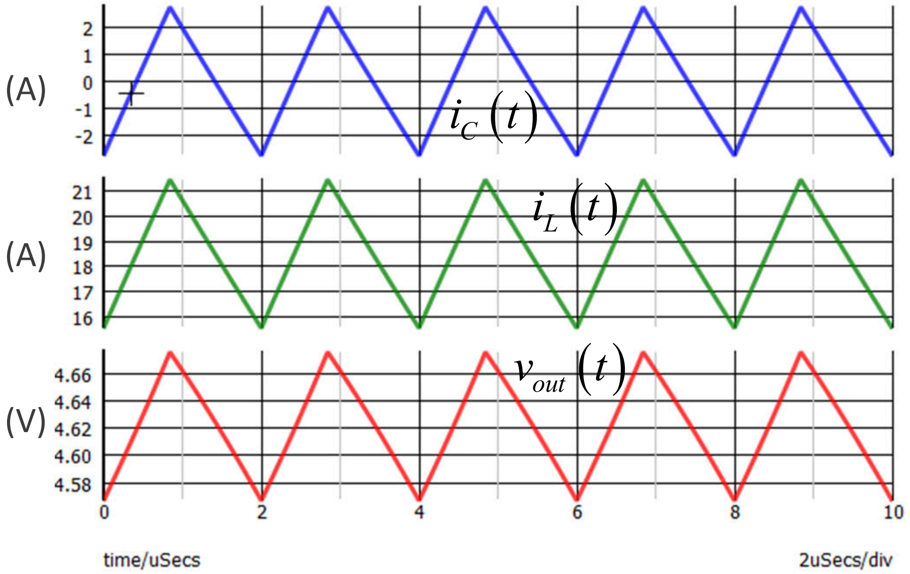


- The POP trigger will synchronize the engine with the start of each periodic cycle
- A typical output can be a clock or a driver output for instance

Find Steady-State Operation in a few Seconds

- When launched, the process finds the operating point very rapidly
- Once at steady-state, small-signal analysis can be initiated

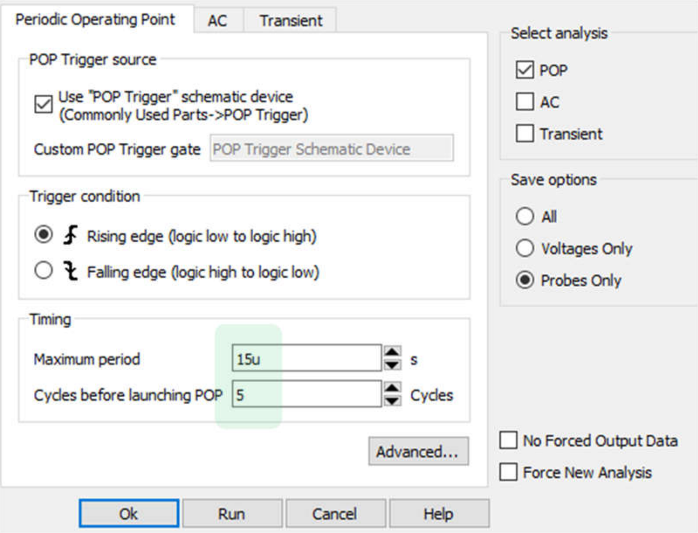




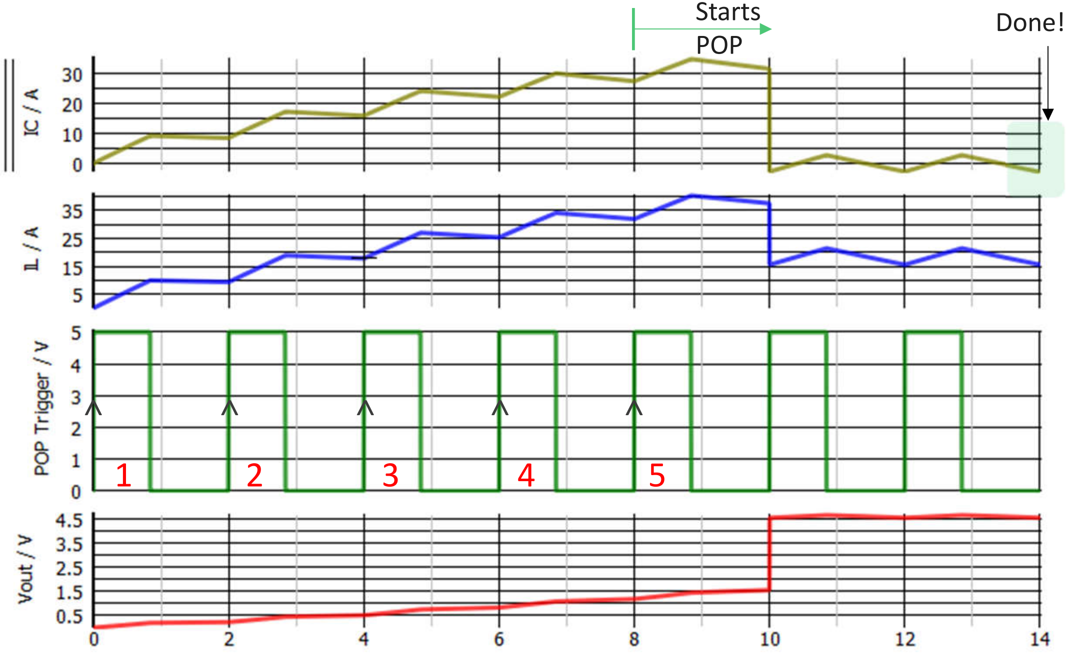
- The process is extremely precise with a convergence precision down to 1 pA and 1 pV

The Process of Finding the Right Point

- Select maximum switching period and instruct the engine when it starts its POP process
  - The clock here is 100 kHz, then choose 15 µs and go for 5 switching cycles

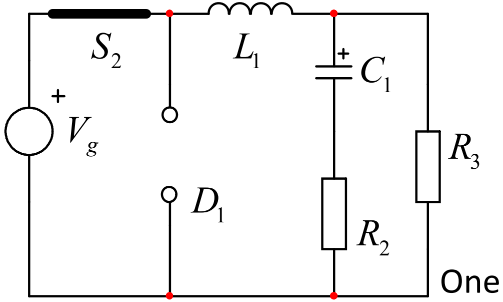


You can select various analyses from this panel

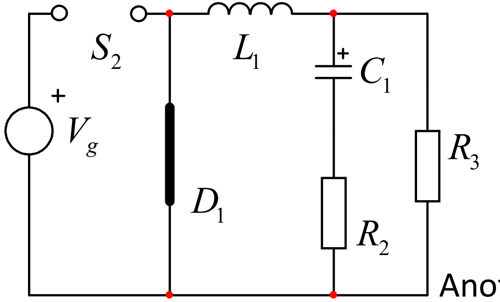


Topology Changes

- SIMPLIS while performing POP calculation explores so-called *topologies*
- A topology represents a unique state which is solved and recorded
  - As simulation progresses, known topologies are retrieved and reused to proceed



One topology



Another topology

During simulation, multiple topologies are explored

```
********************************************************************************
********************************************************************************
simplis VERSION 8.50, RELEASE Rel-21.50.2, Aug 09, 2021
Checking syntax of ``D:/christophe/Simplis/Future/Seminar/SIMPLIS_Data/simple buck.deck''

                                   New topology #1
                                   New topology #2

A starting operating point located.
                                   Elapsed time    :  0 hr  0 min  1    sec
                                   CPU time        :  0 hr  0 min  0.04 sec
                                   Simulation time: 0.000000000000e+00 sec


           PERIODIC OPERATING-POINT ANALYSIS


                                   New topology #3
                                   New topology #4
                                   New topology #5
                                   New topology #6
                                   New topology #7
           PASS    1:   1.637373e+01 %
           PASS    2:   9.162850e-14 %
                                   Elapsed time    :  0 hr  0 min  1    sec
                                   CPU time        :  0 hr  0 min  0.00 sec
                                   Simulation time: 0.000000000000e+00 sec


Writing pertinent data files ...
Leaving SIMPLIS.
```

1st pass unsuccessful

2nd pass successful

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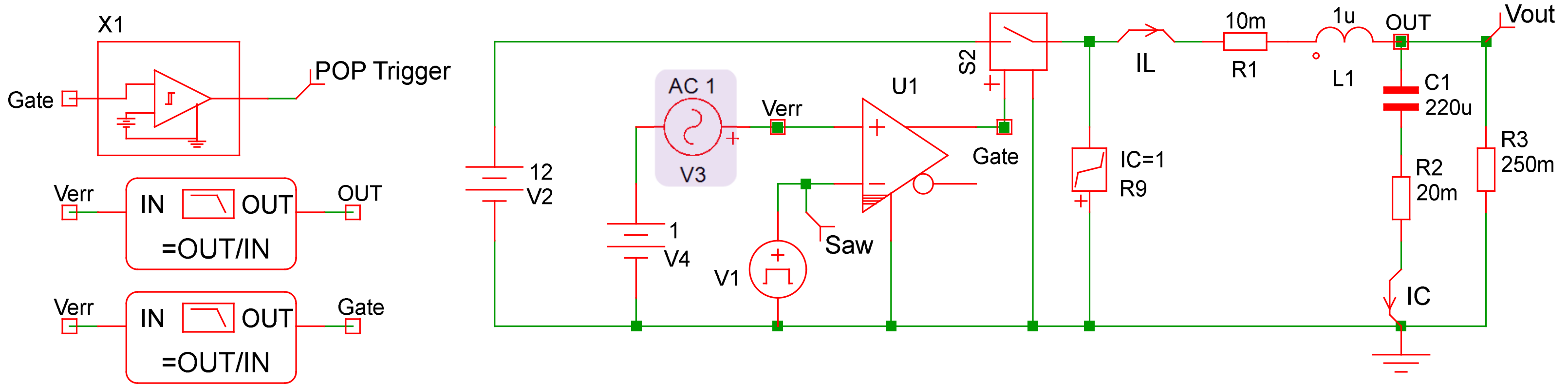
Running Small-Signal Analysis

- As long as a POP analysis is successful, small-signal analysis can be obtained
  - ✓ Obtain frequency response like control-to-output, or loop gain/phase in seconds
  - ✓ Work with all switching converters and those without an averaged model (LLC)

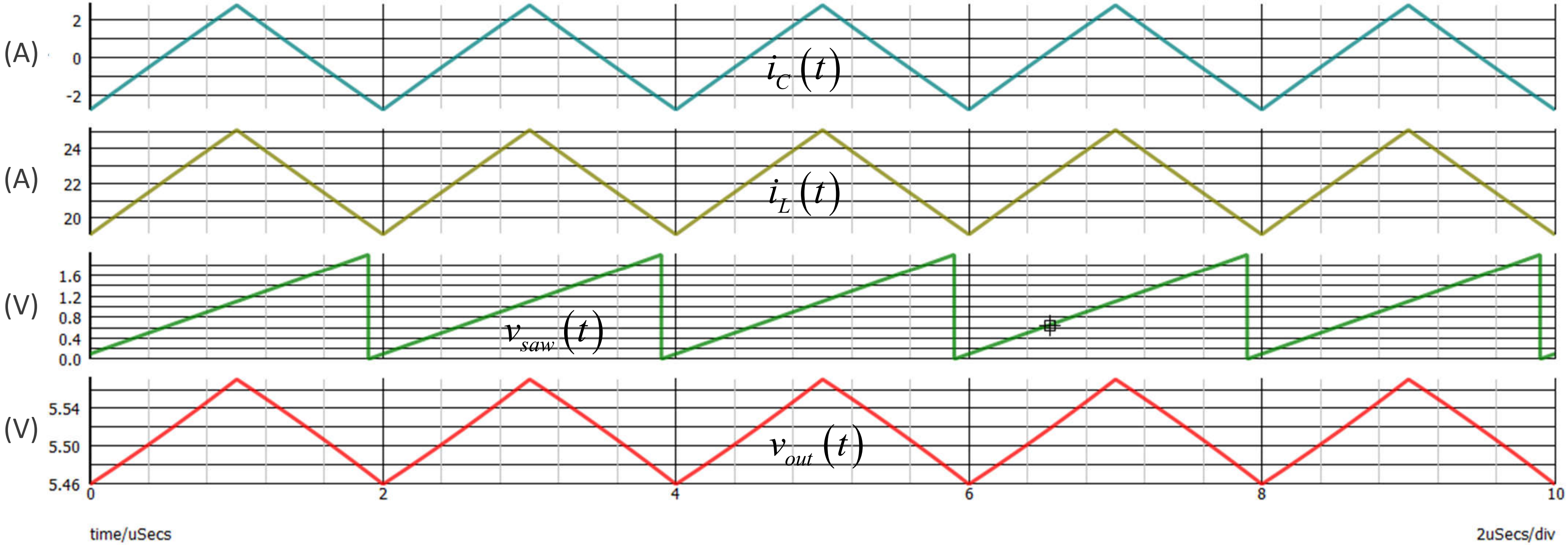


- A pulse-width modulator (PWM) is added to the sketch for duty ratio modulation
- Set source V_3 to 1 and SIMPLIS automatically controls its amplitude

The Steady-State Waveforms are First Obtained

- You can immediately verify that variables are within the expected range
- ✓ Measurements are available such as rms, average or peak values

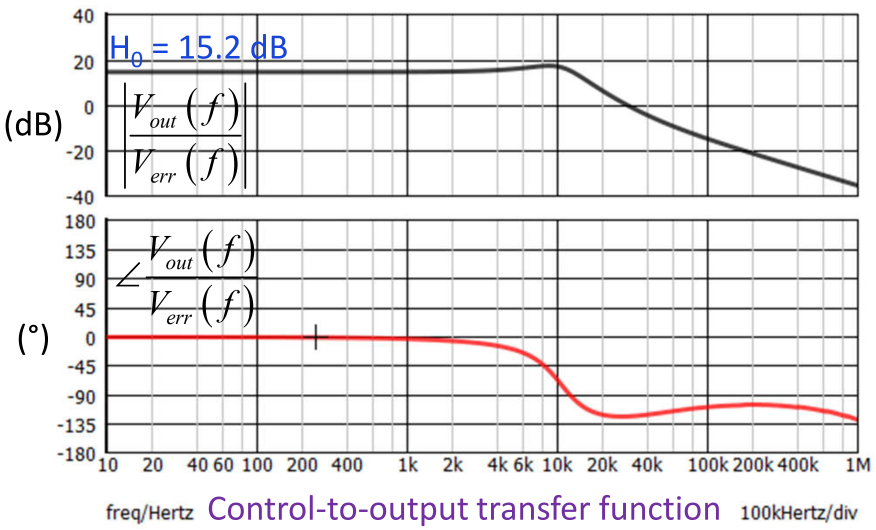
Curve label	Name	Value
IC	RMS/cycle	1.6176011A



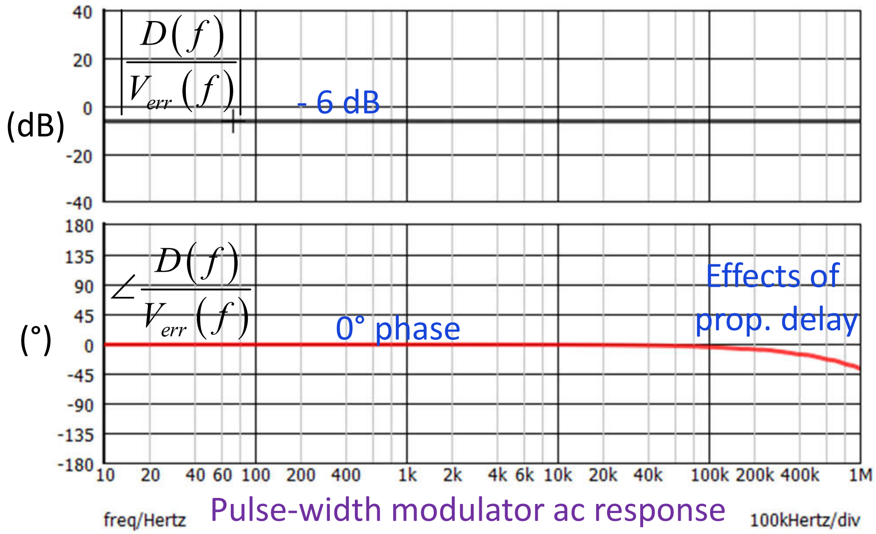
Power Stage Response is the First Step

- The Bode plot for the power stage is obtained in a fraction of seconds
- Same for the PWM section which shows the effects of the propagation delay

✓ The 100-ns pure delay makes the converter a non-minimum phase system



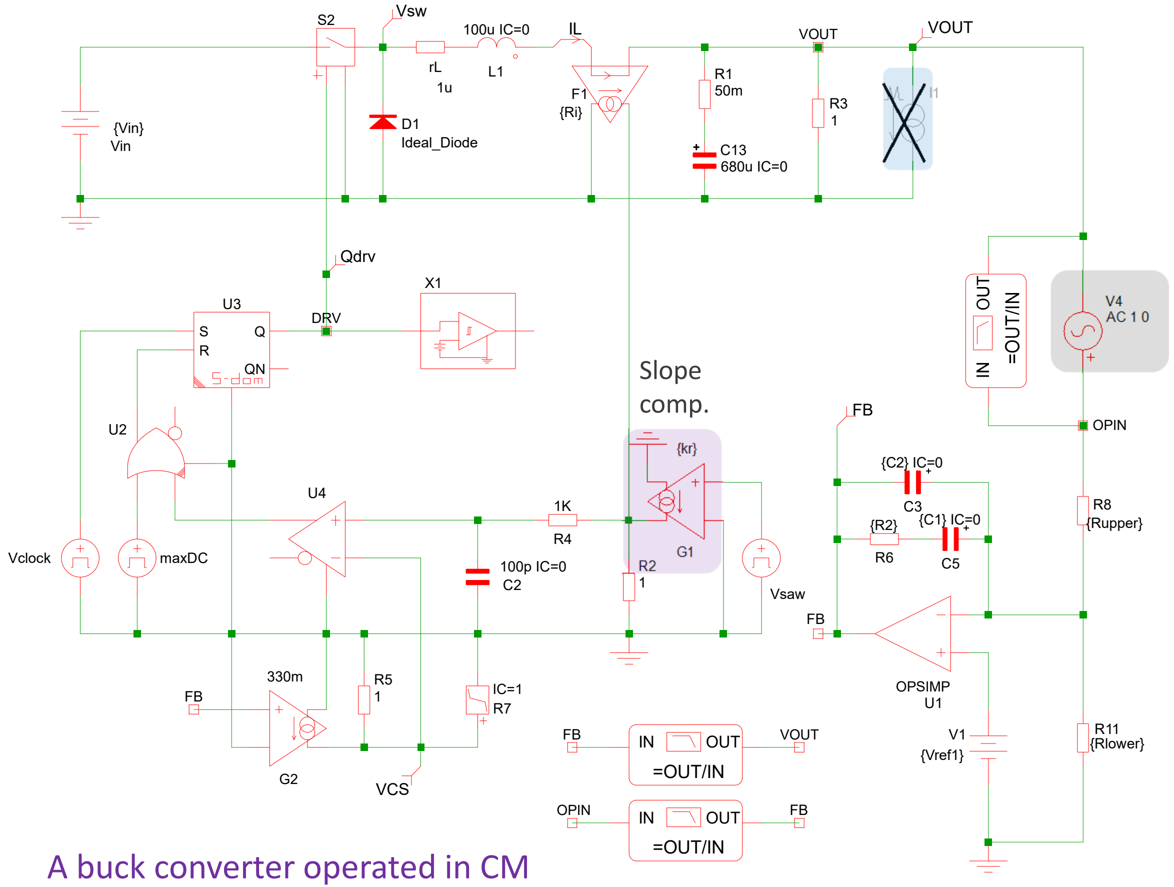
Control-to-output transfer function



Pulse-width modulator ac response

$$H_0 = 20\log\left(\frac{V_{in}}{V_p}\frac{R_L}{R_L + r_L}\right)$$

Closed-Loop Simulations



A buck converter operated in CM

- In the laboratory, it is difficult to physically open the loop especially in high-gain systems
- Perturbing the system while operating in closed-loop is the way to go

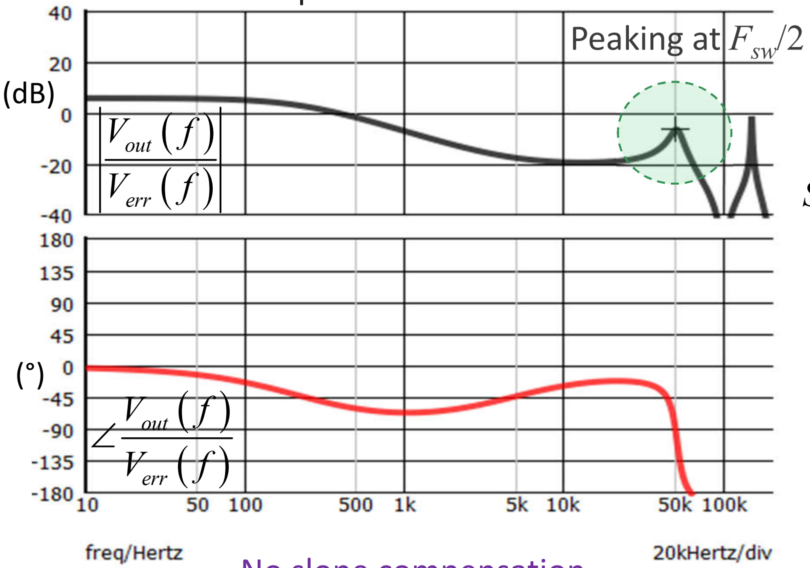
✓ The ac source is of fixed amplitude and does not need adjustment

✓ The same circuit can be used for ac or transient tests

Current Mode and Subharmonic Oscillations

- If the current loop is not properly compensated, instability at $F_{sw}/2$ can happen
- By reducing the gain of the inner current loop, oscillations can be tamed

Control-to-output transfer function



No slope compensation

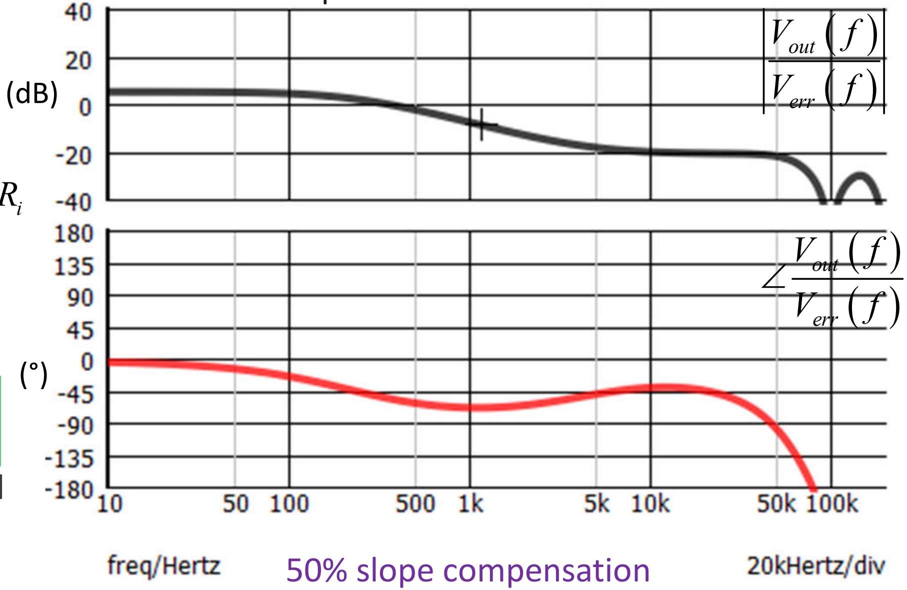
$m_c = 1$

$$S_n = \frac{V_{in} - V_{out}}{L} R_i$$

$$m_c = 1 + \frac{S_e}{S_n}$$

External ramp

Control-to-output transfer function



50% slope compensation

$m_c = 1.5$

Automatic Compensation is Possible

- It is possible to write macros automating components values calculations

➢ Read the power stage magnitude and phase at the selected crossover frequency

```
*
.VAR Vin=12
.VAR Vout=5
.VAR L=100u
.VAR Ri=160m
.VAR Ts=10u * please update clock and ramp generators *
*
.VAR Gfc=-20 * magnitude at crossover *
.VAR PS=-40 * phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.VAR fc=10k * targetted crossover *
.VAR PM=60 * choose phase margin at crossover *
*
.VAR Sn={((Vin-Vout)/L)*Ri}
.VAR Sramp={1/Ts}
.VAR mc=1.5 * set this value for ramp comp *
.VAR Se={(mc-1)*Sn}
.VAR kr={Se/Sramp}
*
```

Determine the amount of compensation

```
* Enter the Values for Vout and Bridge Bias Current *
*
.VAR Ibias=1m
.VAR Vref1=2.5
.VAR Rlower={Vref1/Ibias}
.VAR Rupper={(Vout-Vref1)/Ibias}
*
* Do not edit the below lines *
.VAR boost=PM-PS-90
.VAR G=10^(-Gfc/20)
.VAR fp=(tan(boost*pi/180)+sqrt((tan(boost*pi/180))^2+1))*fc
.VAR fz=fc^2/fp
.VAR a=sqrt((fc^2/fp^2)+1)
.VAR b=sqrt((fz^2/fc^2)+1)
.VAR R2=((a/b)*G*Rupper*fp)/(fp-fz)
.VAR C1=1/(2*pi*R2*fz)
.VAR C2=C1/(C1*R2*2*pi*fp-1)
*
```

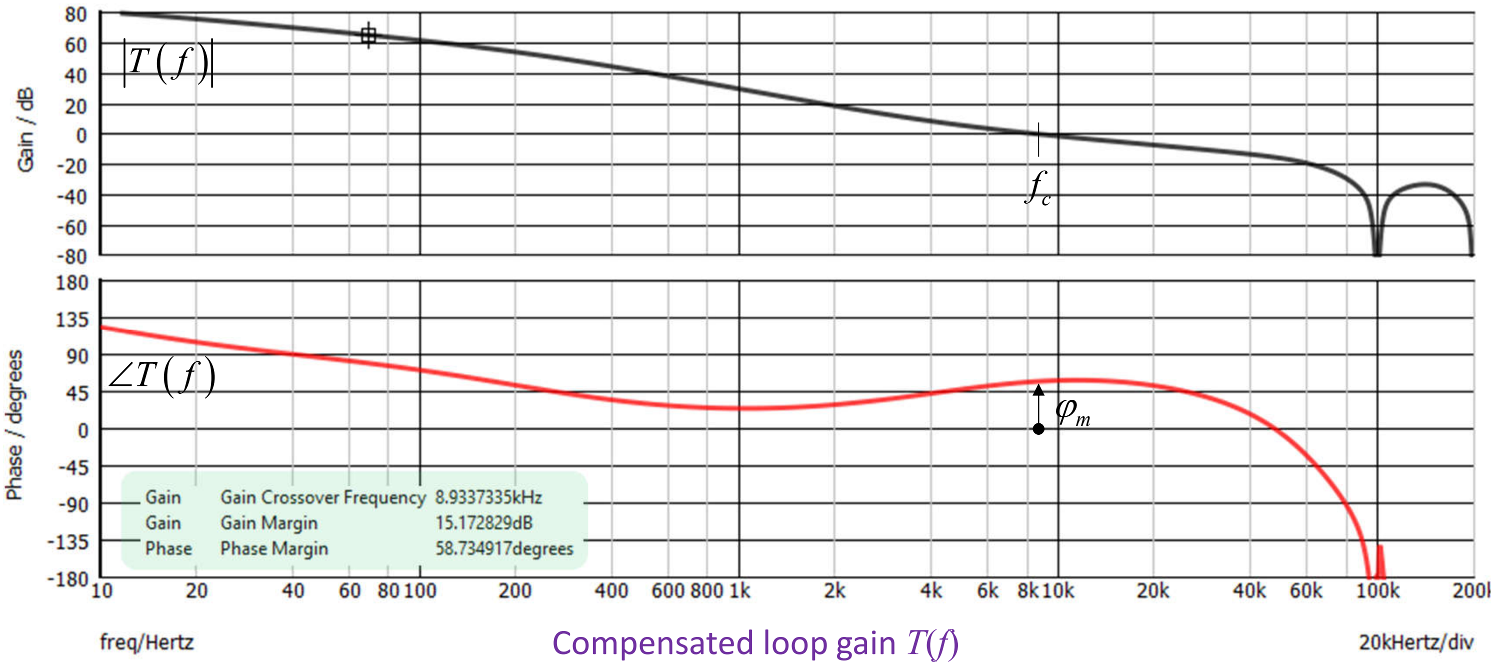
Pole-zero calculation

```
*
{'*'}
{'*'}
{'*'} Rupper = {Rupper}
{'*'} Rlower = {Rlower}
{'*'} R2 = {R2}
{'*'} C2 = {C2}
{'*'} C1 = {C1}
{'*'} Boost = {boost}
{'*'} Fz = {Fz}
{'*'} Fp = {Fp}
{'*'} Sn = {Sn}
{'*'} Se = {Se}
{'*'} kr = {kr}
{'*'}
```

Display values
In the netlist

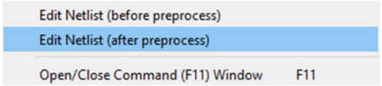
Meeting the Right Crossover in a few Seconds

- SIMPLIS calculates the compensation values based on the adopted strategy
- It is then easy to explore other approaches with different crossover, margins etc.



Compensated loop gain $T(f)$

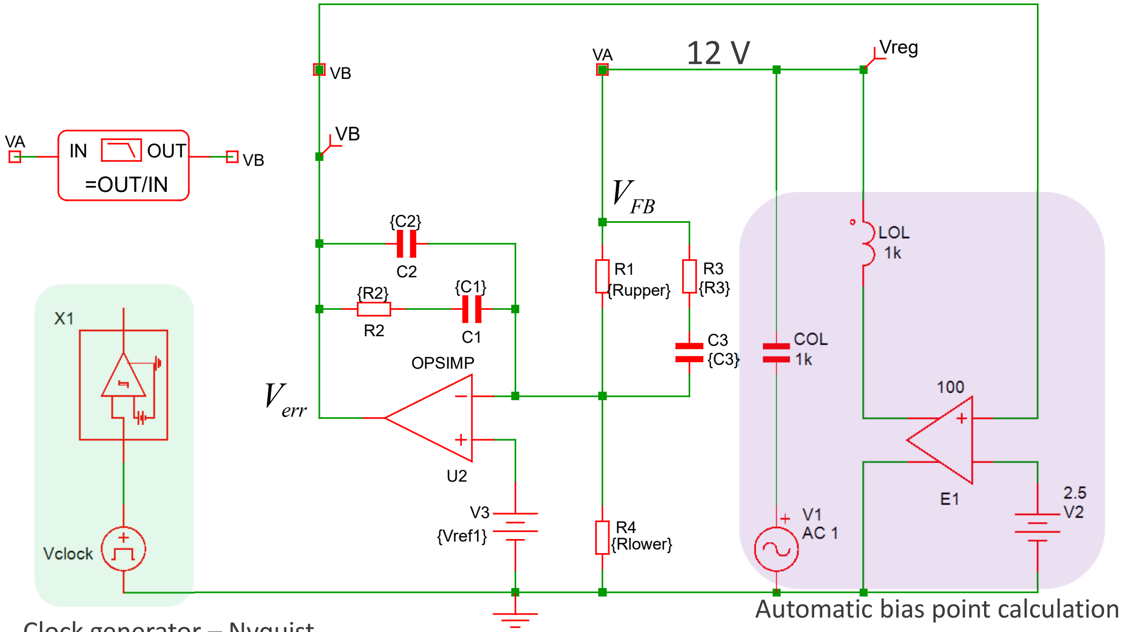
Simulator menu




```
*
* Rupper = 2500
* Rlower = 2500
* R2 = 84484.6310392954
* C2 = 5.34187416193801e-10
* C1 = 2.24506484641772e-10
* Boost = 10
* Fz = 8390.9963117728
* Fp = 11917.5359259421
* Sn = 11200
* Se = 5600
* kr = 0.056
*
```

SIMPLIS is a Time-Domain Simulator

- With a clock source, cheat SIMPLIS and obtain ac-response of non-switching circuits
- A typical application is an automated compensator



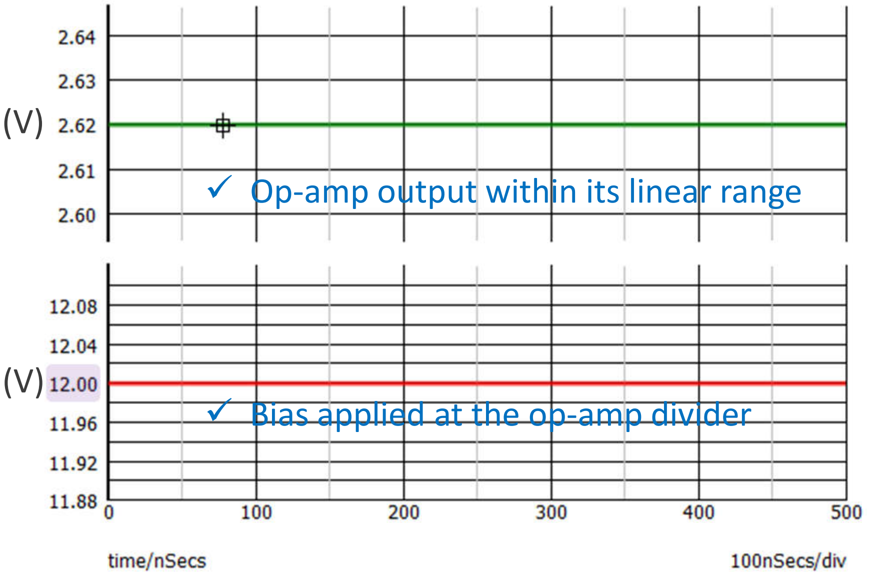
Automatic bias point calculation

Clock generator – Nyquist criterion applies

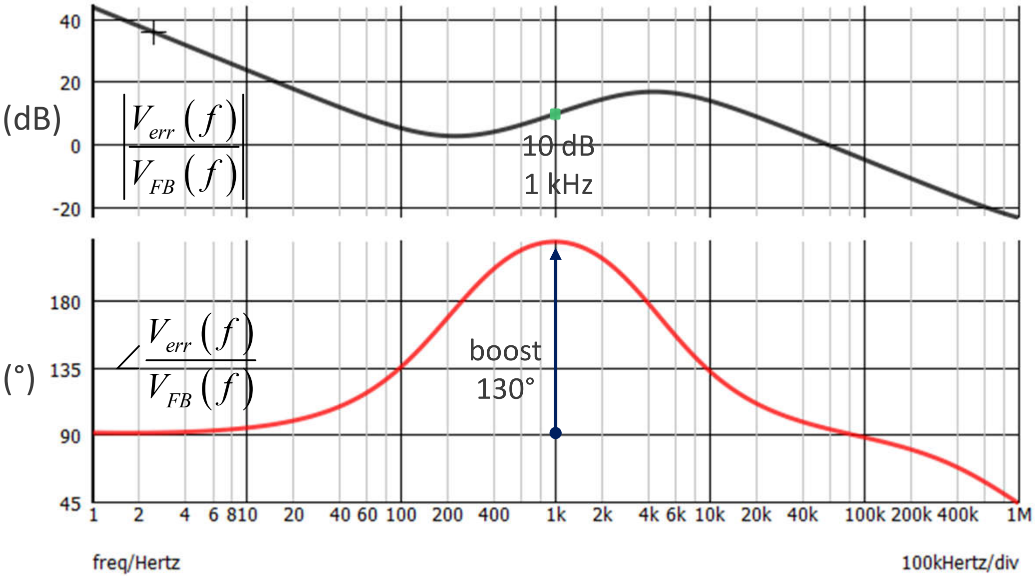
```
.VAR Gfc=-10 * magnitude at crossover *
.VAR PS=-150 * phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.VAR fc=1k * targeted crossover *
.VAR PM=70 * choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.VAR Vout=12
.VAR Ibias=2m
.VAR Vref1=2.5
.VAR Rlower=Vref1/Ibias
.VAR Rupper=(Vout-Vref1)/Ibias
*
* Do not edit the below lines *
.VAR boost=PM-PS-90
.VAR Kf=(tan((boost/4+45)*pi/180))^2
.VAR fz1=fc/sqrt(Kf)
.VAR fz2=fc/sqrt(Kf)
.VAR fp1=fc*sqrt(Kf)
.VAR fp2=fc*sqrt(Kf)
*
.VAR G=10^(-Gfc/20)
.VAR a=sqrt((fc^2/fp1^2)+1)
.VAR b=sqrt((fc^2/fp2^2)+1)
.VAR c=sqrt((fz1^2/fc^2)+1)
.VAR d=sqrt((fc^2/fz2^2)+1)
.VAR R2=((a*b/(c*d))/(fp1-fz1))*Rupper*G*fp1
.VAR C1=1/(2*pi*fz1*R2)
.VAR C2=C1/(C1*R2*2*pi*fp1-1)
.VAR C3=(fp2-fz2)/(2*pi*Rupper*fp2*fz2)
.VAR R3=Rupper*fz2/(fp2-fz2)
.VAR G0=((R2*C1)/(Rupper*(C1+C2)))*c*d/(a*b)  * Gain at fc sanity check *
*
```

Confirming Bias Point and Frequency Response

- The simulation confirms the applied voltage for regulation is 12 V
- Frequency response shows the wanted 10-dB gain at 1 kHz



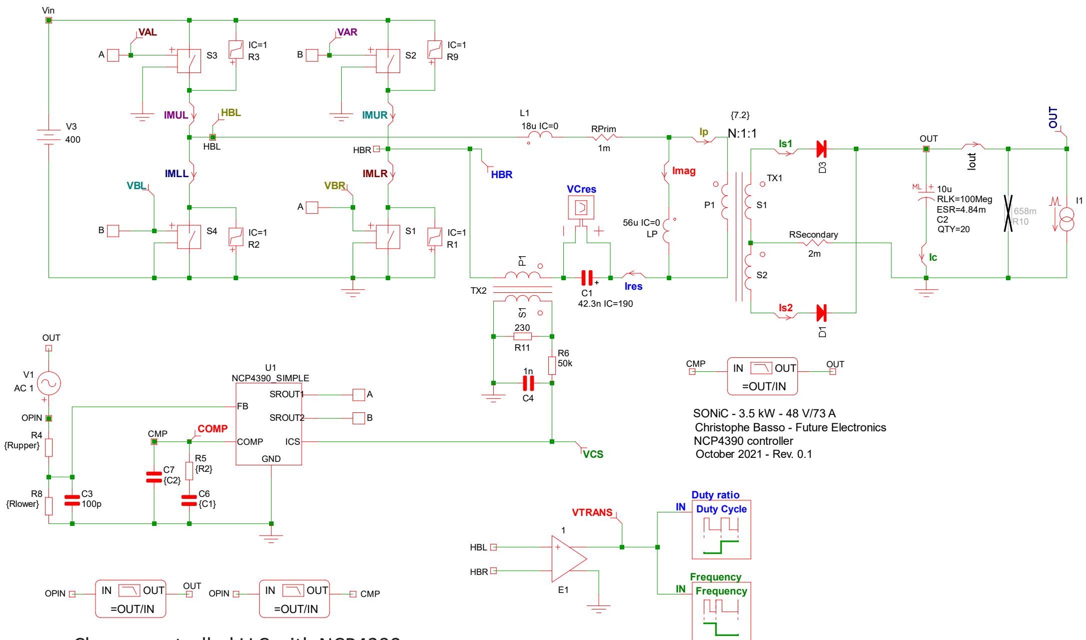
Dc value confirming the 12-V target



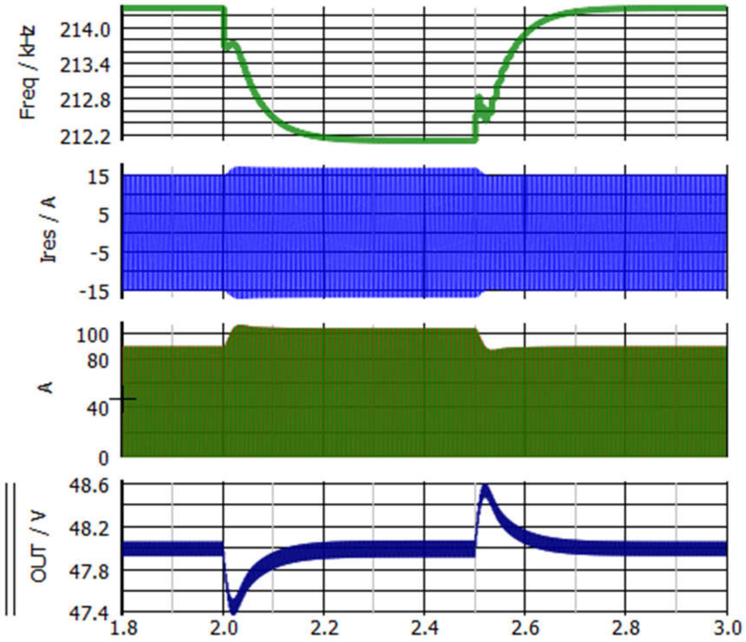
Compensator response

Explore Complicated Converters

- Any converter can be simulated to determine the control-to-output transfer function
- Start with a simple circuit for which the POP is easily obtained
- ✓ Then add more comprehensive models to see 2^{nd}- and 3^{rd}-order effects

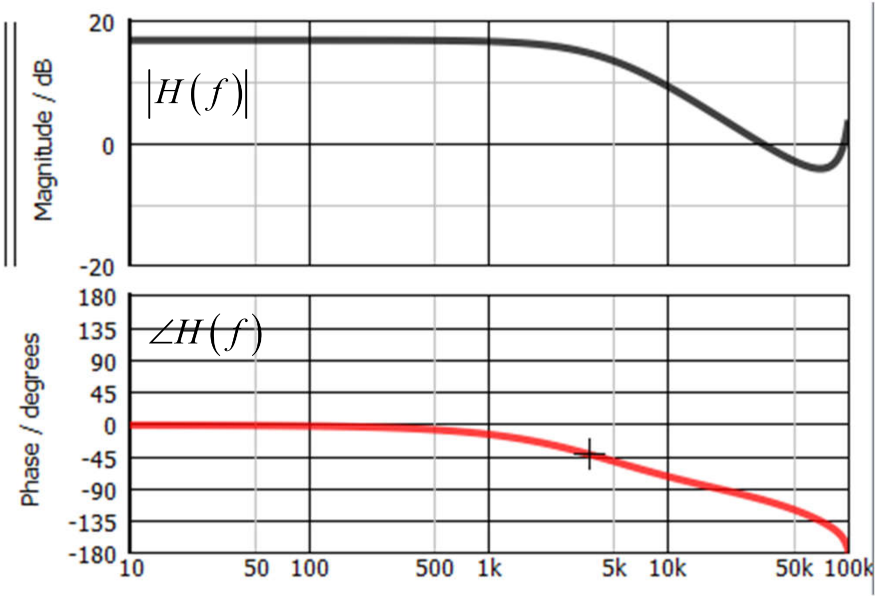


Charge-controlled LLC with NCP4390

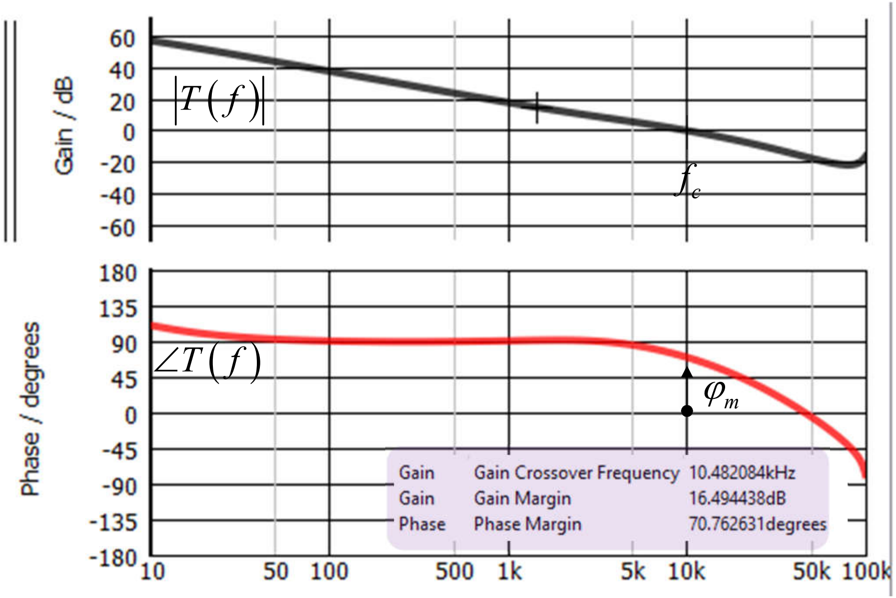


Obtain the Transfer Function Instantly

- Any converter can be simulated to determine the control-to-output transfer function
- Start with a simple circuit for which the POP is easily obtained
- ✓ Then add more comprehensive models to see 2nd- and 3rd-order effects



Power stage small-signal response



Compensated loop gain (10 kHz f_c)

Agenda

- SPICE and Power Converters
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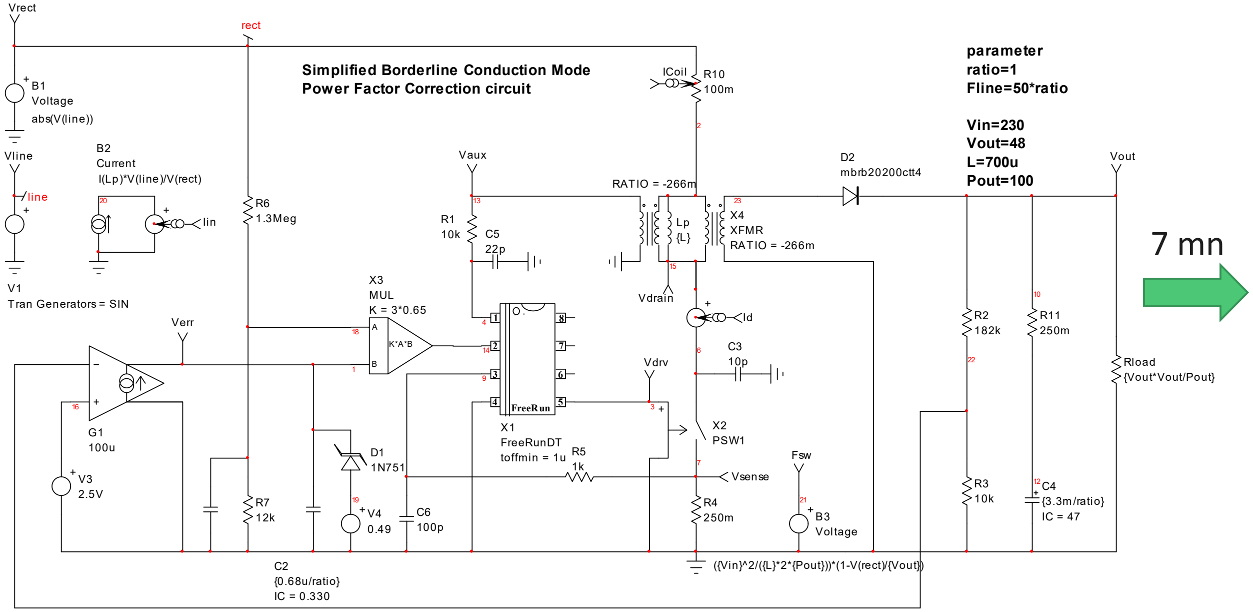
- Monte Carlo Analysis
- Design Example of a Flyback Converter

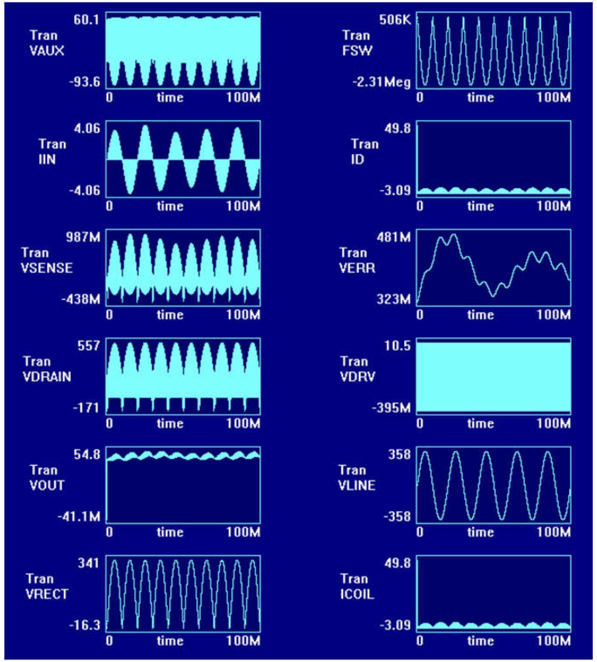
Power Factor Correction

- Power factor correction simulation places a heavy burden on computers
- High-frequency events spread across several tens of mains cycles imply simulation power
- SPICE users simulate only a small portion of the operations



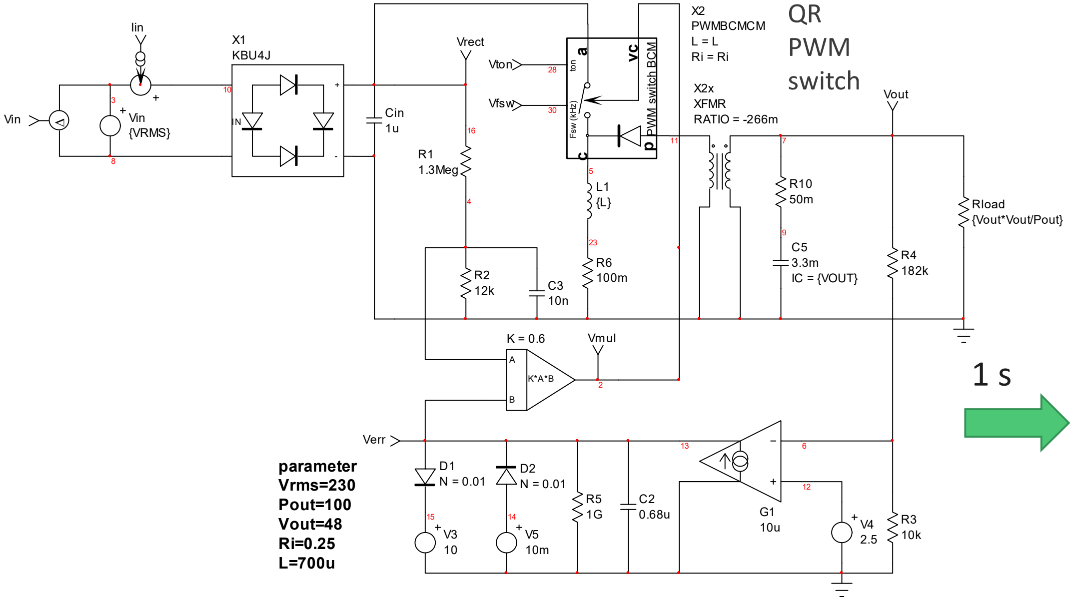
48-V/100-W single-stage QR flyback converter

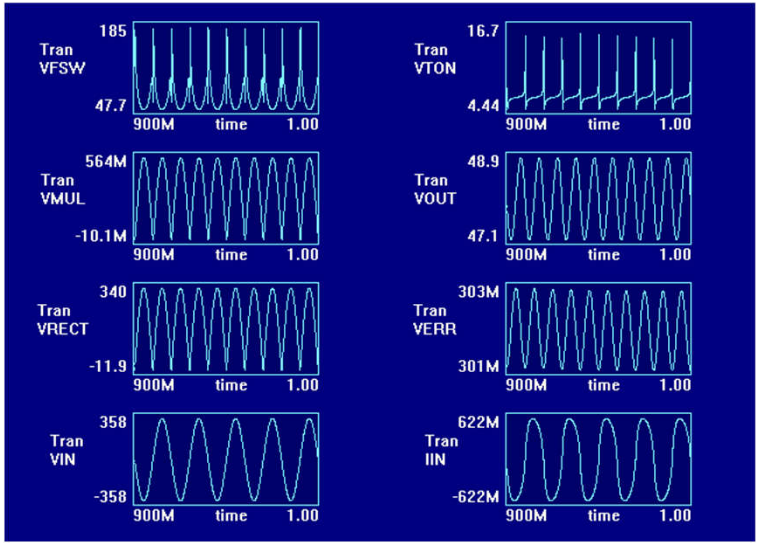
7 mn



Averaged Model Alternative

- Averaged models are an alternative for transient and ac analyses
- The switching component has disappeared and they simulates fast
- ➢ Convergence issues are likely to appear depending on model robustness

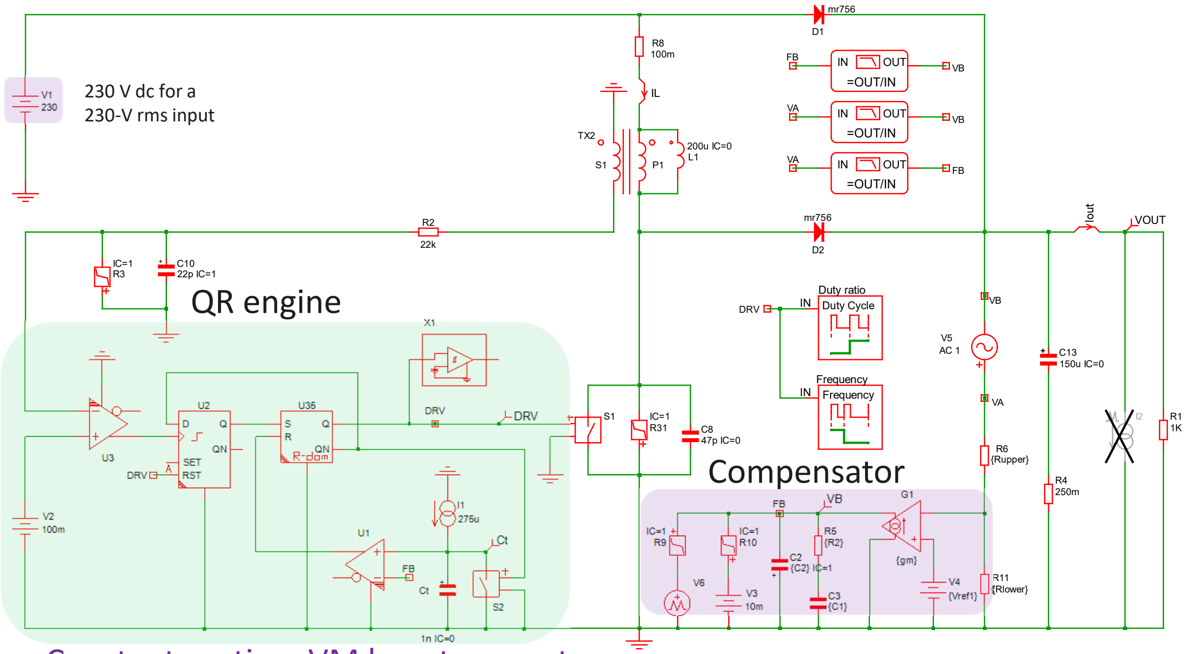




Averaged model of the single-stage QR flyback converter

Cycle-by-Cycle Simulations with SIMPLIS

- SIMPLIS lets you examine the frequency response using a fixed dc bias
- This dc level equals the rms value of the input voltage, e.g. 230 V dc for a 230-V_{ac} input
- You can test the operating point and obtain the small-signal response in a few seconds



Constant on-time VM boost converter

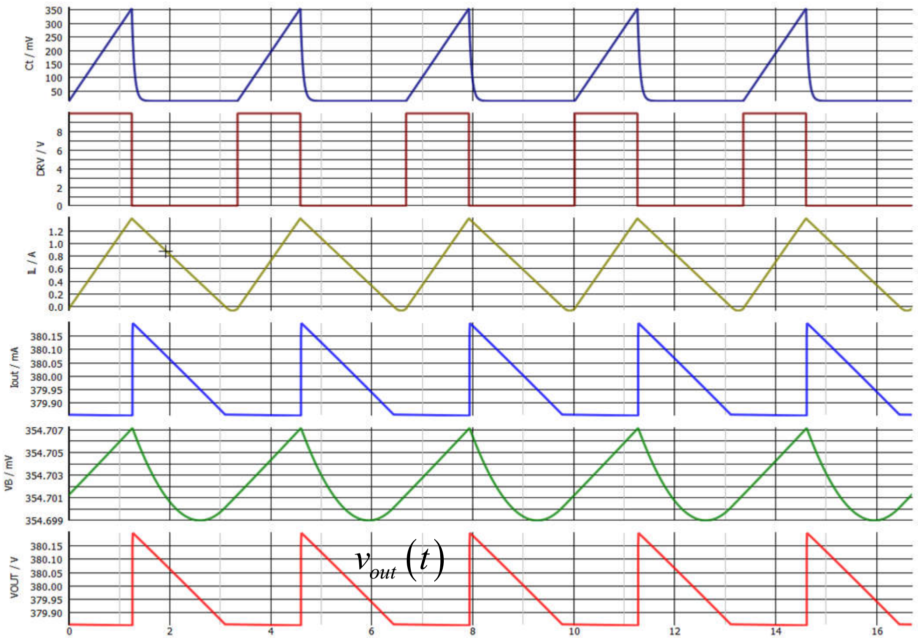
✓ Works for operating point determination

✓ Can give the small-signal response of the control-to-output transfer function

✓ Simulates in 1 s!

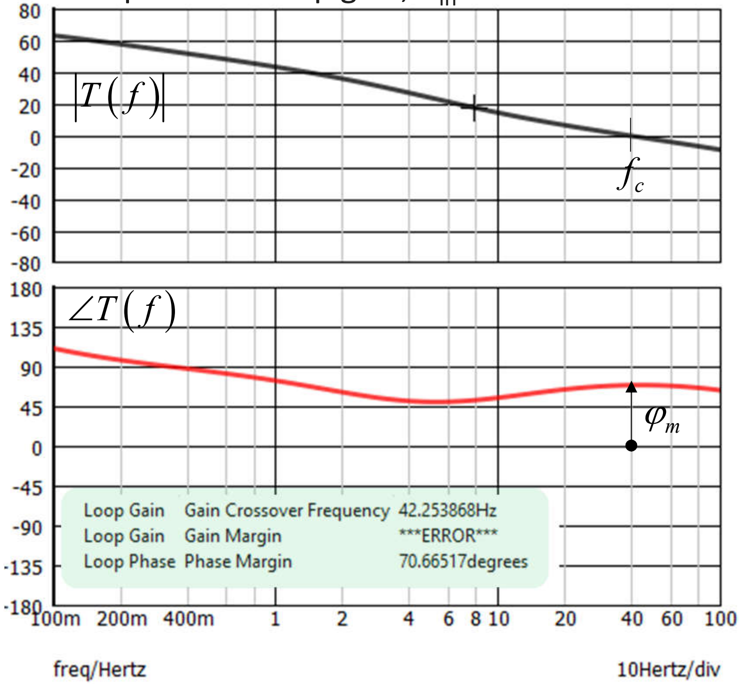
Operating Point and Ac Response

- The operating point lets you check that the converter regulates properly
- The POP process works fine with the dc input but would fail with a sinewave input
  - ➢ Use multi-tone ac analysis instead



POP of the CrM boost converter

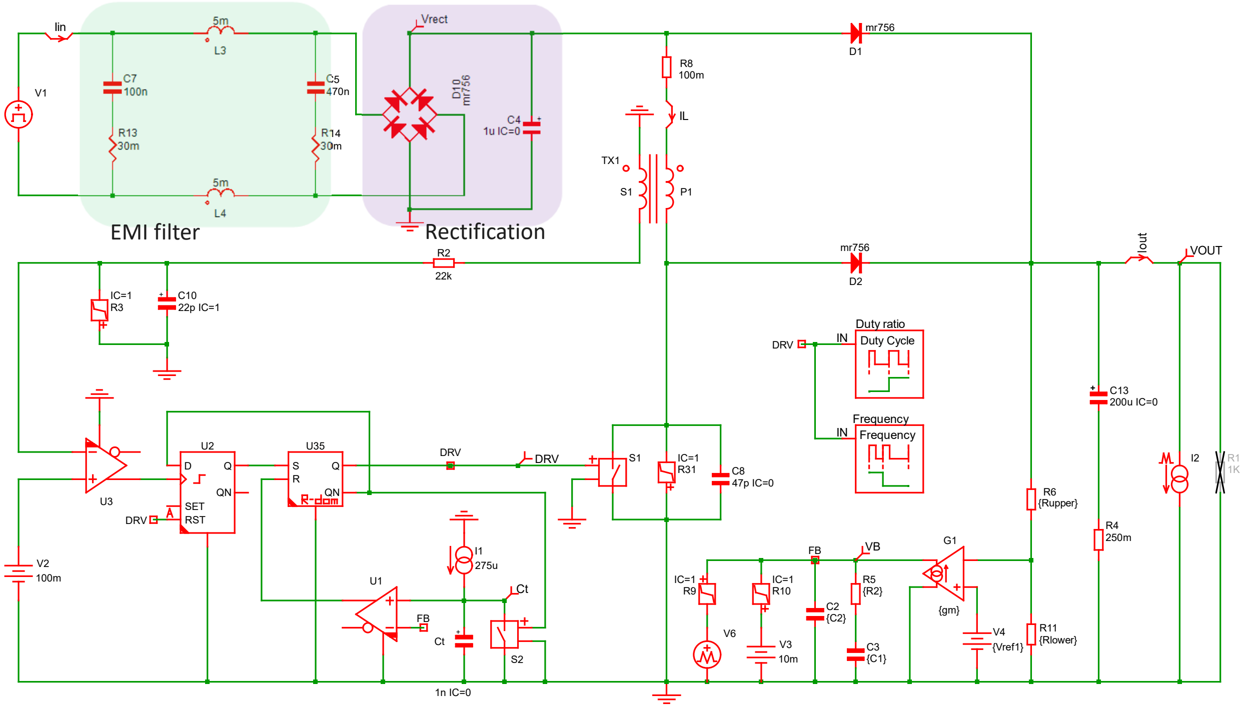
Compensated loop gain, V_{in} = 230 V



Transient Simulations

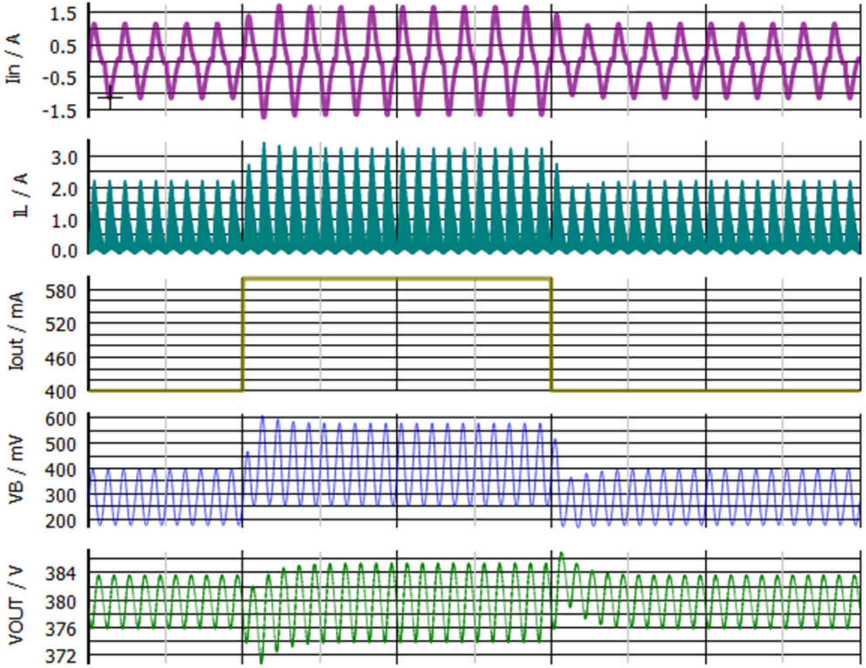
- With a sinusoidal input you can run simulations in the long range
- ✓ Check input current distortion and transient response in different conditions

Ac source

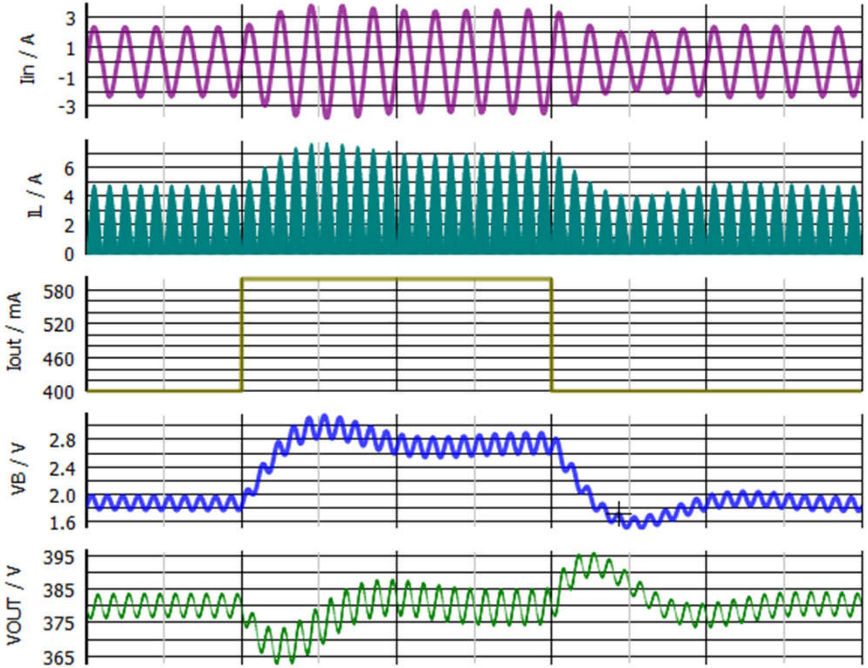


Dynamic Performance

- The transient response can be quickly assessed at low- and high-line input voltages
- The available granularity allows you to zoom-in and precisely look at switching events



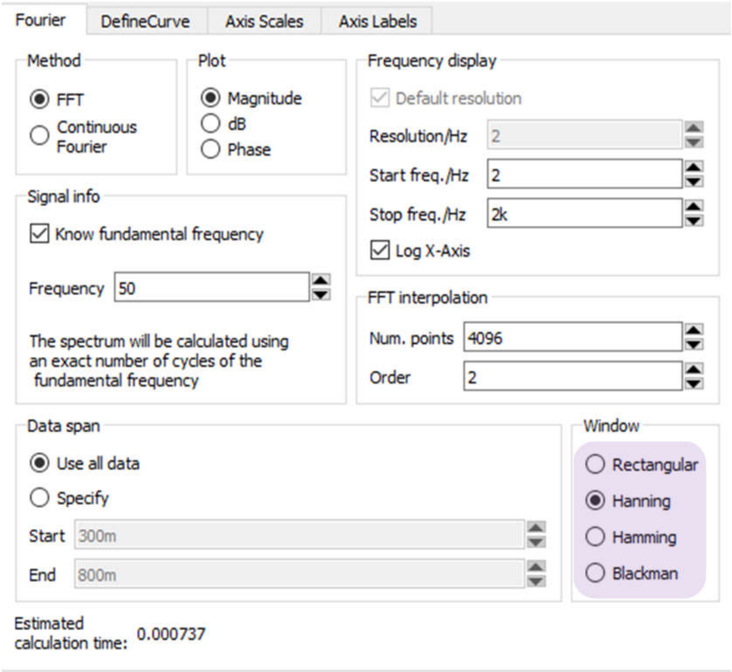
200-mA load step at V_{in} = 265 V rms

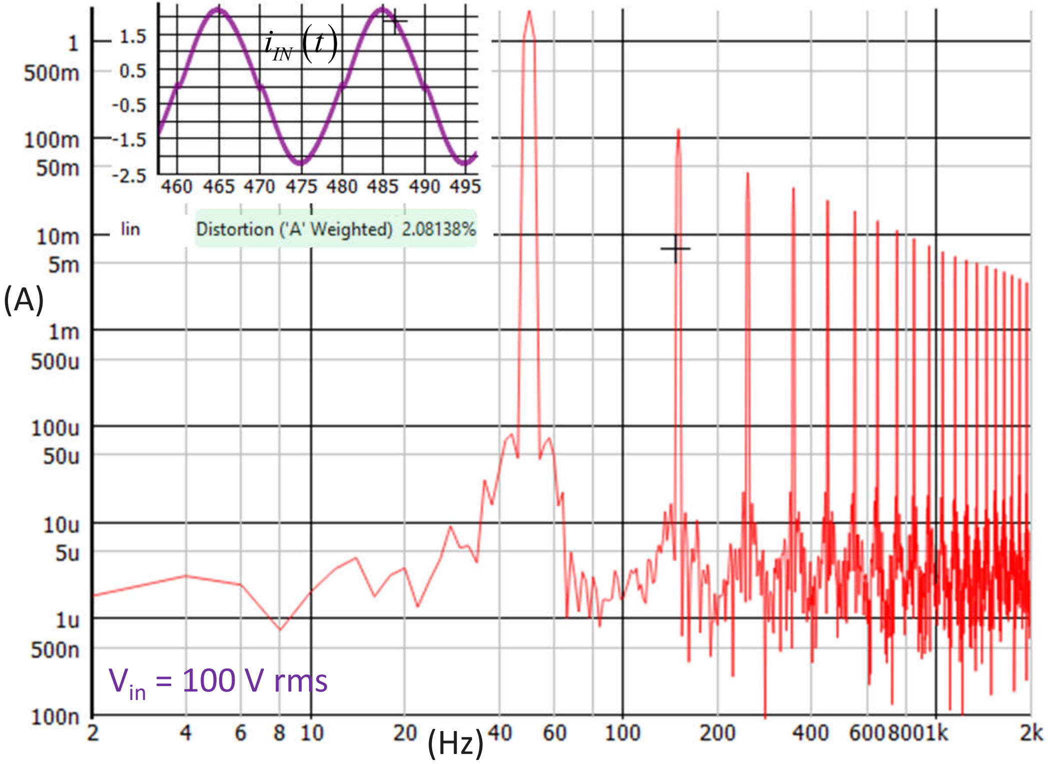


200-mA load step at V_{in} = 100 V rms

Explore Distortion and Harmonic Limits

- SIMPLIS lets you interpolate data and choose different apodization windows
- You can also easily evaluate the input current distortion





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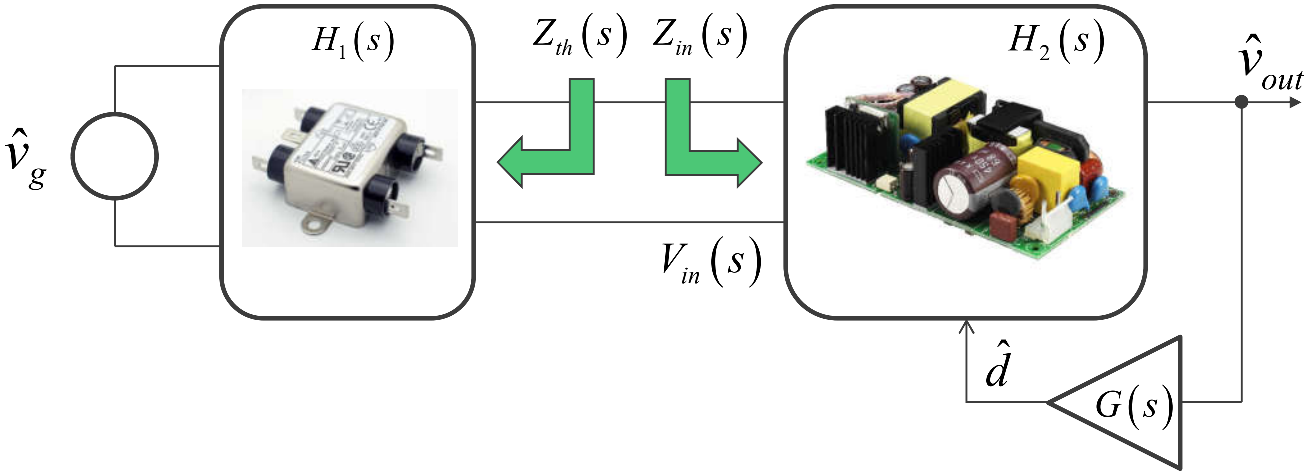
Impedance Association

- A converter fed by an EMI filter will see its transfer functions affected:
- ✓ The control-to-output transfer function can have degraded margins
- ✓ The output impedance of the converter can be significantly changed
- ➢ Always confirm stability is not at stake when the filter is installed

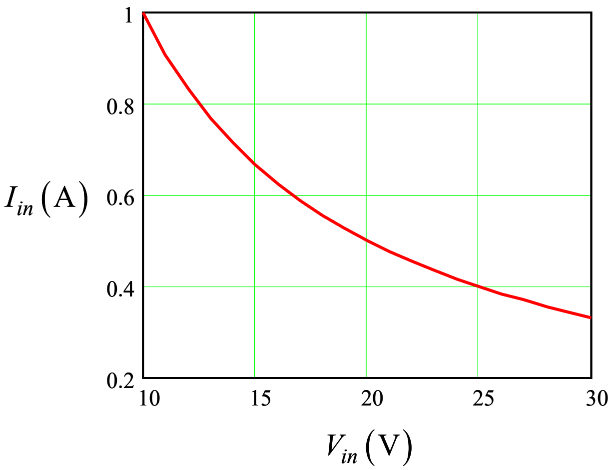


A Negative Resistance

- The *incremental* or *small-signal* resistance of a closed-loop converter is negative
- When associated with an EMI filter, a mechanism for oscillations exists
- Considering a 100%-efficient converter, we have: $P_{out} = P_{in} \longrightarrow I_{in}V_{in} = I_{out}V_{out}$
- In closed-loop operations, P_{out} is constant, no link to V_{in}

Infinite rejection

$$\longrightarrow \quad I_{in}\left(V_{in}\right) = \frac{P_{out}}{V_{in}}$$



Calculate slope

$$\frac{dI_{in}\left(V_{in}\right)}{dV_{in}} = \frac{d\left(\frac{P_{out}}{V_{in}}\right)}{dV_{in}} = -\frac{P_{out}}{V_{in}{}^{2}}$$

The incremental input resistance is negative

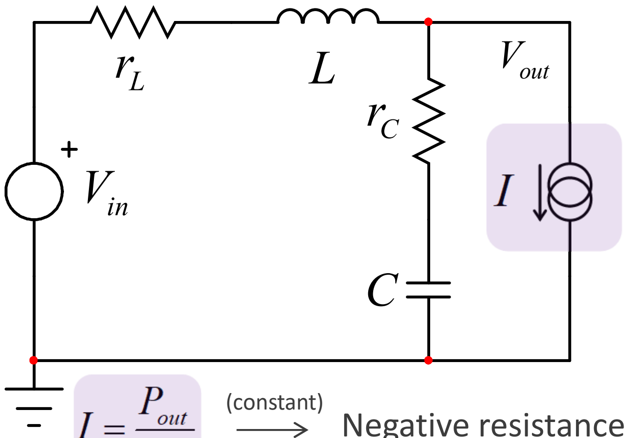
$$\boxed{R_{in} = -\frac{V_{in}{}^{2}}{P_{out}}}$$

A Simple Example

- Losses in the EMI filter are illustrated by a damping ratio ζ or a quality factor Q
- If losses are exactly compensated by a negative resistance, you built an oscillator

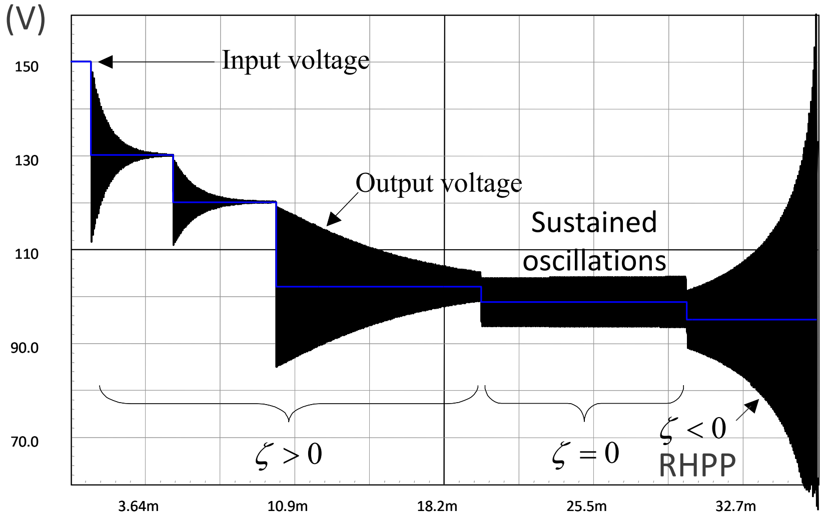
$$H(s) = H_0 \frac{1 + s/\omega_z}{\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1} \qquad Q = \frac{1}{2\boxed{\zeta}}$$

→ If ohmic losses are gone, the damping ratio is zero, Q is infinite.



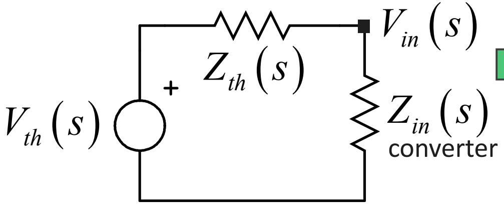
$I = \frac{P_{out}}{V_{out}}$ (constant) → Negative resistance

Infinite bandwidth

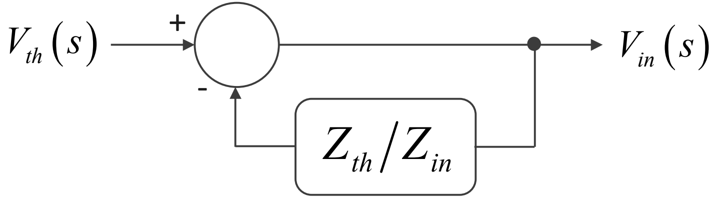


Conditions for Stability

- The front-end filter and the downstream converter can be modeled with a minor loop
- This loop reflects the action of an impedance divider



$$V_{in}(s)=V_{th}(s)\frac{1}{1+\underbrace{\boxed{\frac{Z_{th}(s)}{Z_{in}(s)}}}_{\text{gain}}}$$



- In this particular arrangement, the Nyquist criterion applies for stability assessment

$$V_{in}(s)=V_{th}(s)\frac{1}{1+\frac{Z_{th}(s)}{Z_{in}(s)}}$$

$$\frac{Z_{th}(s)}{Z_{in}(s)}=-1$$

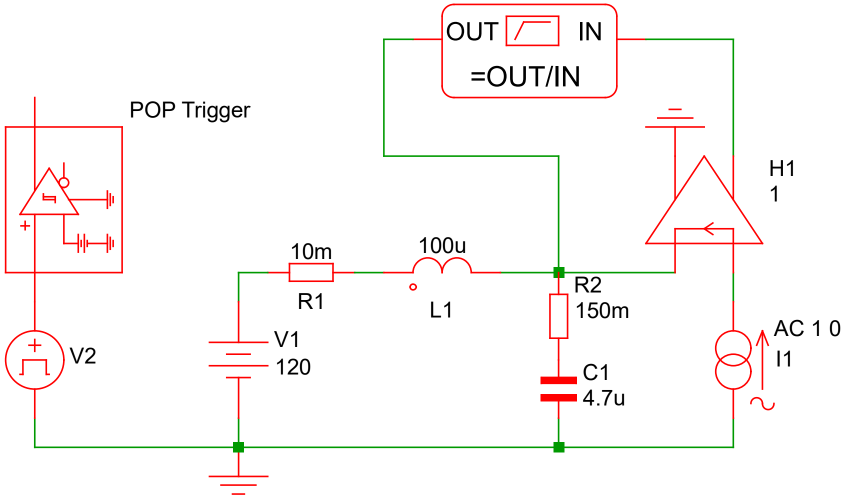
$$\left|\frac{Z_{th}(s)}{Z_{in}(s)}\right|=1 \text{ and } \angle\frac{Z_{th}(s)}{Z_{in}(s)}=-180°$$

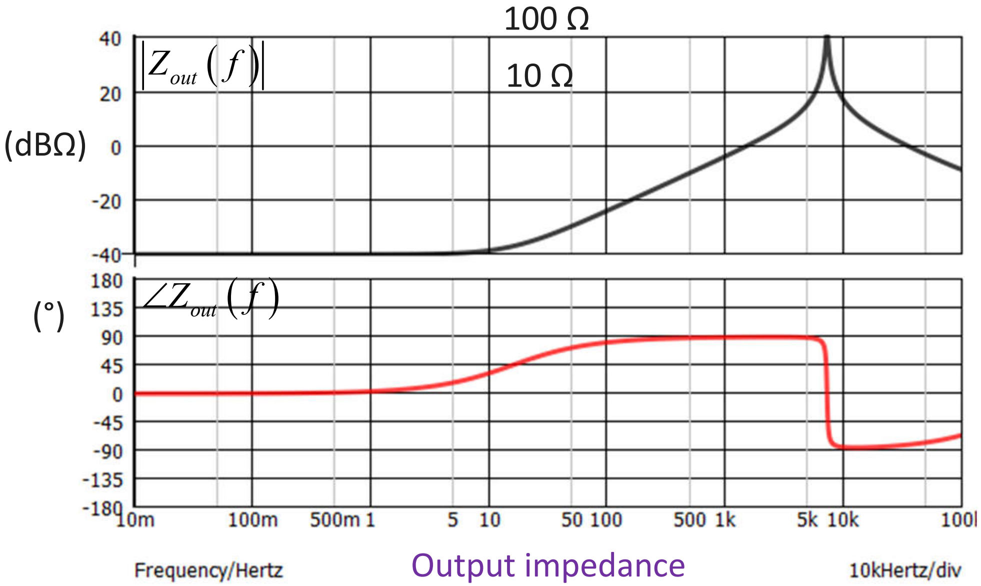
Conditions for oscillations

R. D. Middlebrook, *Input Filter Considerations in Design and Application of Switching Regulators*, IEEE Proceedings, 1976

Simulating an Output Impedance

- Once the EMI filter has been determined, you must plot its output impedance
  - ✓ Check the presence of peaks in the transfer function
  - ✓ Calculate the necessary damping in case of too high a peaking

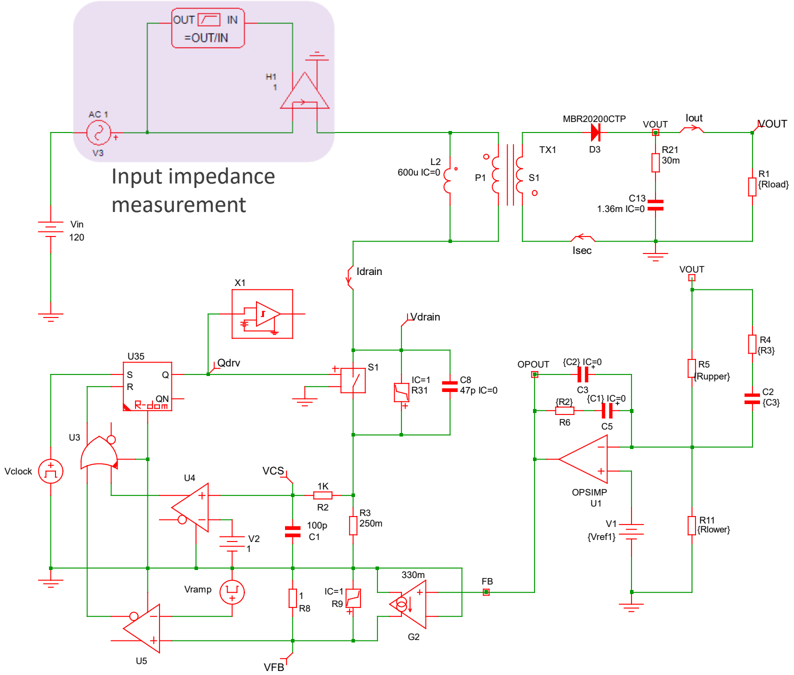


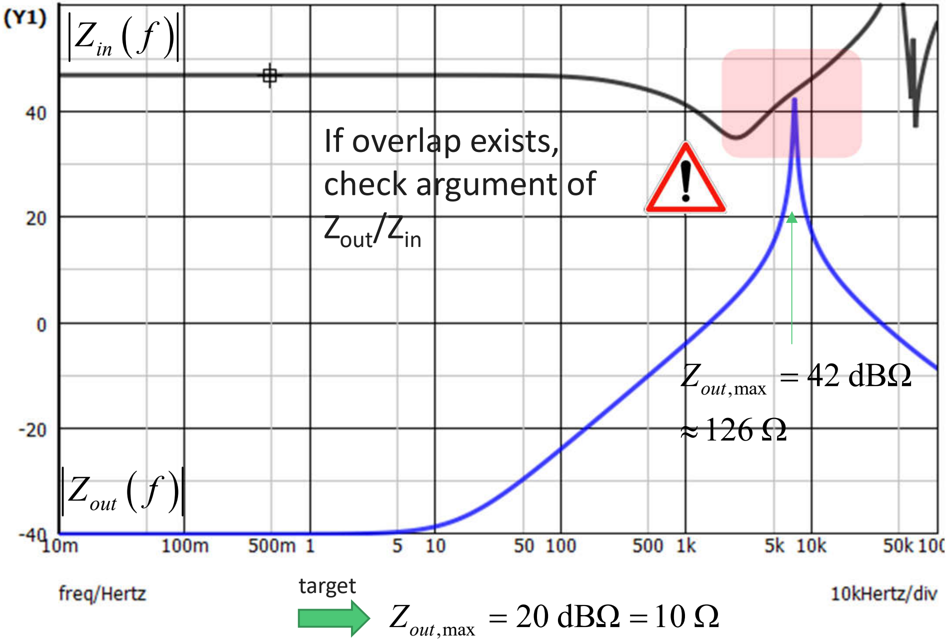


Output impedance magnitude and phase

Simulate the Closed-Loop Input Impedance

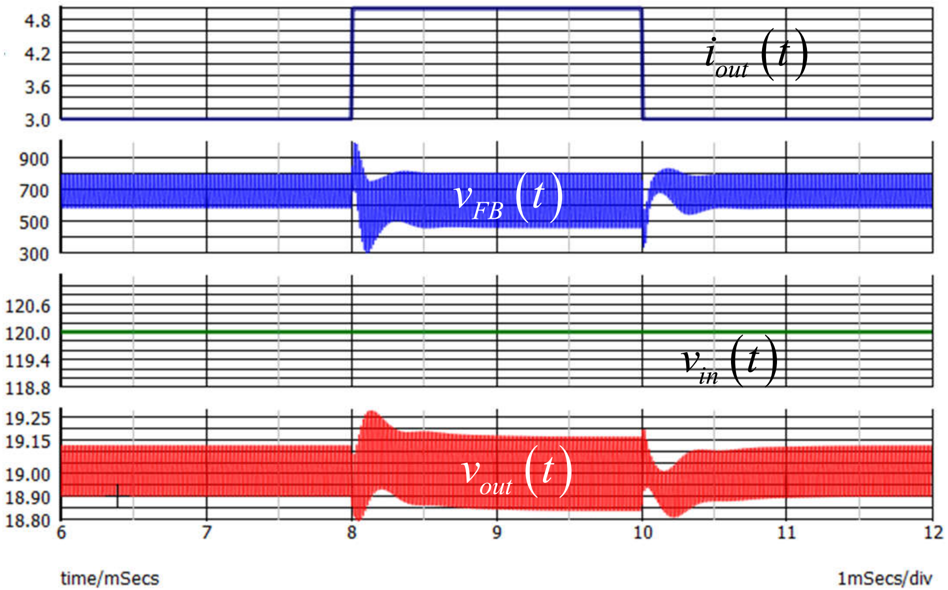
- You must now check the input impedance of the converter once stabilized
- Identify the overlap areas and check if sufficient margins exist
- ➢ If margins are too thin or if overlaps exist, filter damping is mandatory



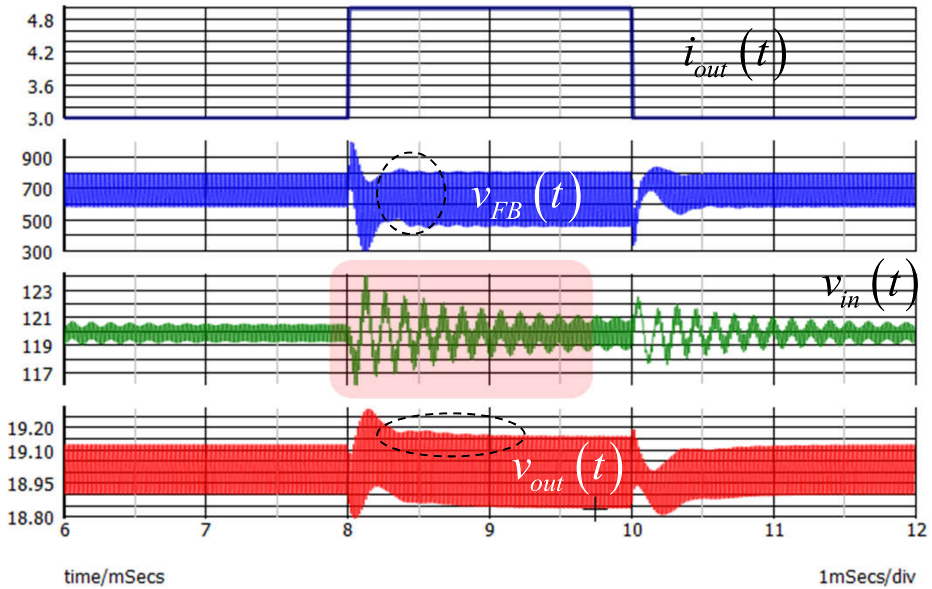


Check Input Voltage in Load Step

- Once the filter is installed, check the transient response to see the effects
- With current-mode control, oscillations may be observed on the input rail



Transient response without EMI filter



Transient response with EMI filter

Optimally Damping the Filter

- It is possible to show that an optimal RC damper exists to reduce the peaking
- Determine the values of R and C to meet a maximum peak of 20 dBΩ or 10 Ω

➢ Based on R.D. Middlebrook method, R = 6 Ω and C = 5.45 µF

Optimal damping calculations

$Z_{0mm} := 10\Omega$ target

$$R_0 := \sqrt{\frac{L_1}{C_3}} = 4.613\Omega$$

$$\frac{Z_{0mm}}{R_0} = \sqrt{\frac{2\cdot(2+n)}{n^2}}$$

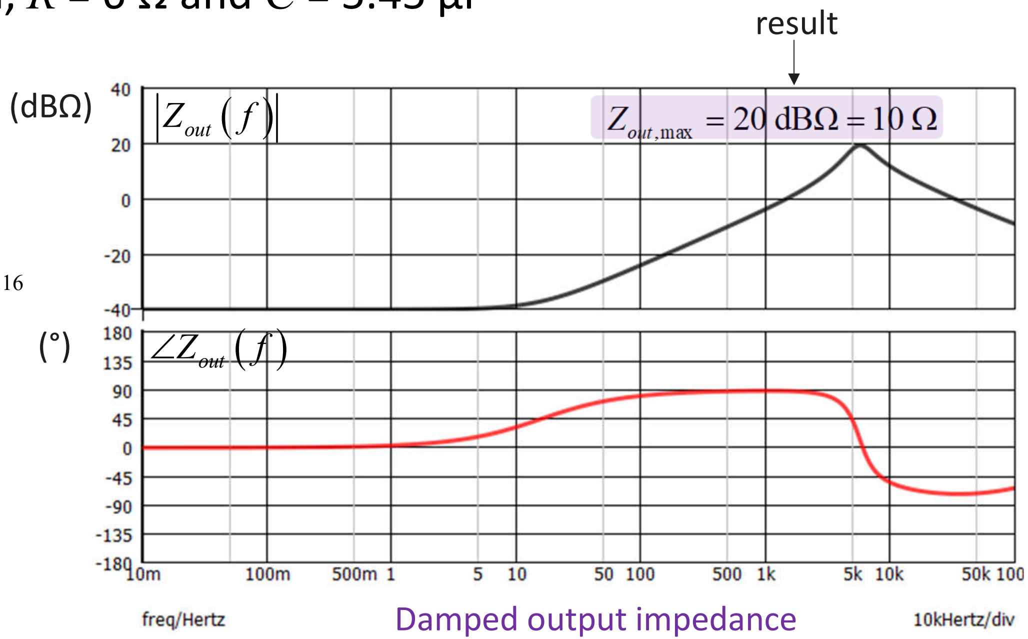
$$n := \frac{R_0\cdot\left(R_0 + \sqrt{R_0^{\,2} + 4\cdot Z_{0mm}^{\,2}}\right)}{Z_{0mm}^{\,2}} = 1.16$$

$$Q_{opt} := \sqrt{\frac{(4+3\cdot n)(2+n)}{2\cdot n^2\cdot(4+n)}} = 1.305$$

$$C_{damp} := C_3\cdot n = 5.45\cdot\mu F$$

$$R_{damp} := R_0\cdot Q_{opt} = 6.02\Omega$$

✓ Rather than determining R alone and making C 10x the EMI cap., determine the optimal RC couple to meet the wanted peak

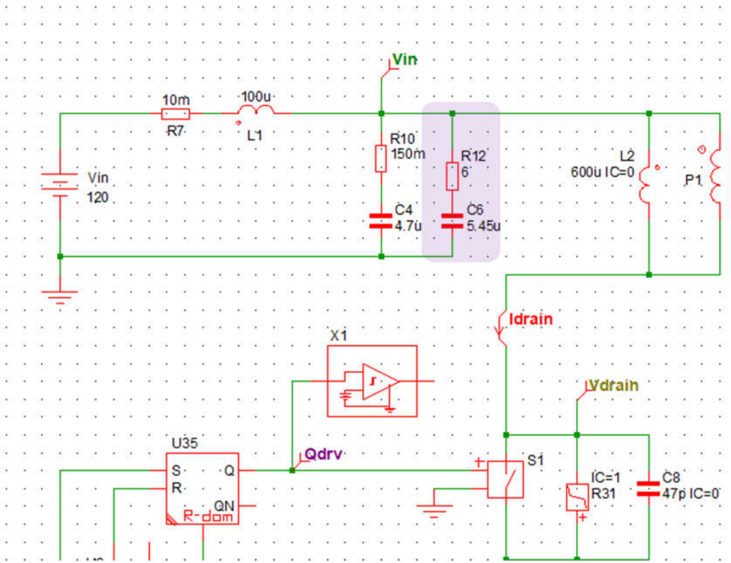


Damped output impedance magnitude and phase

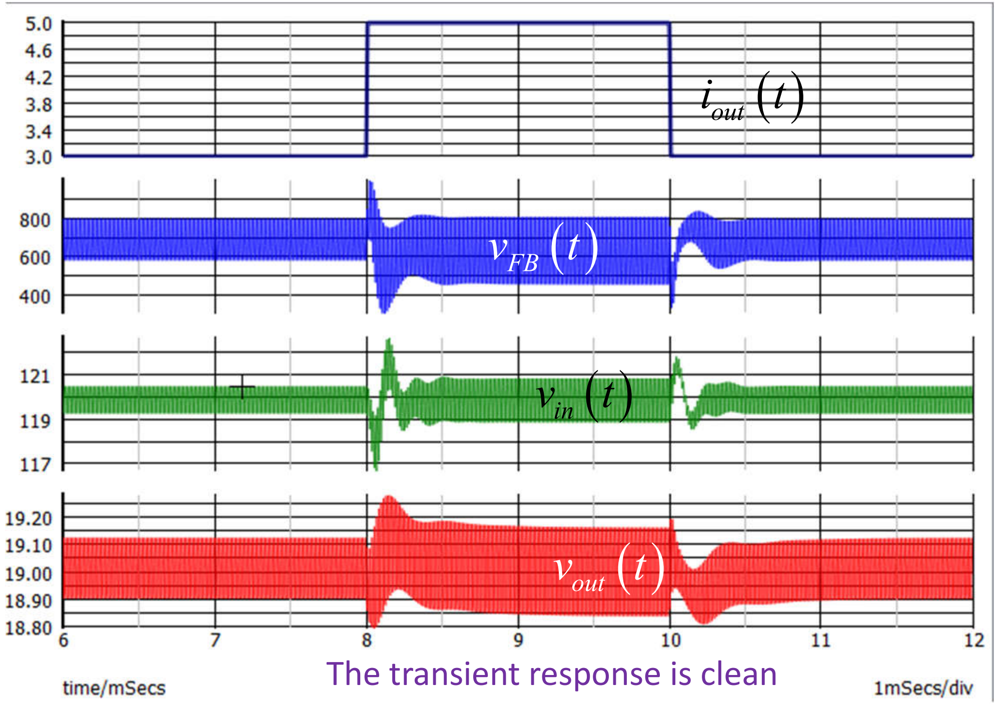
C. Basso, *Input Filter Interactions with Switching Regulators*, APEC Professional Seminar, Tampa (FL), 2017

Damper is Installed and Oscillations are Tamed

- The RC network is installed across the original capacitor
  - Watch for power dissipation as R_{12} will dissipate ac power



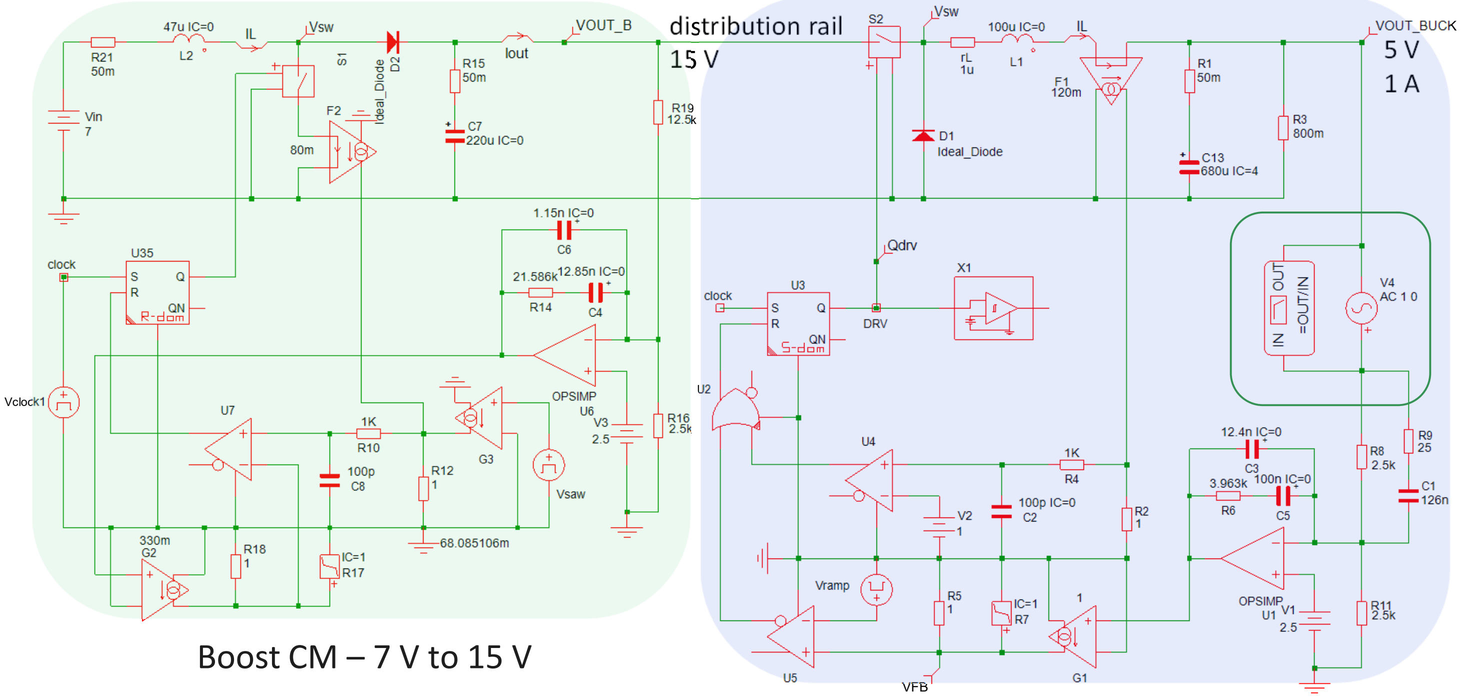
The damper is installed across the original EMI capacitor



The transient response is clean

Cascading Converters

- When power stages are associated, check interaction between converters
- The criterion involving the output and input impedance applies



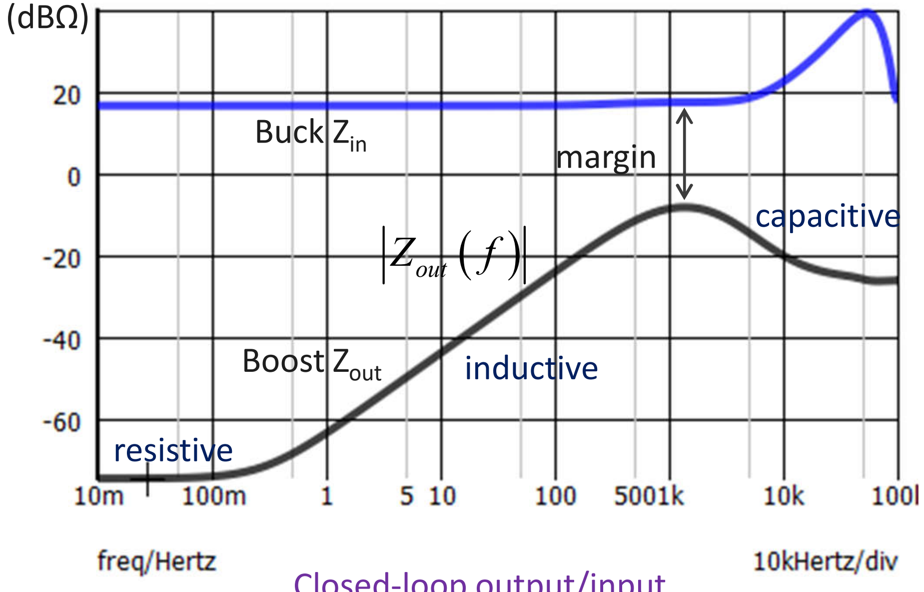
Open-loop gain frequency response

Boost CM – 7 V to 15 V

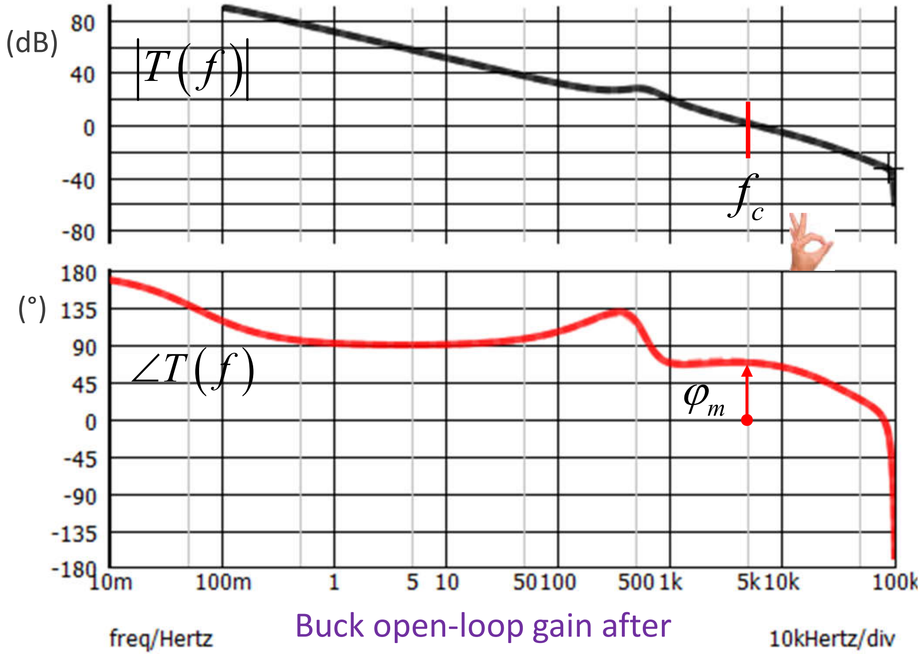
Buck CM – 5 V/1 A

A Stable Response

- You must individually plot output and input impedances of the boost and buck stages
- Then check the stability of the downstream converter in different operating conditions



Closed-loop output/input impedances overlap check



Buck open-loop gain after addition of the damped filter

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Transfer Function Sensitivity

- The loop gain of a converter involves a power stage and a compensator
  - The power stage response is affected by parasitics and the modulator stage
  - The compensator response depends on components tolerances including the op-amp
- How will crossover, phase and gain margins be preserved along the production cycle?

CM buck power stage | Type 2 filter

$$T(s) \approx \underbrace{H_0 \frac{1+\frac{s}{\omega_{z_1}}}{1+\frac{s}{\omega_{p_1}}} \frac{1}{1+\frac{s}{\omega_n Q}+\left(\frac{s}{\omega_n}\right)^2}}_{\text{CM buck power stage}} \underbrace{G_0 \frac{1+\frac{\omega_z}{s}}{1+\frac{s}{\omega_p}}}_{\text{Type 2 filter}}$$

$$H_0 = \frac{R}{R_i} \frac{1}{1+\frac{RT_{sw}}{L_2}\left[m_c(1-D)-0.5\right]} \qquad \omega_{z_1} = \frac{1}{r_C C_3} \qquad m_c = 1+\frac{S_e}{S_n}$$

Artificial ramp (S_e)

Inductor on-slope (S_n)

$$\omega_{p_1} = \frac{1}{RC_3}+\frac{T_{sw}}{L_2 C_3}\left[m_c(1-D)-0.5\right] \qquad \omega_n = \frac{\pi}{T_{sw}} \qquad Q = \frac{1}{\pi\left[m_c(1-D)-0.5\right]}$$

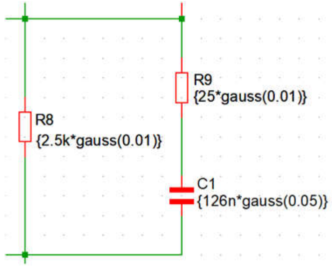
Sensitivity analysis to all elements!

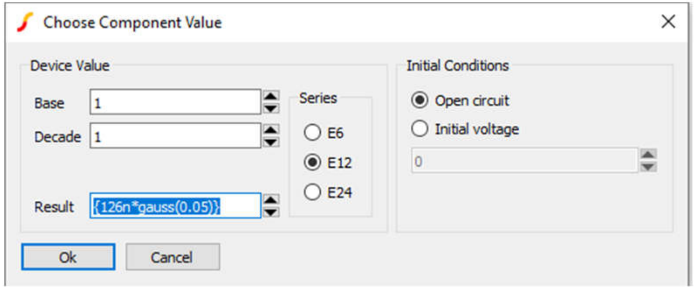
$$\left.\frac{\partial\left|T(R_i)\right|}{\partial R_i}\right|_{f=f_c}$$

$$\left.\frac{\partial\angle T(R_i)}{\partial R_i}\right|_{f=f_c}$$

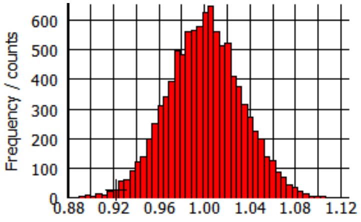
Statistical Parameters Variations

- A Monte Carlo analysis is a multivariate modeling technique
- Assign tolerances to components, see how combinations affect a variable
  - ➢ Check dispersion on crossover frequency, phase and gain margins

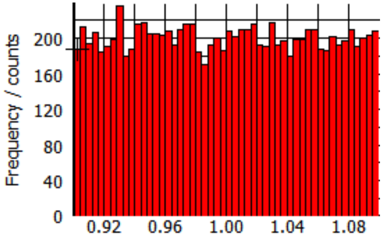




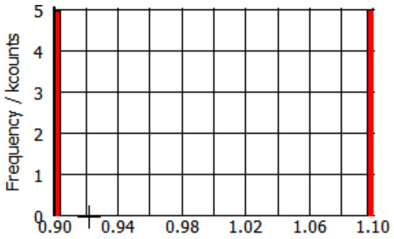
- Chose distribution type like gaussian (normal), uniform or corner (WCA)



gauss(tol)



unif(tol)

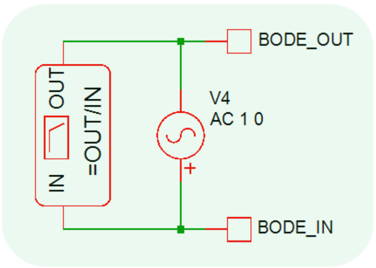


WC(tol)

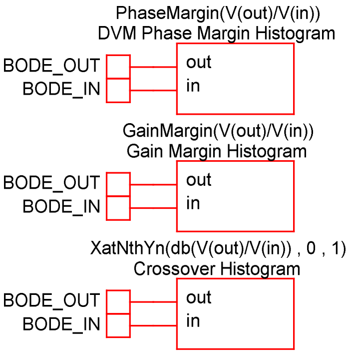
C. Hymowitz, *Monte Carlo Gone Wrong*, https://www.edn.com/monte-carlo-gone-wrong/

Monte Carlo Steps

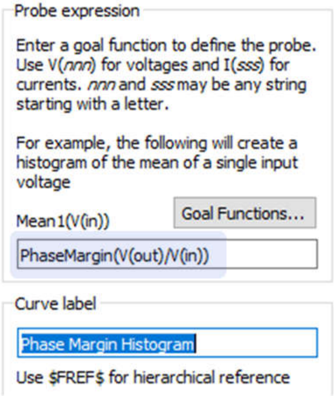
- You need to place specific probes instructing what parameters to record
- We want to check margins versus components variations



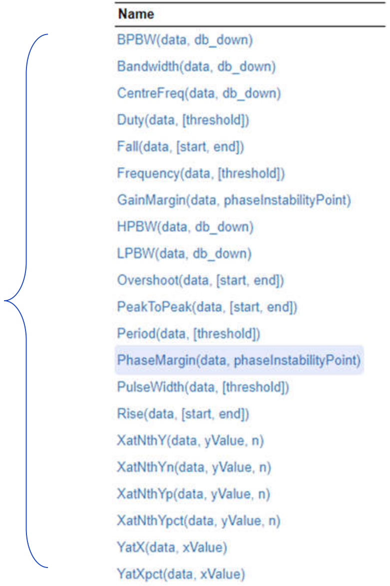
Transfer function measurement



Measurement probes



Goal functions

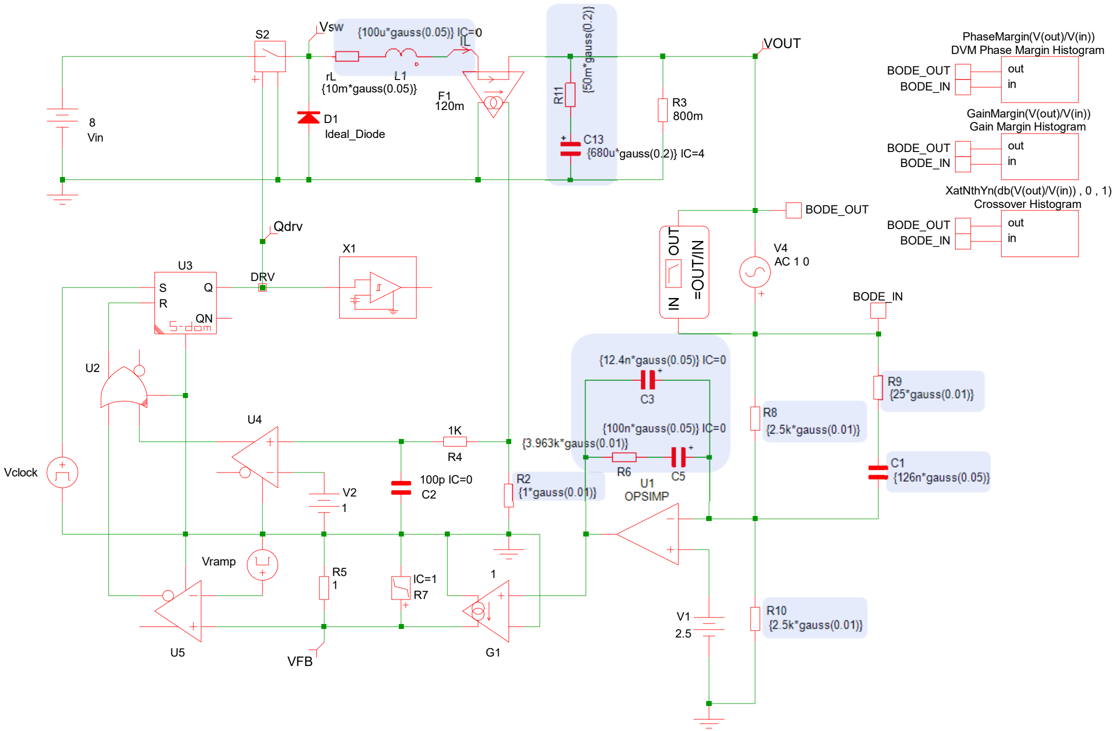


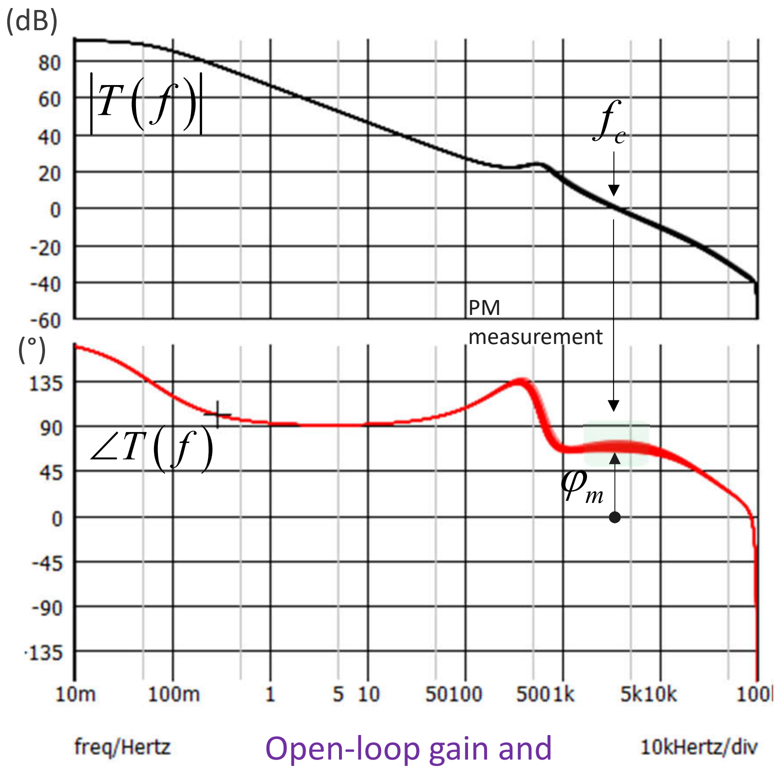
✓ Install special probes with a dedicated goal function

✓ Pick the right goal function in the list like PhaseMargin, GainMargin etc.

Running the Simulations

- Simulations can be run through the Monte Carlo menu using several computing cores

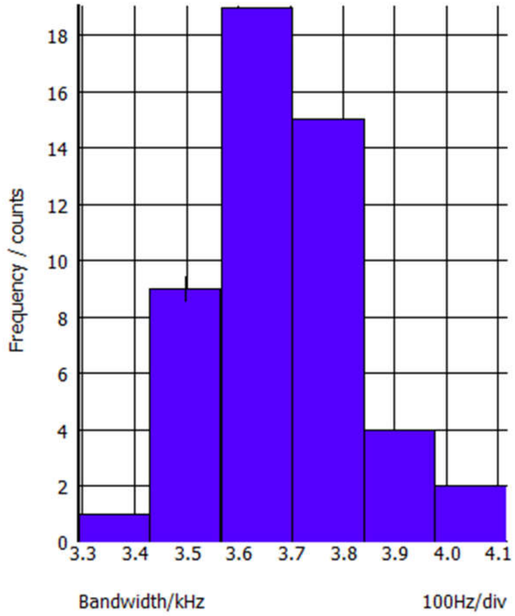




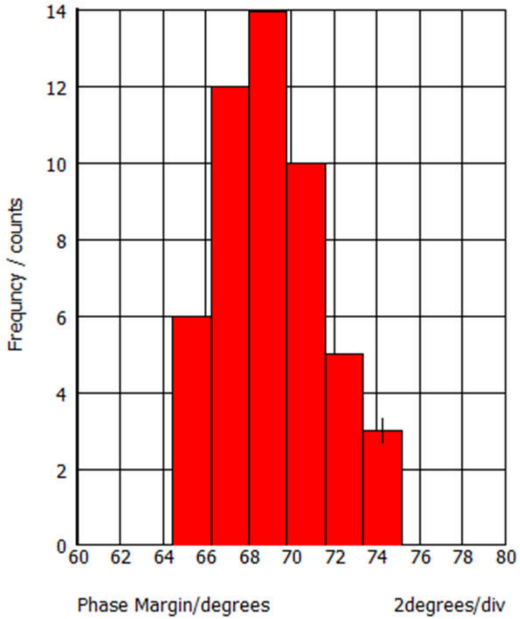
Open-loop gain and phase variations

Histogram Representation

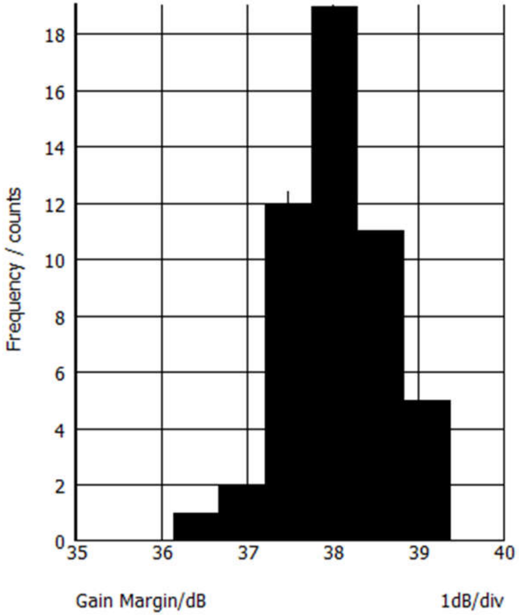
- SIMPLIS will build the histogram representation of the parameters we've selected
- In this example, all the margins are safe and crossover variations remain narrow



Crossover



Phase margin



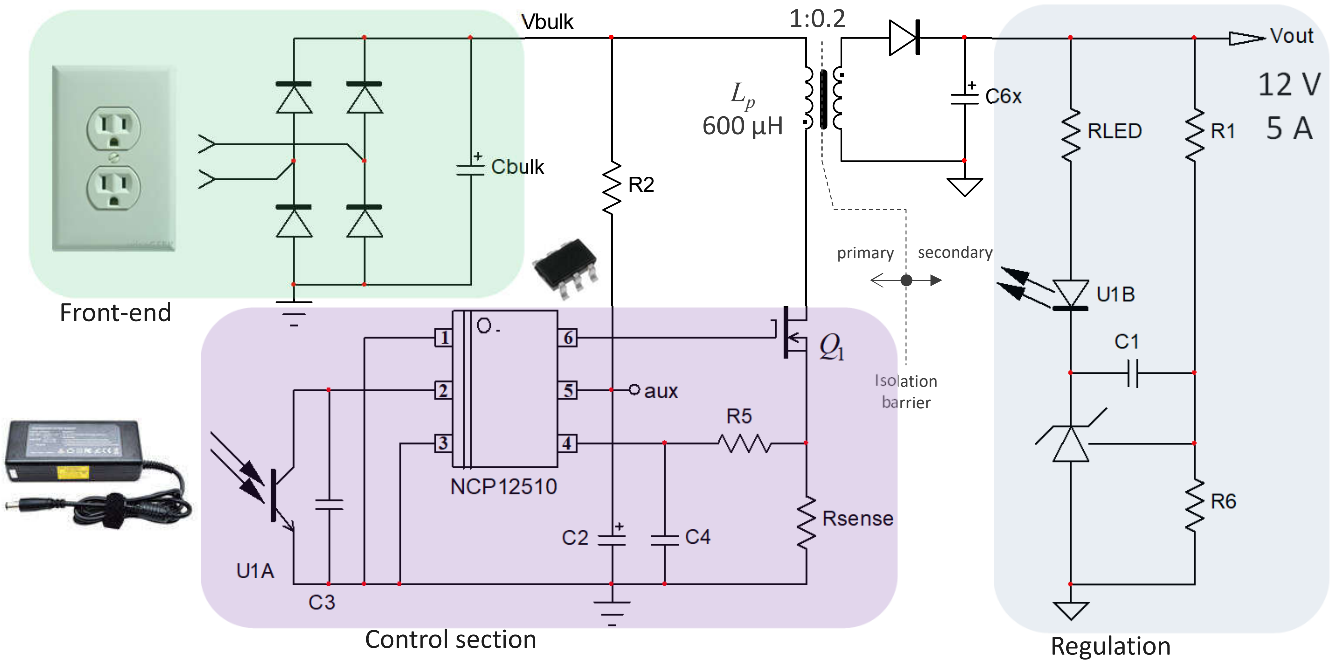
Gain margin

Agenda

- SPICE and Power Converters
- The SIMPLIS Approach
- Transfer Functions
- Power Factor Correction
- Interactions with EMI Filter
- Monte Carlo Analysis
- Design Example of a Flyback Converter

Designing a Flyback Converter

- We are going to design a universal-mains 60-W flyback converter delivering 12 V/5 A
- The study is divided in three parts: front-end, converter and control loop



The Front-End Rectifying Section

- The mains is rectified with a diode bridge and converted to a dc voltage
- A bulk capacitor plays the role of an energy reservoir when the input sine decreases
  - ➢ The utmost important parameter is the worst-case rms current

$$C_{bulk} = \frac{2P_{out}\left(\frac{1}{4F_{line}} + \frac{\sin^{-1}\left(\frac{V_{\min}}{V_{peak}}\right)}{2\pi F_{line}}\right)}{\eta\left(V_{peak}^{2} - V_{\min}^{2}\right)} \approx 93\ \mu\text{F}$$

60 V

Choose 100 µF

$$I_{C,rms} = I_{avg}\sqrt{\frac{2}{3F_{line}t_d} - 1} = 1.2\ \text{A rms}$$

V_{in} = 85 V rms

- Chose the component based on its rms capability at the worst-case temperature

(µF)	(ϕD)	(L)	ripple (mA rms)	tan δ	endurance (hours)				Panasonic part-number
100	18.0	40.0	2060	0.24	10000	0.8	7.5	—	EEUEE2G101

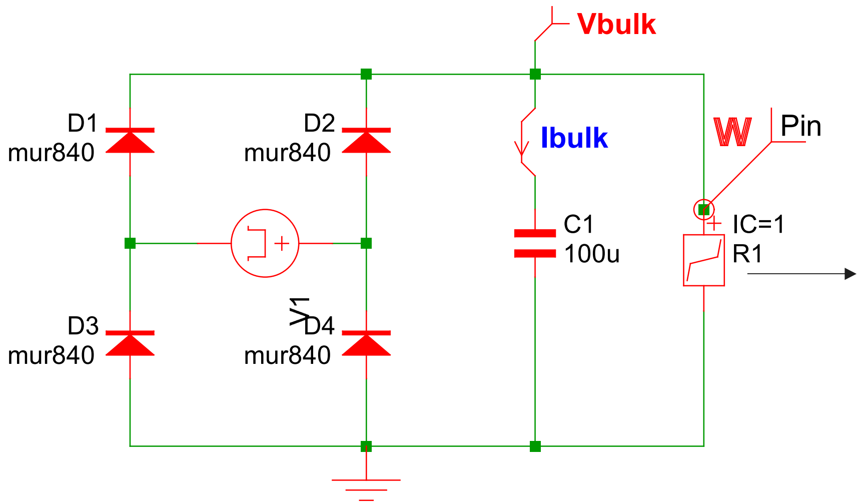
$$r_C = \frac{\tan\delta}{2\pi \cdot 120 \cdot 100u} = 3.4\ \Omega$$

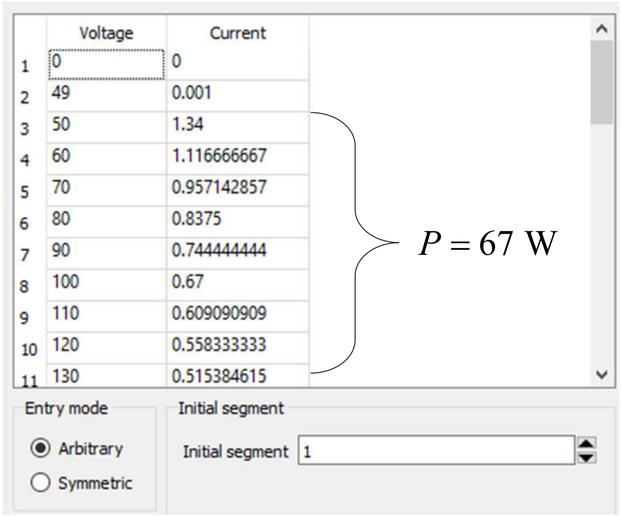
$$P_d = 1.16^2 \cdot 3.4 \approx 4.6\ \text{W}$$

sims

Implement a Constant-Power Load

- The load is the downstream converter which keeps a constant output power
- This is important to increase the absorbed current as the rectified voltage drops



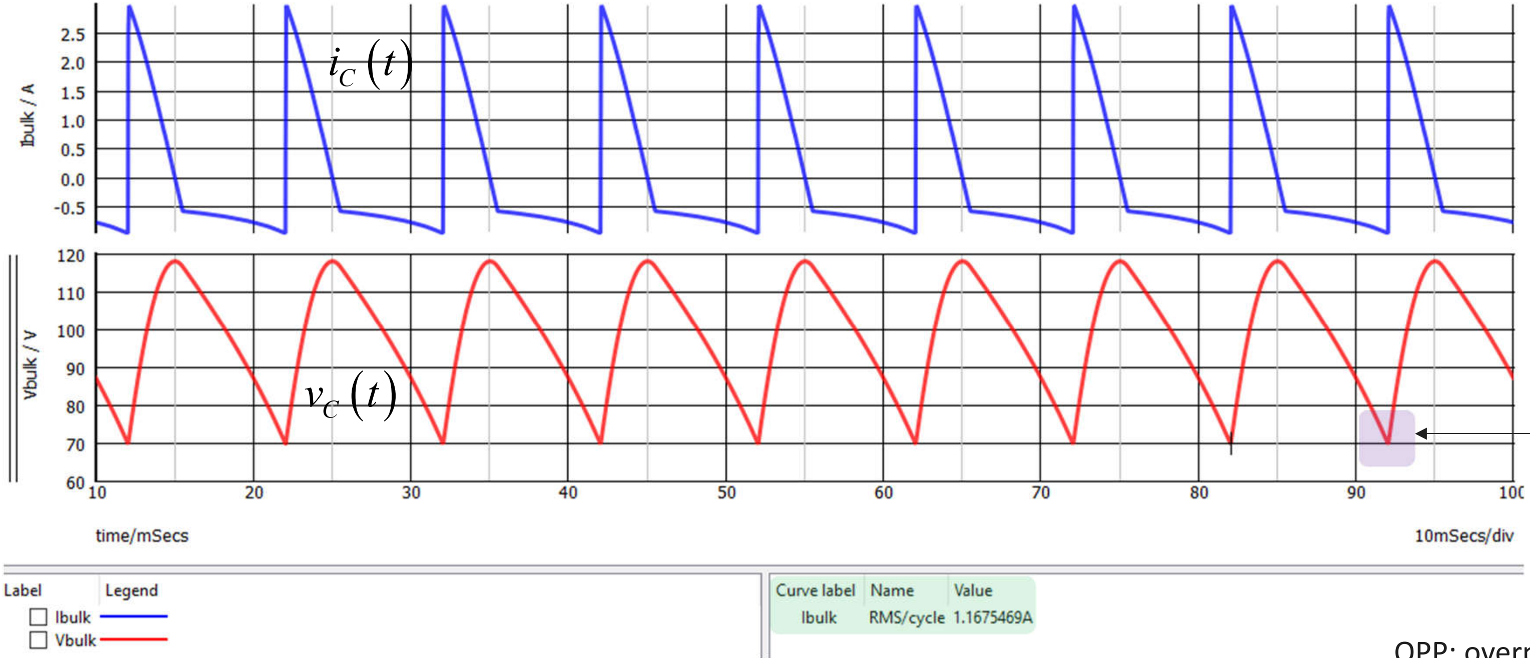


	Voltage	Current
1	0	0
2	49	0.001
3	50	1.34
4	60	1.116666667
5	70	0.957142857
6	80	0.8375
7	90	0.744444444
8	100	0.67
9	110	0.609090909
10	120	0.558333333
11	130	0.515384615

- A PWL resistance mimics the constant-power load with values calculated by Excel

Determining the Valley Voltage

- The converter shall deliver its nominal current down the rectified valley voltage
- It can imply an oversize of the converter if the ripple is too large – OPP issue
- ➢ Increasing the bulk capacitance is a possibility to increase the minimum voltage

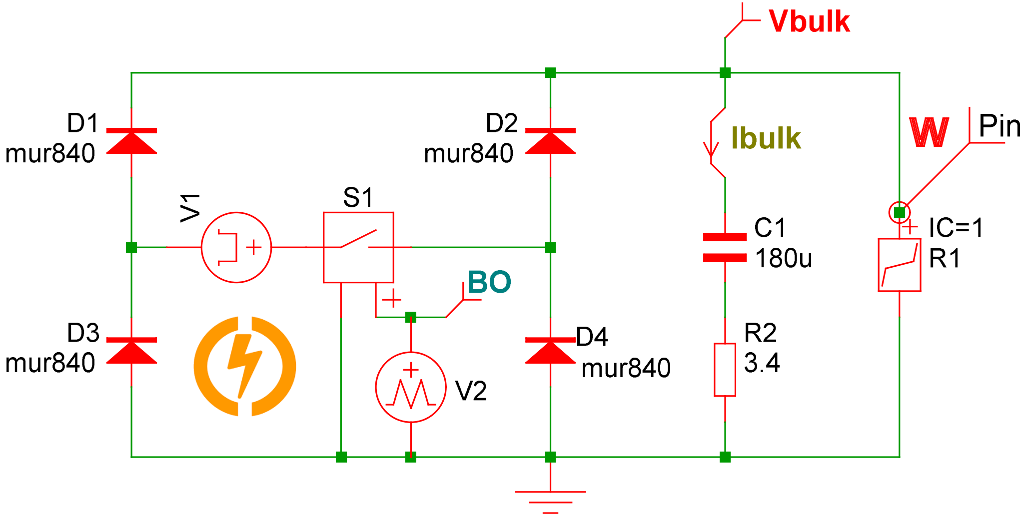


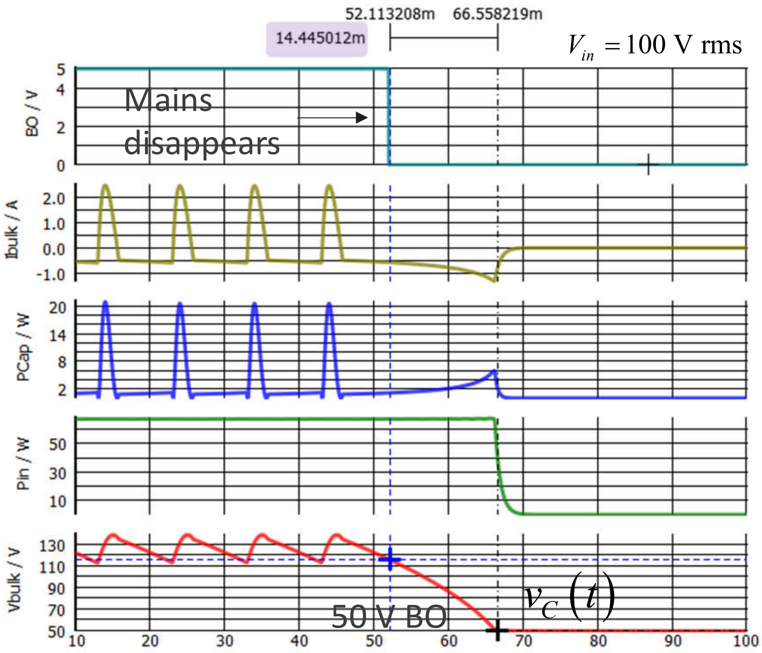
Valley voltage is 70 V

OPP: overpower protection

Check Hold-Up Time

- If the mains disappears, the bulk capacitor must maintain the dc rail for some time
- The converter shall continue operation for 10 ms in the worst case
- ➢ You may need to increase the capacitance to meet this goal





- ✓ The 180-µF capacitor brings 14 ms of hold-up time
- ✓ Rms current is 1.1 A and 88 V is the valley at 85 V_{ac}

Determine Primary Inductance Value

- The primary-side inductance sets the operating mode at nominal load current
- ✓ Too small an inductance yields to a high peak current and large conduction losses
- ✓ Too high the inductance will lead to slow converter with a low-frequency RHPZ

Adjust ripple

$$\delta I_r = \frac{\Delta I_L}{I_{L,avg}} = 1$$

$$N_{turns} := \frac{k_c \cdot (V_{out} + V_f)}{BVdss \cdot k_d - V_{os} - V_{bulkmax}} = 0.103$$

transformer turns ratio

$$L_p := \frac{\eta \cdot V_{bulkmin}^{2} \cdot \left(\frac{V_{out} + V_f}{N_{turns}}\right)^2}{\delta I_r \cdot F_{sw} \cdot P_{out} \cdot \left[V_{bulkmin} + \left(\frac{V_{out} + V_f}{N_{turns}}\right)\right] \cdot \left[\left(\frac{V_{out} + V_f}{N_{turns}}\right) + \eta \cdot V_{bulkmin}\right]} = 556.424\,\mu H$$

Adjust ripple

88 V

$$L_{leak} := L_p \cdot k_{leak} = 3.339\,\mu H$$

leakage inductance

$$V_{clamp} := k_c \cdot \frac{V_{out} + V_f}{N_{turns}} = 157.5V$$

selected clamp voltage

BV_{DSS} = 650 V
IPP65R190C7

$I_{D,rms}$ = 0.87 A rms

$P_{D,cond} \approx$ 0.4 W

Determine RHP zero position

$$f_{RHPZ} = \frac{(1 - D_{max})^2 R_{load}}{2\pi D_{max} L_p N_{turns}^2} \approx 34 \text{ kHz}$$

$$f_c < 30\% \cdot f_{RHPZ}$$

$$f_c < 10 \text{ kHz}$$

Choose 2-3 kHz

RHPZ: right-half-plane zero

FUTURE ELECTRONICS

Determine Secondary-Side Ripple

- It is important to assess the secondary-side rms current
  - Determine power dissipated in the diode
  - Determine rms current in the capacitor

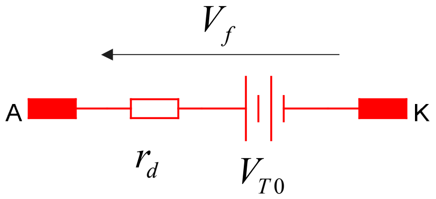


Peak Inverse Voltage: $PIV := V_{bulkmax} \cdot N_{turns} = 38.536V$

Secondary Peak Current: $I_{secpeak} := \dfrac{I_{LpeakM}}{N_{turns}} = 17.41A$

Secondary rms current: $I_{secrms} := \sqrt{(1 - D_{max})\left(I_{secpeak}^{2} - \dfrac{I_{secpeak} \cdot \Delta I_{L}}{N_{turns}} + \dfrac{\Delta I_{L}^{2}}{N_{turns}^{2} \cdot 3}\right)} = 7.886A$

Diode power dissipation: $P_{diode} := I_{out} \cdot V_f = 2.25W$



$$P_d = V_{T0} I_{d,avg} + r_d I_{d,rms}^{2}$$

$$P_d \approx V_f I_{out}$$


Maximum ESR value: $R_{ESR} := \dfrac{V_r}{I_{secpeak}} \approx 0.014\Omega$ ESR at 100 kHz

Capacitor rms current: $I_{Crms} := \sqrt{I_{secrms}^{2} - I_{out}^{2}} = 6.098A$

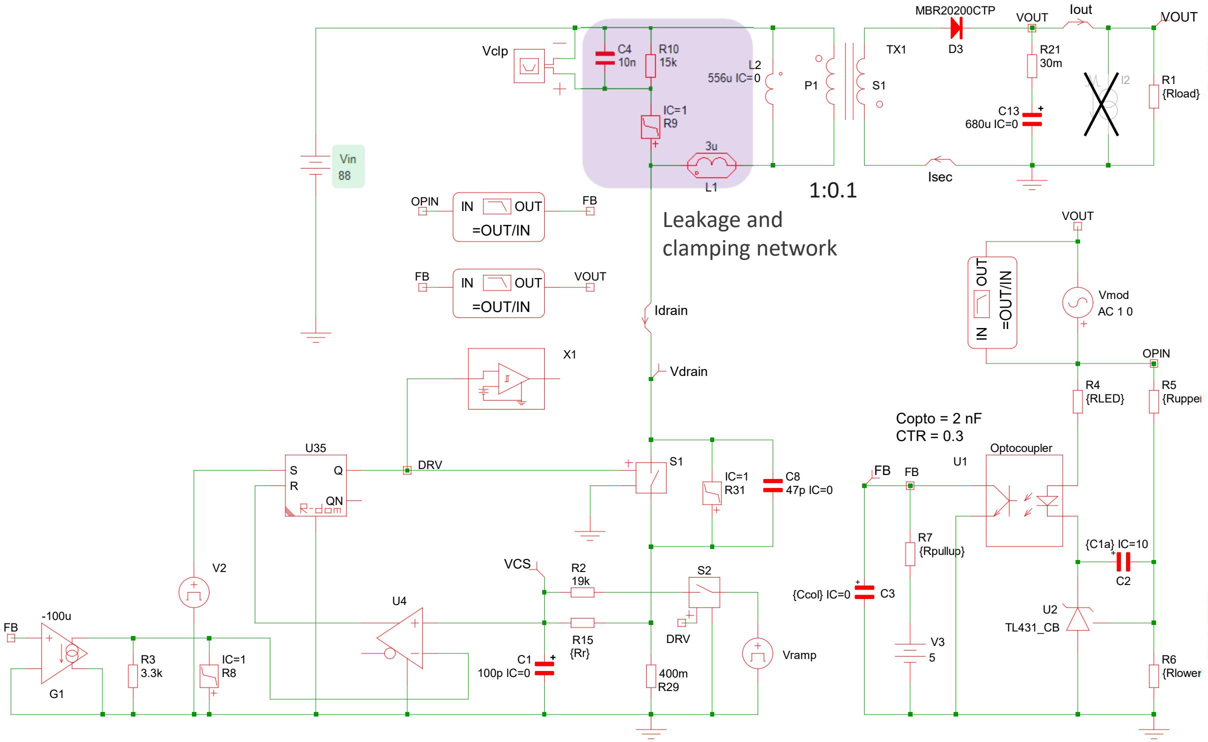
Capacitor dissipation: $P_C := I_{Crms}^{2} \cdot R_{ESR} = 0.534W$

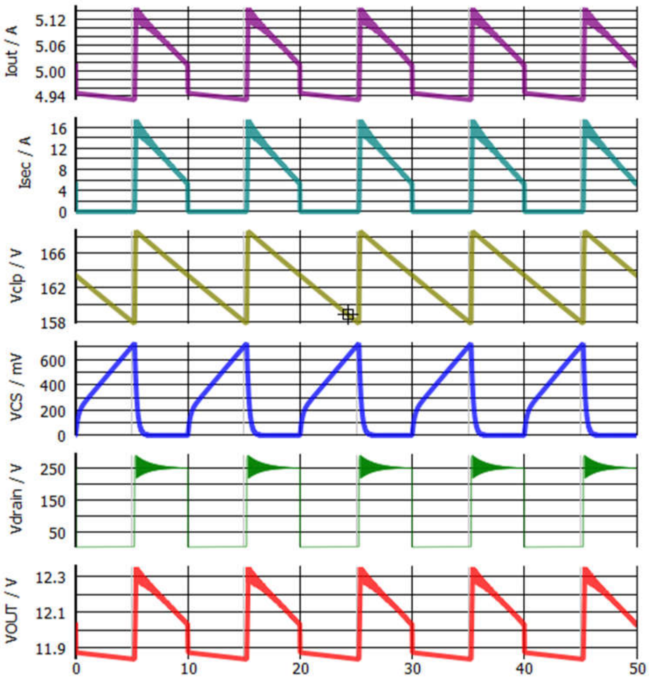

Secondary rms current sizes the wire gauge

Simulating the Basic Converter

- The current-mode structure compensation can be automated

➢ Verify the operating point is correct at the lowest input voltage (88 V)

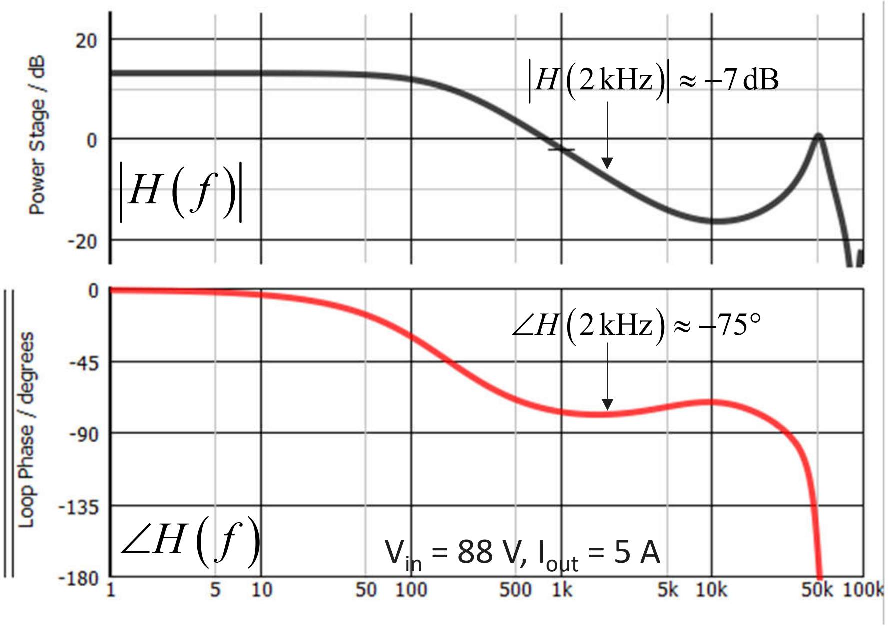




✓ V_{out} = 12 V
✓ I_{out} = 5 A

Looking at the Compensation Strategy

- A current-mode converter can be stabilized with a type 2 compensator
- It can boost the phase up to 90° with a zero and a pole adequately placed
- ➢ Start with the frequency response at the lowest dc input voltage



Automate calculations

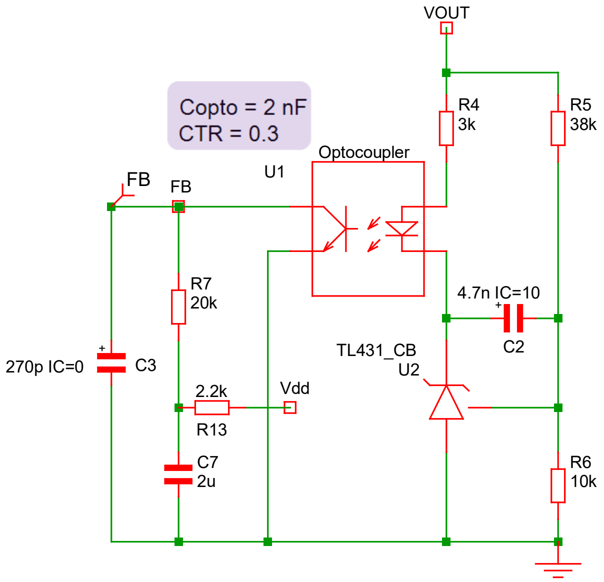
Enter text

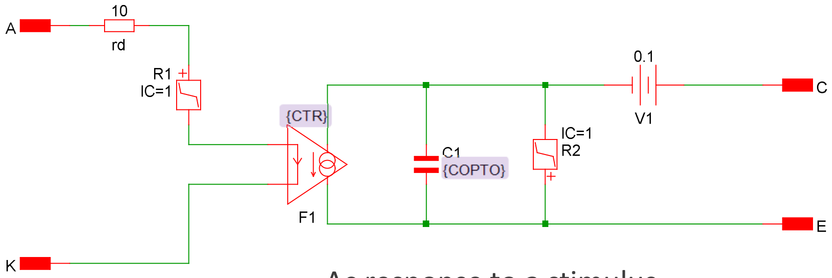
```
*
* Enter values extracted from the plant Bode plot
*
.VAR Gfc=-7 * magnitude at crossover *
.VAR PS=-75 * phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.VAR fc=2k * targetted crossover *
.VAR PM=60 * choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.VAR Ibias=250u
.VAR Vref=2.5
.VAR Rlower=Vref/Ibias
.VAR Rupper=(Vout-Vref)/Ibias
*
* Optocoupler specifications *
*
.GLOBALVAR Rpullup=20k * check with the selected control chip *
.GLOBALVAR Fopto=6k
.GLOBALVAR Copto=1/(2*pi*Fopto*Rpullup)
.GLOBALVAR CTR=0.33
*
.VAR VL=0.2
.VAR VCEsat=0.3
.VAR Vdd=5
.VAR Vf=1
.VAR A=Vout-Vf-VL
.VAR B=Vdd-VCEsat
.VAR Rmax=(A/B)*Rpullup*CTR
*
* Do not edit the below lines *
*
.VAR boost=PM-PS-90
.VAR fp=(tan(boost*pi/180)+sqrt((tan(boost*pi/180))^2+1))*fc
.VAR fz=fc^2/fp
.VAR G=10^(-Gfc/20)
.VAR RLED=CTR*Rpullup/G
.VAR C1a=1/(2*pi*fz*Rupper)
.VAR C2a=1/(2*pi*fp*Rpullup)
.VAR Ccol=C2a-Copto
```

From Bode plot

The Compensation Path Includes the Optocoupler

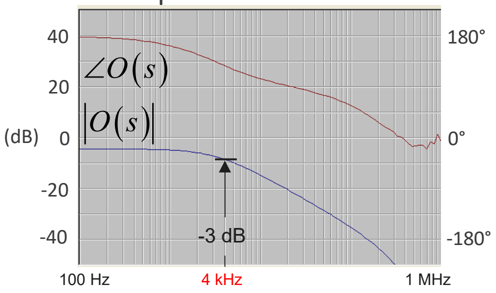
- The type 2 compensator can be built around a TL431 and an optocoupler
- The optocoupler exhibits a current transfer ratio and a low-frequency pole
- ➢ Always thoroughly characterize the optocoupler including its ac response





Characterize the opto

Ac response to a stimulus



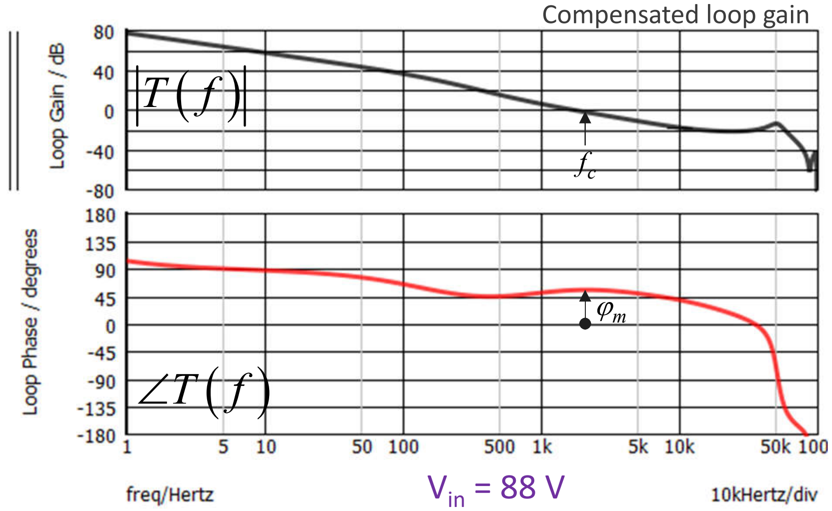
$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}}$$

$$C_{opto} \approx 2\ \text{nF}$$

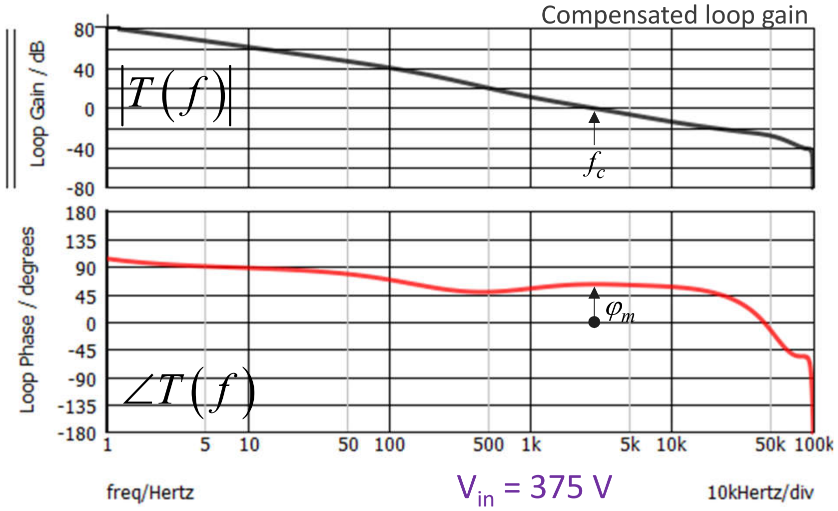
Assess Compensated Open-Loop Gain

- Once the stabilization strategy is selected, check crossover and phase margin

✓ Verify margins in low- and high-line operating conditions



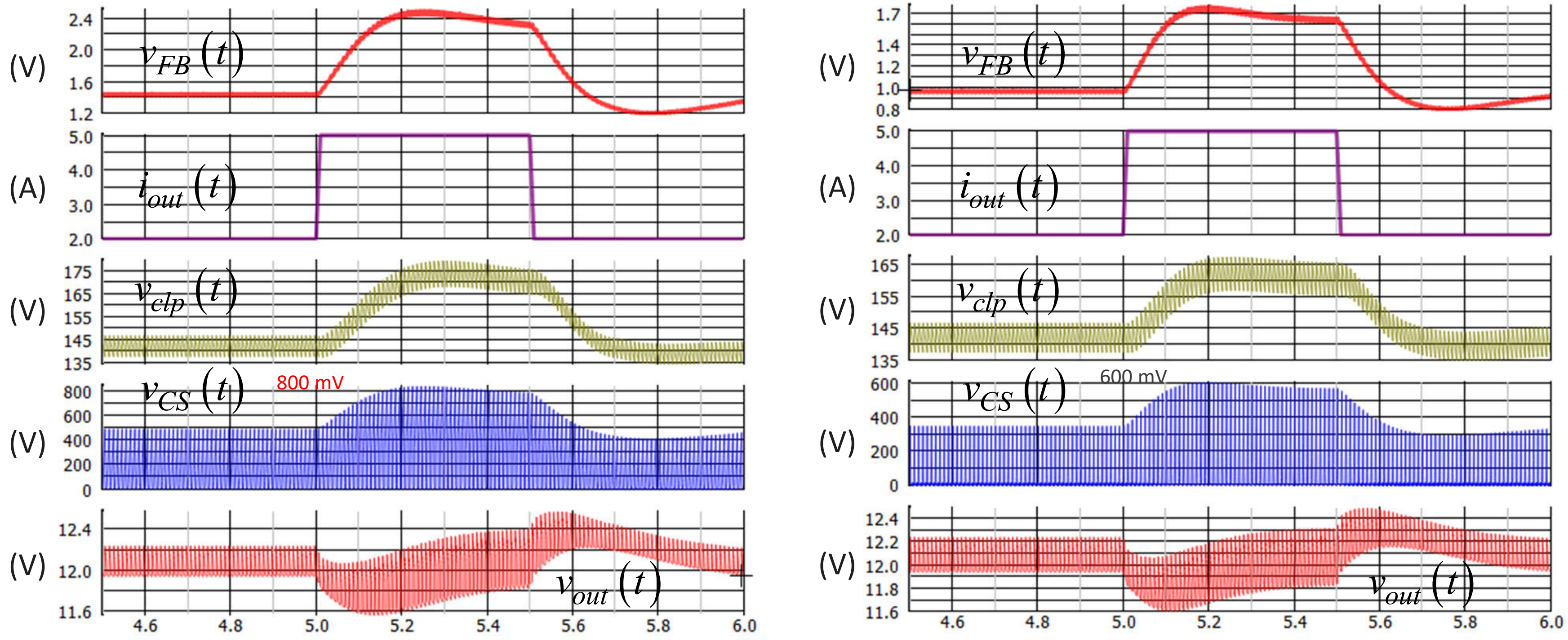
Curve label	Name	Value
Loop Gain	Gain Crossover Frequency	1.8814254kHz
Loop Gain	Gain Margin	18.964765dB
Loop Phase	Phase Margin	56.852504degrees



Curve label	Name	Value
Loop Gai...	Gain Crossover Frequency	2.9225618kHz
Loop Gai...	Gain Margin	25.879044dB
Loop Pha...	Phase Margin	62.721606degrees

Transient Response at Low- and High-Line Inputs

- Once the converter is stabilized and shows good margins, run transient tests
- Check undershoots are acceptable for the downstream load

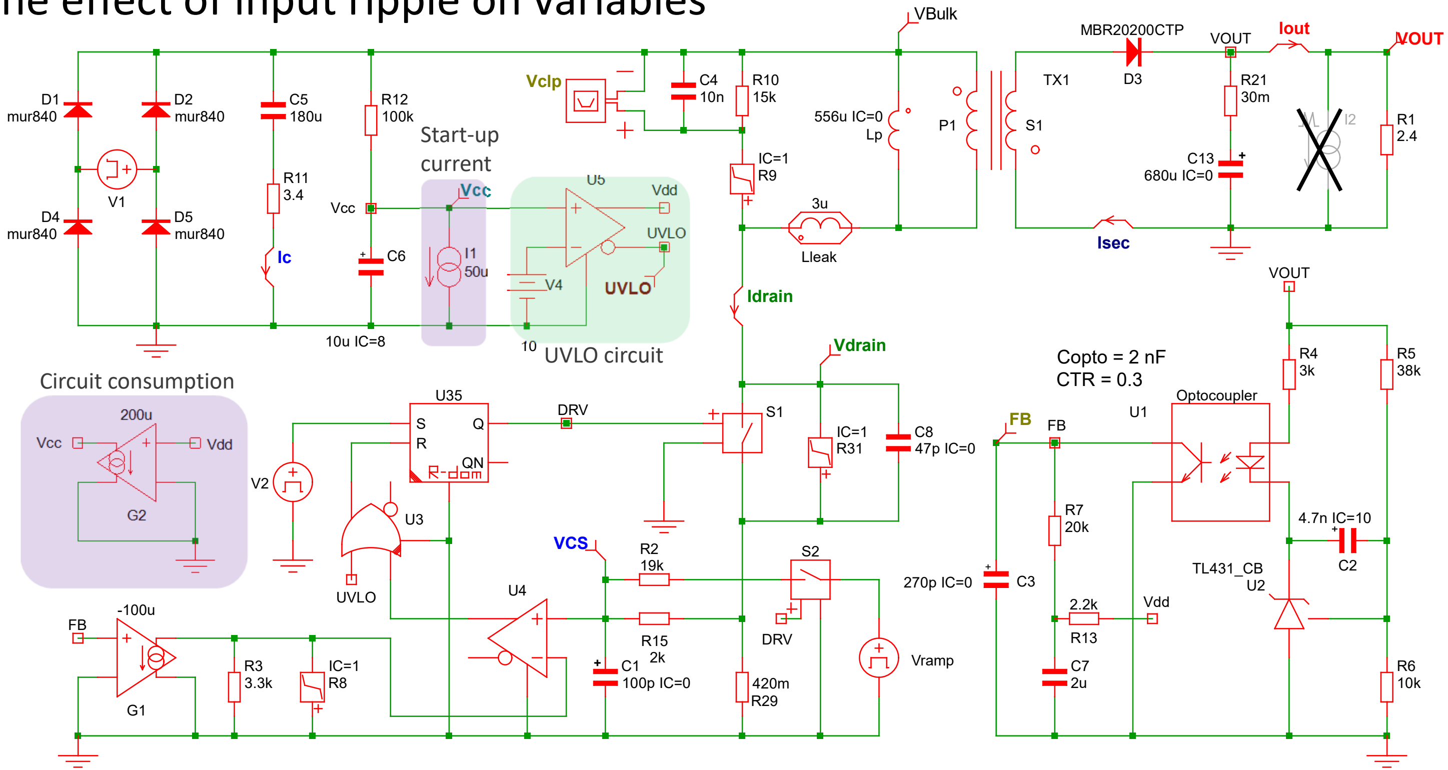


V_{in} = 88 V

V_{in} = 375 V

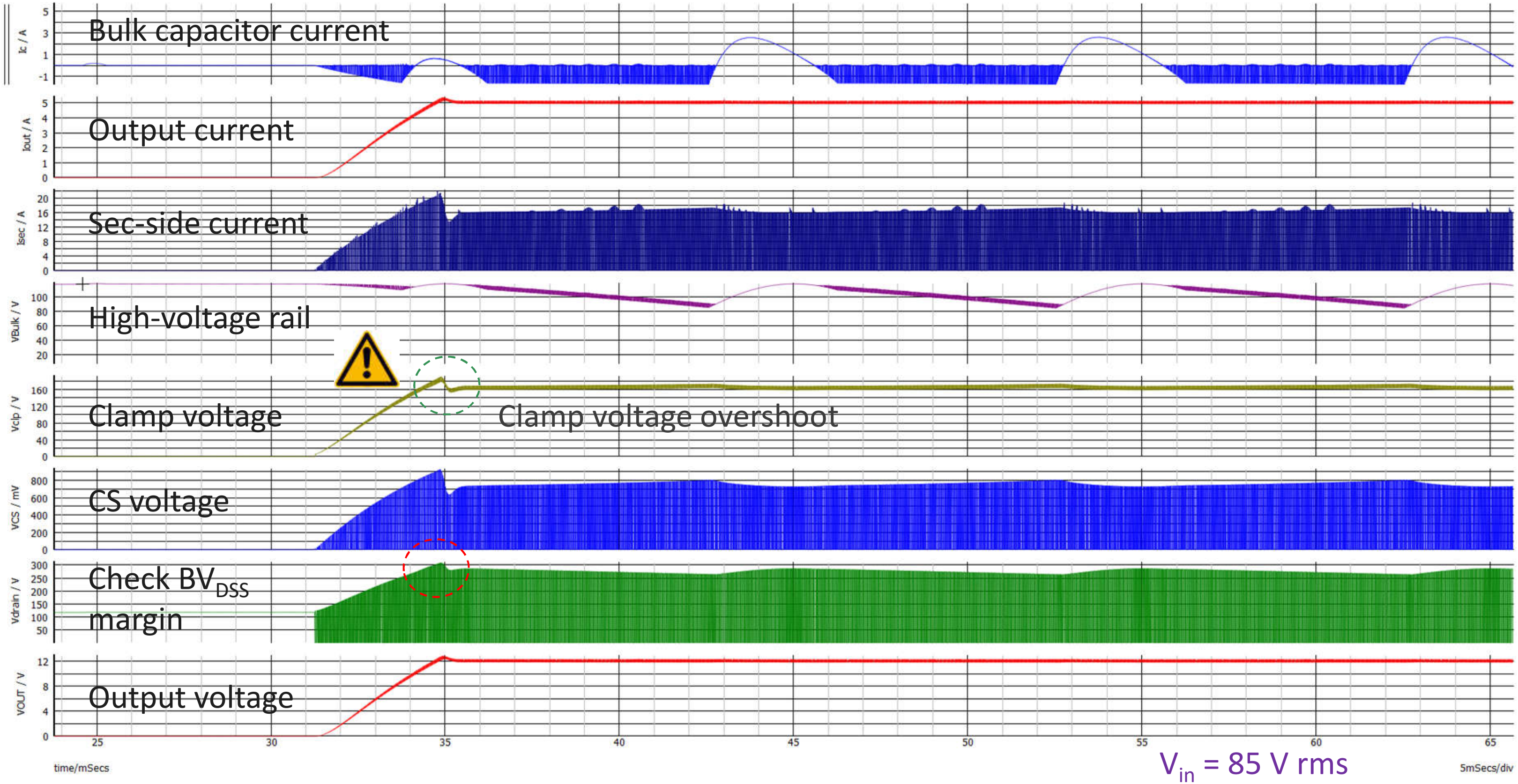
Look at the Big Picture

- It is now interesting to look at the same converter but powered from the mains
- See the effect of input ripple on variables



Looking at the Start-Up Sequence

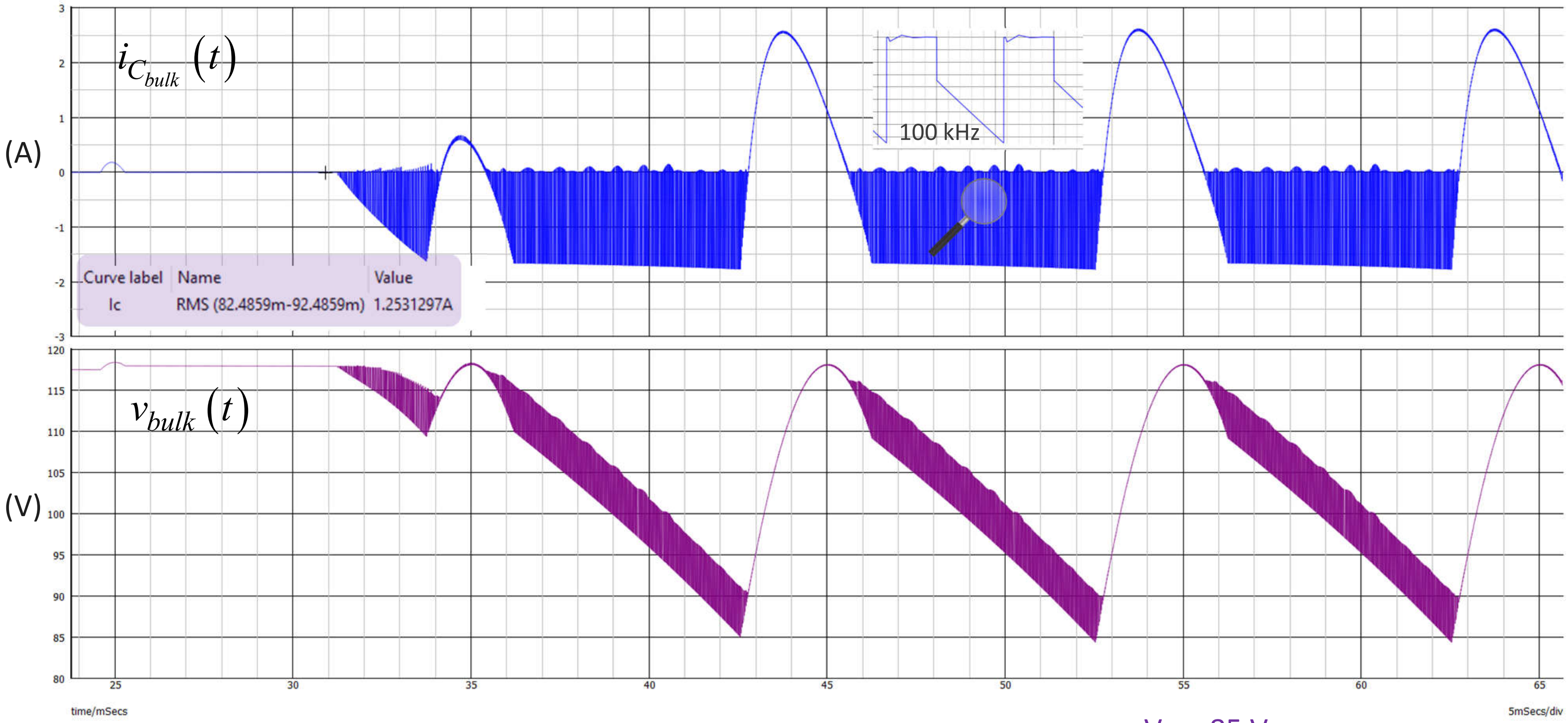
- The start-up sequence takes a simulation time of 30 s for a 100-ms run



V_{in} = 85 V rms

Check the Contribution of the Combined Currents

- The bulk rms current is made of low- and high-frequency ripple



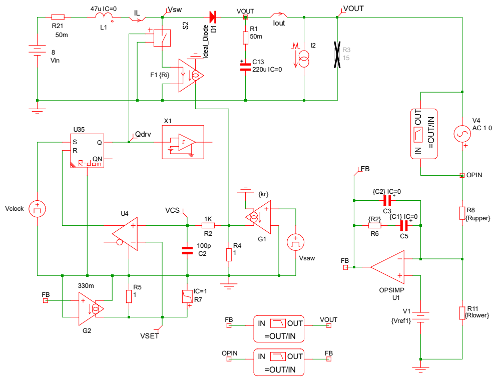
V_{in} = 85 V rms

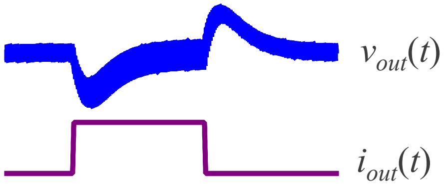
Ready-Made Templates

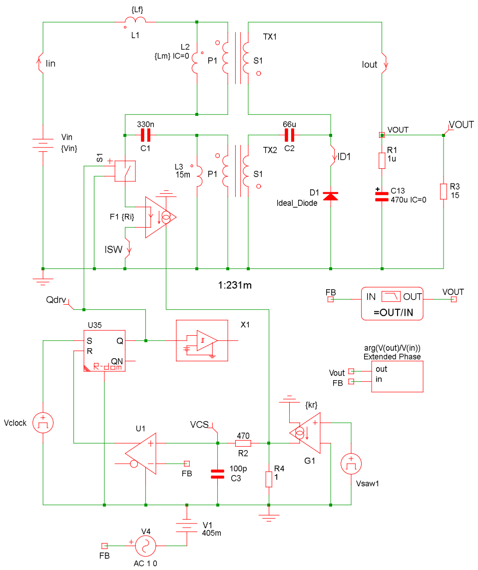
- My last book on transfer functions covers numerous switching topologies
- 120+ examples are now available in a free ZIP files you can download

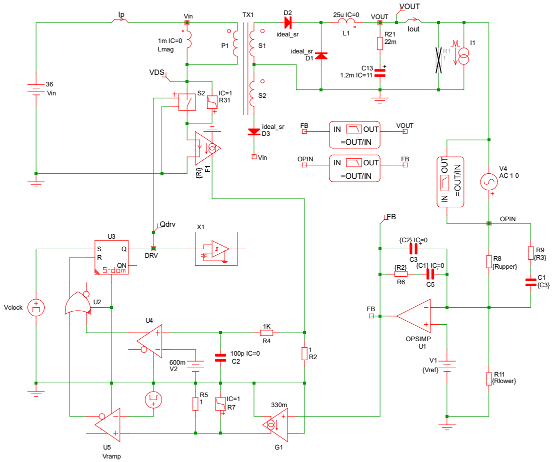
✓ Most of these circuits run on the demonstration version of SIMPLIS!

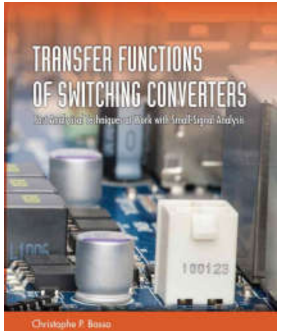
http://powersimtof.com/Downloads/Book/Christophe Basso SIMPLIS Collection.pdf











https://stairwaypress.com/product/transfer-functions-of-switching-converters/

Conclusion

- Simulating your power supply is an important part of the design flow
- SPICE simulation is an option but simulation time and lack of switching ac analysis is a problem
- SIMPLIS with its PWL engine delivers results in a flashing time
- ✓ An averaged model is no longer necessary and ac response is available from switching circuits
- ✓ It is a particularly-interesting feature for resonant converters for which modeling is difficult
- SIMPLIS allows you to test digital compensators and check coefficient values before coding
- Quick simulation is also a tremendous advantage for power correction circuits