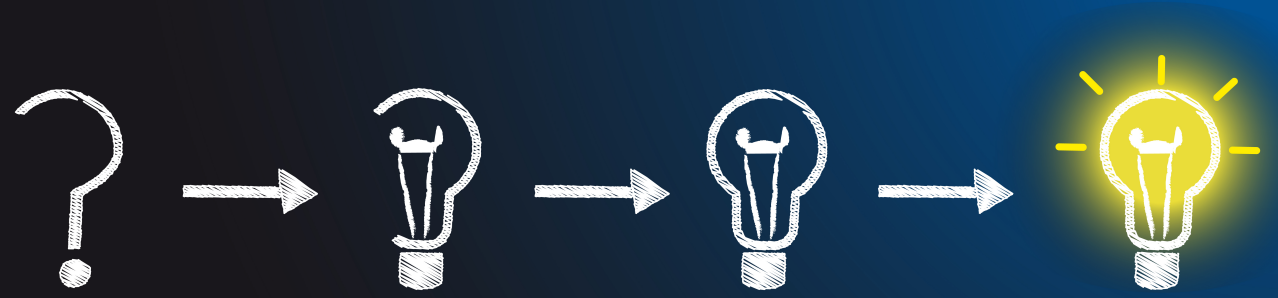


10th Power Analysis & Design Symposium

March 10th, 2021 - Worldwide (Virtual)

Net Capacitance

by Axel Schmidt (KEMET Electronics) & Günther Klenner (K&K Prime Engineering

OMICRON LAB

Welcome

10th Power Analysis & Design Symposium 2021 (VIRTUAL)

Net Capacitance

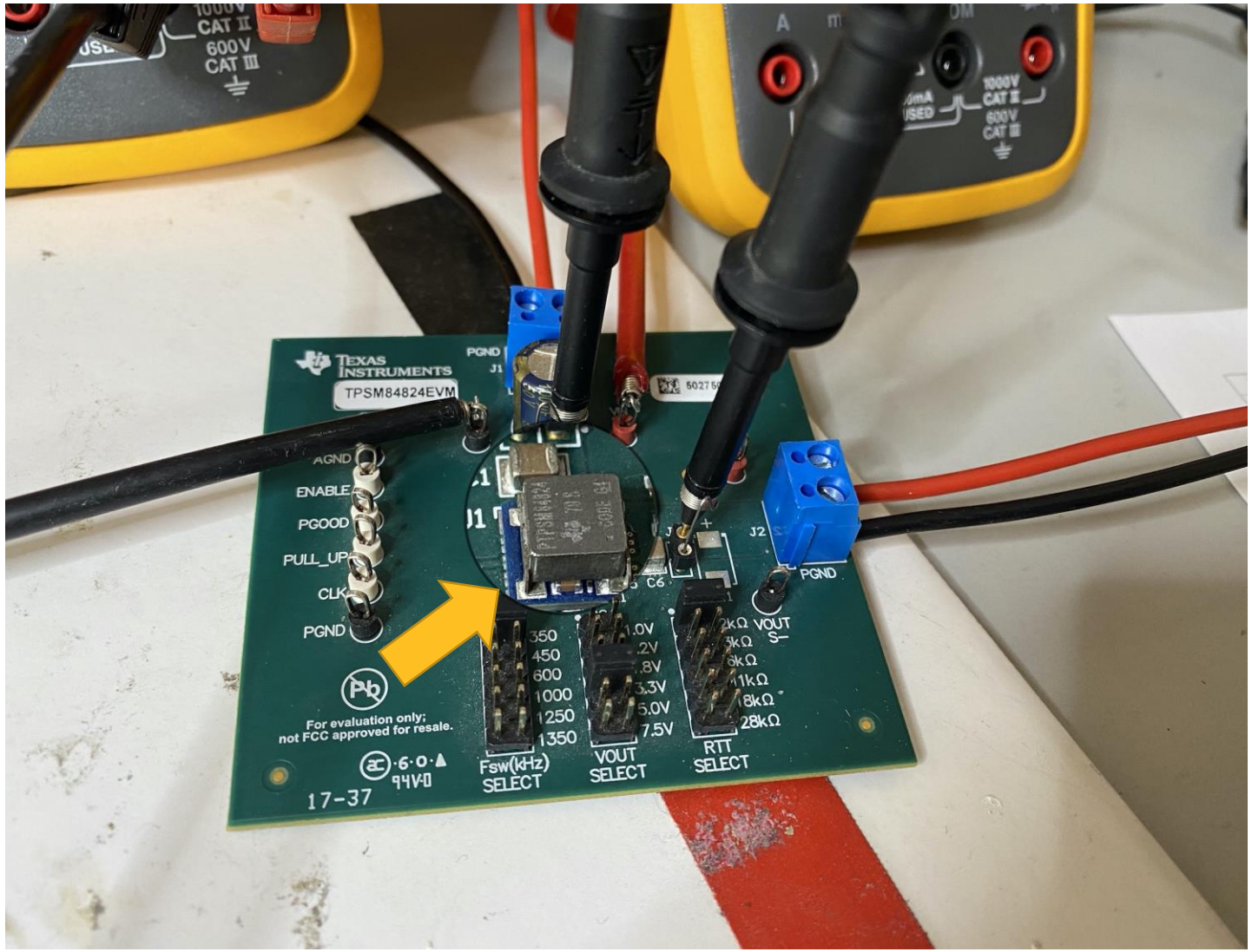
by Axel Schmidt (KEMET Electronics) & by Günther Klenner (K&K Prime Engineering)

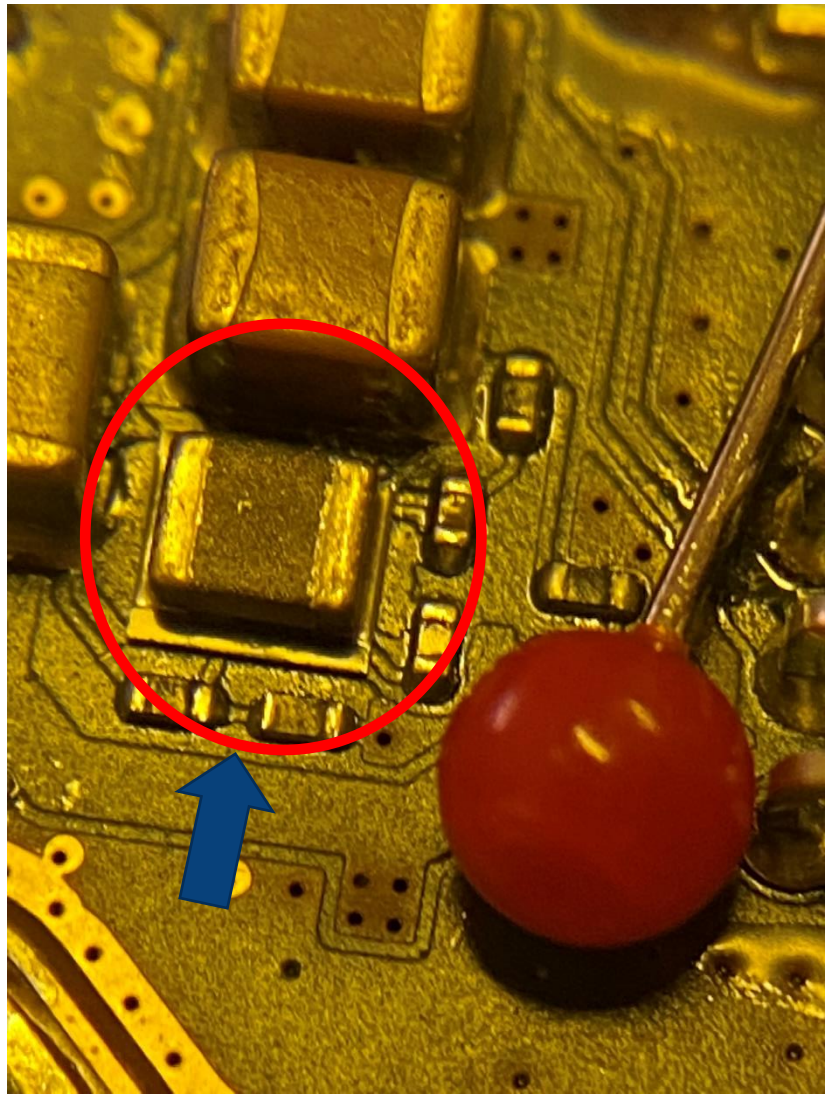
Speakers

- Günther Klenner
- Engineering Manager
- Fonder KK-Prime 2009

- Axel Schmidt,
- Senior Technical Marketing Manager
- with KEMET since 2003

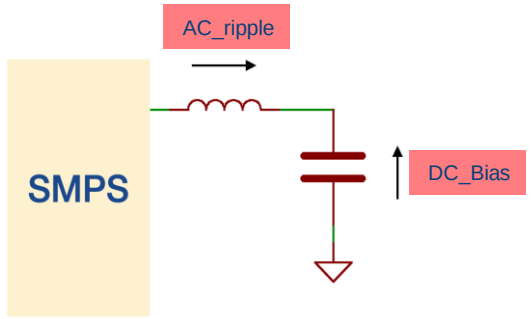
Modern SMPS

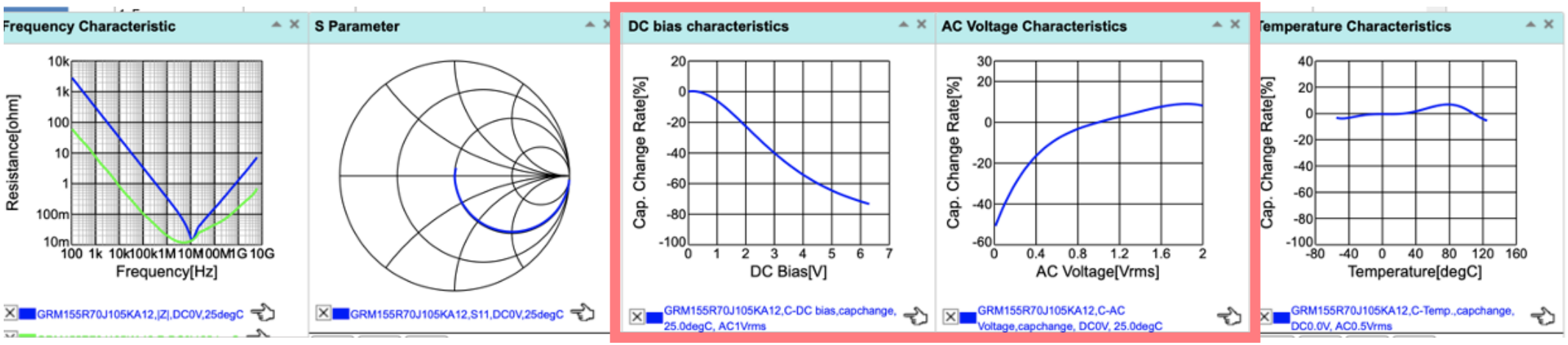




SMPS Questions

- SMPS output impedance depends on the effective capacitance.
- This capacitance depends on several application parameters.
- Do these parameters have an impact against each other?
- How do I process this data to get the “NET CAPACITANCE”?

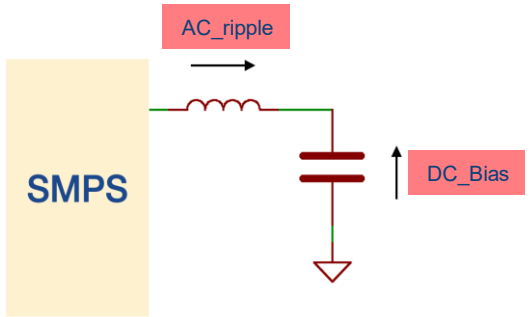




Net Capacitance

$$C_{net} = 1 - (Tolerance \cdot DC\_Bias \cdot AC\_ripple \cdot Frequency \cdot Temperature \cdot Aging)$$

Property	Typical values	Comments
Manufacturing tolerance	5%, 10% and 20%	
Temperature (X7R)	15%	
DC-Bias	20% - 90% nominal	Depend on the relation Vapp/Vrated
AC-Ripple	6% .. 12% at 10mV	Smaller Ripple higher caploss
Frequency	6% .. 10%	Smaller case loose more cap
Aging (Time)	2% to 5% per decade	Case size independent



How capacitance defined based on EIA 198

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	−55°C to +125°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	±15%
[1]Aging Rate (Maximum % Capacitance Loss/Decade Hour)	3.0%
[2]Dielectric Withstanding Voltage (DWV)	250% of rated voltage (5 ±1 seconds and charge/discharge not exceeding 50 mA)
[3]Dissipation Factor (DF) Maximum Limit at 25°C	See Dissipation Factor Limit Table
[4]Insulation Resistance (IR) Minimum Limit at 25°C	See Insulation Resistance Limit Table (Rated voltage applied for 120 ±5 seconds at 25°C)

[1] Regarding Aging Rate: Capacitance measurements (including tolerance) are indexed to a referee time of 1,000 hours.

[2] DWV is the voltage a capacitor can withstand (survive) for a short period of time. It exceeds the nominal and continuous working voltage of the capacitor.

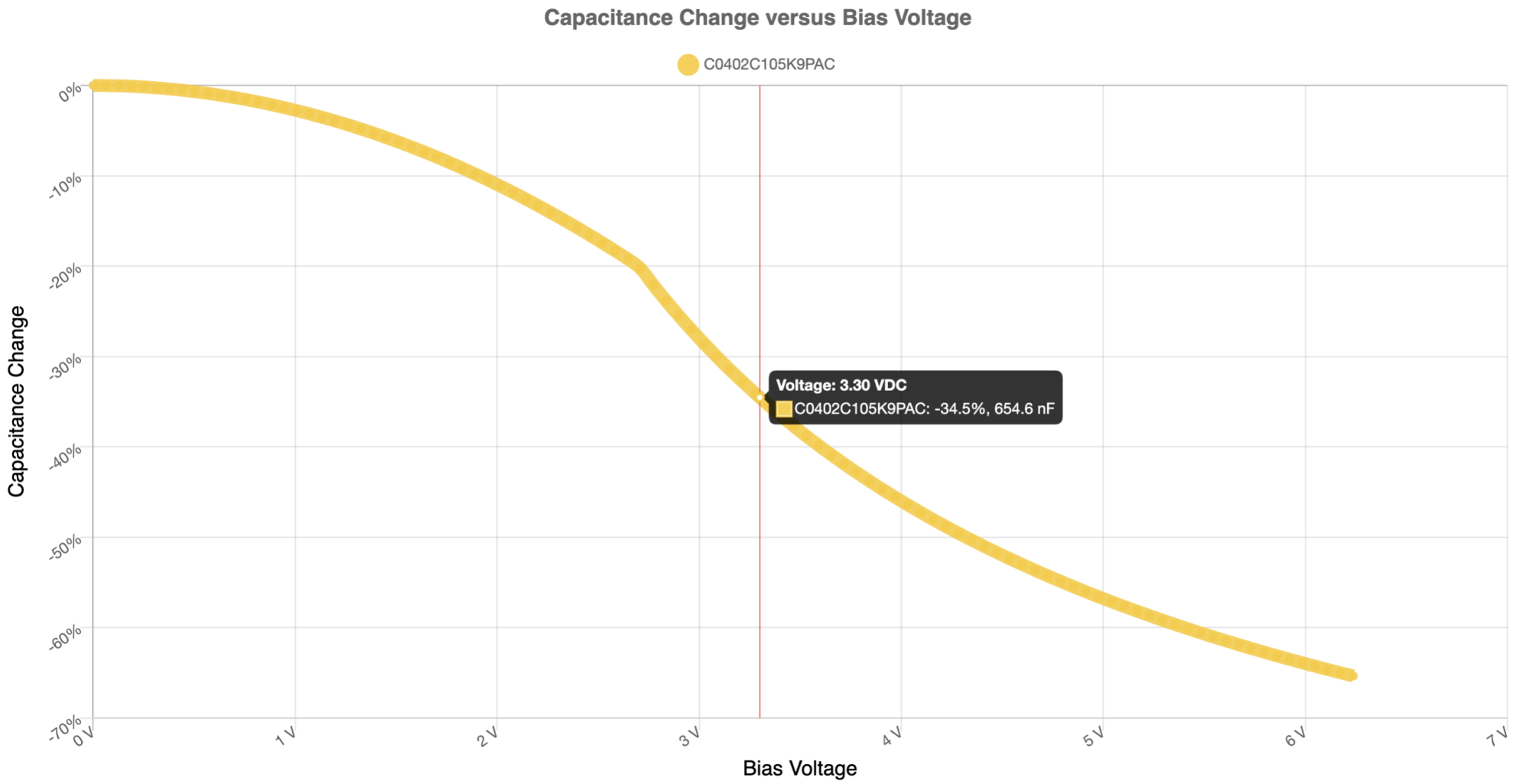
[3] Capacitance and dissipation factor (DF) measured under the following conditions:
1 kHz ±50 Hz and 1.0 ±0.2 V_{rms} if capacitance ≤ 10 µF
120 Hz ±10 Hz and 0.5 ±0.1 V_{rms} if capacitance > 10 µF

and NO DC-BIAS

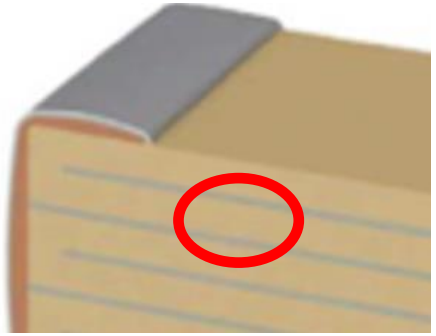
[4] To obtain IR limit, divide MΩ-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Capacitance loss on DC-Bias measured at 1kHz

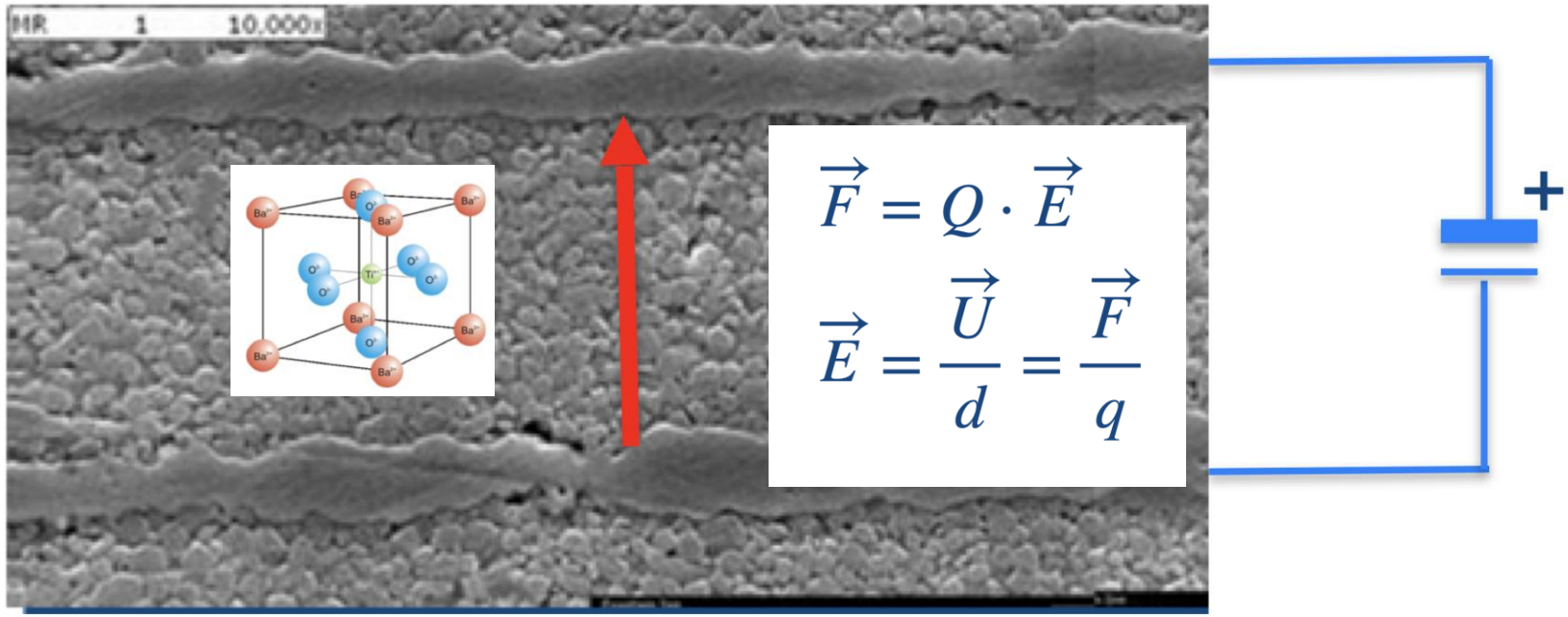


DC-Stress in the component



- Force on charged particle
- Depend on the E-Field in the dielectric
- Thinner dielectric leads to higher capacitance loss

$$C = \frac{\varepsilon_o \; k(E,T,freq) \; A \; (n-1)}{d}$$



Some hints @ 1kHz–
but what about other frequency

Measure Capacitance of Class-II and Class-III Ceramic Capacitors

This application note addresses proper capacitance measurement techniques of Class-II (X7R/X5R) and Class-III (Y5V/Z5U) ceramic capacitors and identifies common errors that are made upon incoming inspection or after board assembly. The methods outlined below highlight these errors and provides instruction for better electrical measurements and results.

Measurement Method for Capacitance

Overview

There are many instruments that can be used to measure the electrical properties of a capacitor. Instruments that measure capacitance, measure the impedance of a capacitor using a known AC voltage and frequency. The capacitance value is then extracted from the impedance measurement. Table 1 illustrates the voltage and frequency parameters recommended for measurement of Class-II and Class-III ceramic capacitors.

In this application note, the capacitor under test may also be referred to as a device under test or DUT.

Capacitance	Voltage	Frequency
≤ 10 µF	1.0 Vrms	1 kHz
>10 µF	0.5 Vrms	120 Hz

Table 1. Voltage and Frequency for Class-II and Class-III capacitance measurements

Output Impedance of the Instrument

All capacitance measurement equipment will have a known output impedance greater than zero. The output impedance will vary based upon the model and/or capacitance measurement range of the equipment. Impedance is a critical factor in the measurement of capacitance, especially when the impedance of the DUT approaches the impedance of the instrument. Figure 1 shows the general schematic of a capacitance measurement with the instrument source impedance.

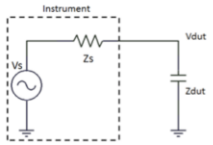


Figure 1. Schematic of Capacitance Measurement with Source Impedance

Instrument Voltage versus Actual Voltage on DUT

When a DUT is being measured for capacitance, the source voltage of the test equipment must be set to the desired measurement voltage. In the case of a 10 µF capacitor, the source voltage would be 1.0 Vrms based on Table 1. If the instrument's output impedance is high enough, it will cause a voltage divider and reduce the actual test voltage across the DUT.

Equation 1 shows the voltage across the DUT during the measurement. From the equation, as the source impedance (Zs) approaches the impedance of the DUT, there will be a voltage drop across the part.

$$Vdut = Vs * \frac{Zdut}{Zdut + Zs}$$

Equation 1. Voltage across the DUT during measurement

Using this equation, we can plot the percent voltage drop across the DUT during measurement as a function of capacitance. Figure 2 shows this plot which illustrates a drop in voltage at around 100 nF with only 15% of the voltage at 10 µF. The voltage steps up to around 80% just after 10 µF, due to the change in frequency.

Example 1:

Agilent E4980 LCR meter measuring capacitance of a 10 µF 10% X5R capacitor.

From Table 1, the desired voltage and frequency are 1.0 Vrms and 1 kHz, respectively. In this example, the output impedance of the test meter is 100 ohms based on the meter's specifications. At 1 kHz, the DUT impedance will be j*15.91 ohms. Using Equation 1, the voltage across the DUT will be approximately 157 mV. Thus, only about 15% of the output voltage is actually applied to the DUT. Because of the resulting voltage drop across the DUT, the capacitance measurement is invalid since it does not meet the test specifications outlined in Table 1. It is important to maintain a constant test voltage while measuring capacitance. Figure 3 shows an actual measurement of a 10 µF capacitor using the Agilent E4980 LCR meter. The measured AC voltage across the capacitor is only 186 mV, far below the 1 Vrms specification. The result of the test falsely indicates that the capacitor does not meet its rated specification. The next section will show how to correct for this anomaly and limitation.

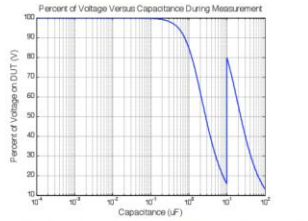


Figure 2. Percent of Voltage across DUT versus Capacitance

How do we correct for the voltage drop?

To ensure the voltage across the DUT is maintained at the desired level, the output voltage must be increased on the test meter to adjust for the voltage divider. Some capacitance measurement equipment will have a function called Auto-Level Control (ALC) which does this automatically. This feature enables the instrument to automatically increase the source voltage to meet the set voltage. When considering the case in Example 1, without the ALC function, the voltage across the DUT was 186 mV with a set voltage of 1.0 Vrms. If we enable the ALC function, the instrument will automatically raise the source voltage to achieve the desired 1.0 Vrms across the DUT. Figure 4 shows a measurement of the same 10 µF capacitor using the Agilent E4980 LCR meter with the ALC feature set to ON. The result of the test shows the capacitor measures within the 10% tolerance range.

Figure 3. Capacitance measurement of 10 µF capacitor.

Figure 4. Capacitance measurement of 10 µF capacitor using ALC function.

Voltage range of the Bode100

- The Bode100 has 50Ω Impedance

$$Z = 50\Omega$$

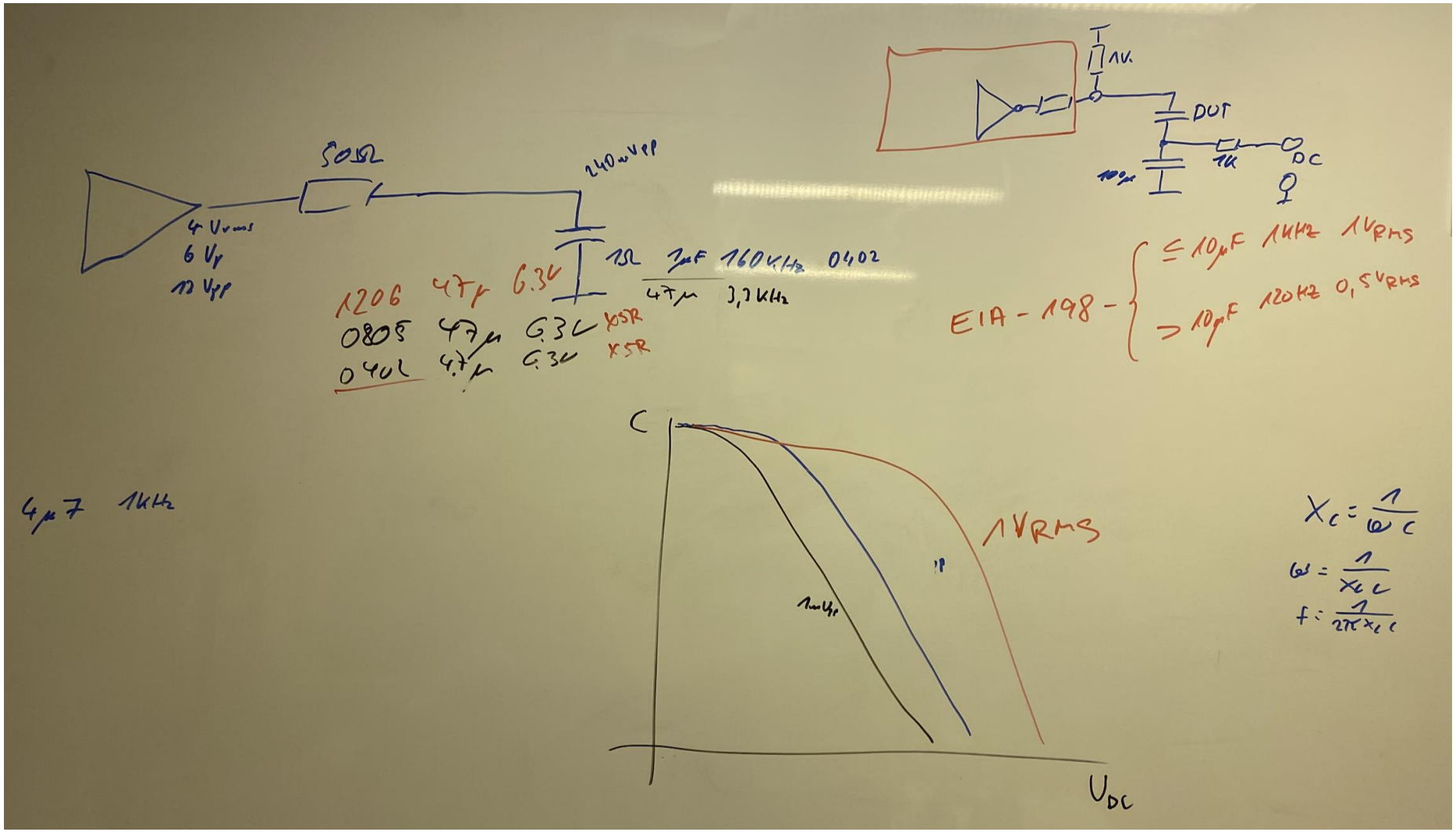
$$V = \sqrt{10^{\frac{dBm}{10}} \cdot Z \cdot 10^{-3}}$$

$$dBm = 20 \cdot log_{10}(V) - 10 \cdot log_{10}(Z) + 30$$

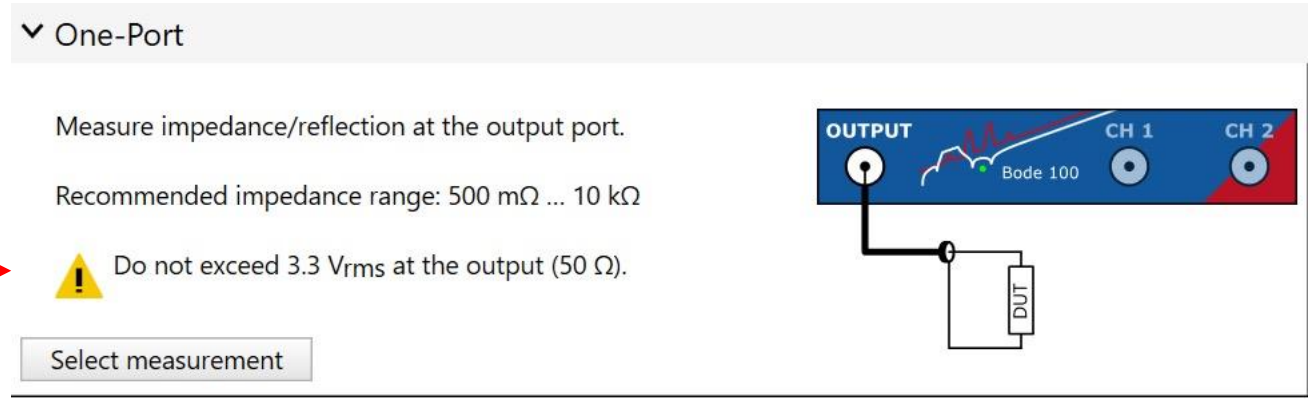
dBm an 50Ω in V

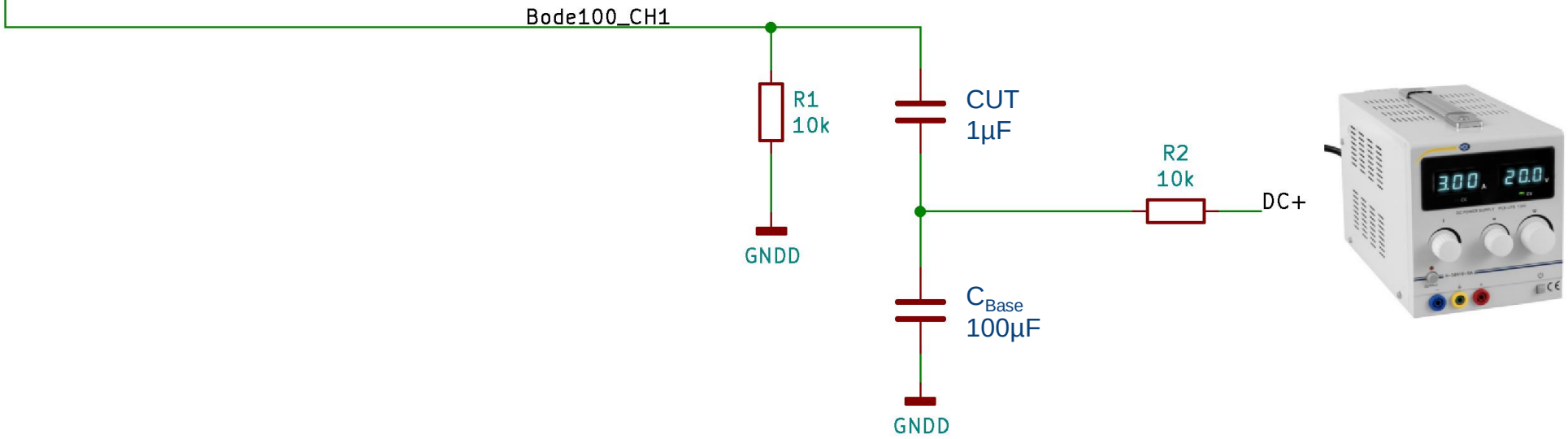
dBm	U/V	
-30	0,007	Bode 100 minimum
-20	0,022	
-19	0,025	Typical Ripple voltages
-13	0,050	Typical Ripple voltages
-10	0,071	Typical Ripple voltages
-5	0,127	
0	0,224	
5	0,396	
10	0,707	
13	1,000	Bode 100 maximum
18	1,800	Application DC-Bias Level
20	2,300	Application DC-Bias Level
23	3,300	Application DC-Bias Level
25	4,000	Bode 100 + Bode AMP12
27	5,000	Application DC-Bias Level

Using Bode 100 to measure: Basic ideas

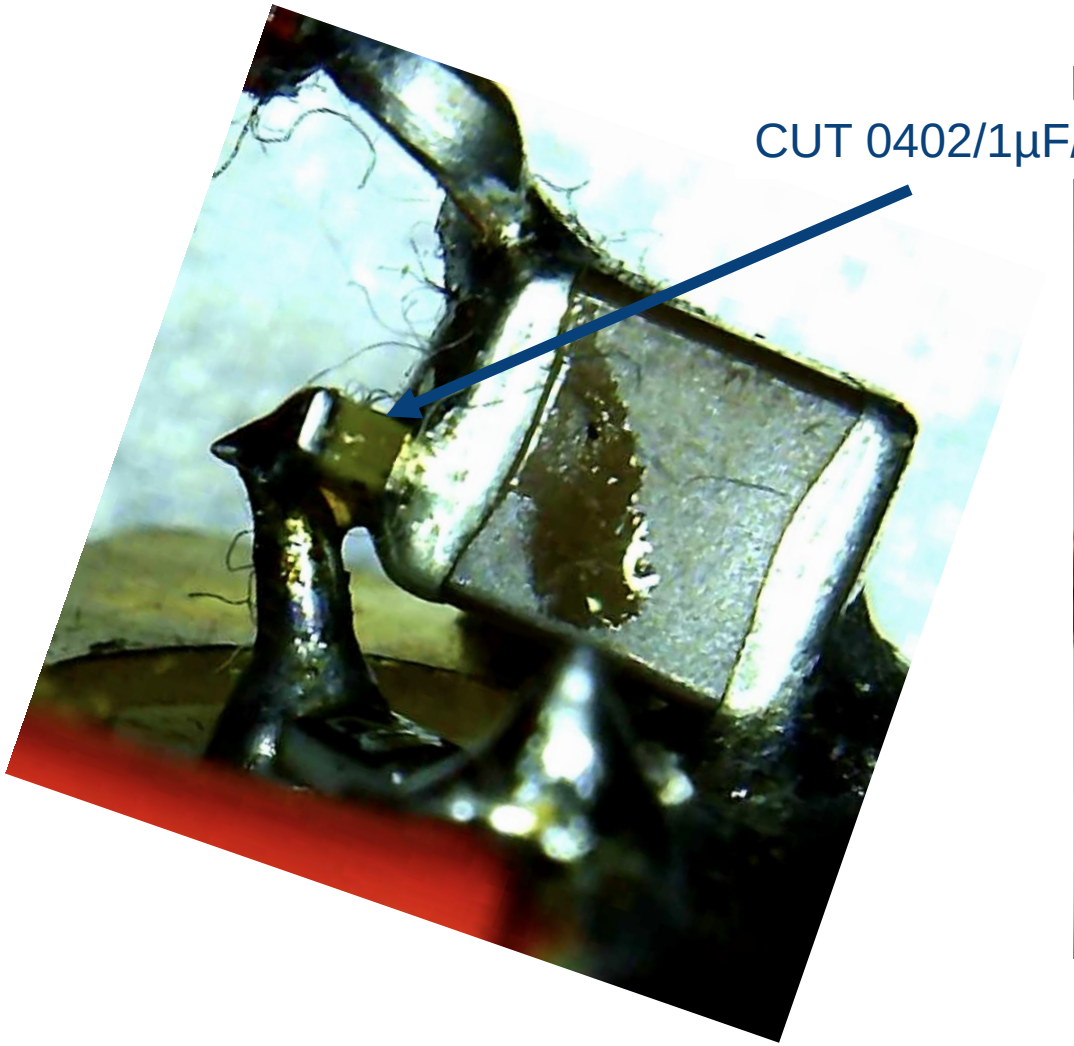


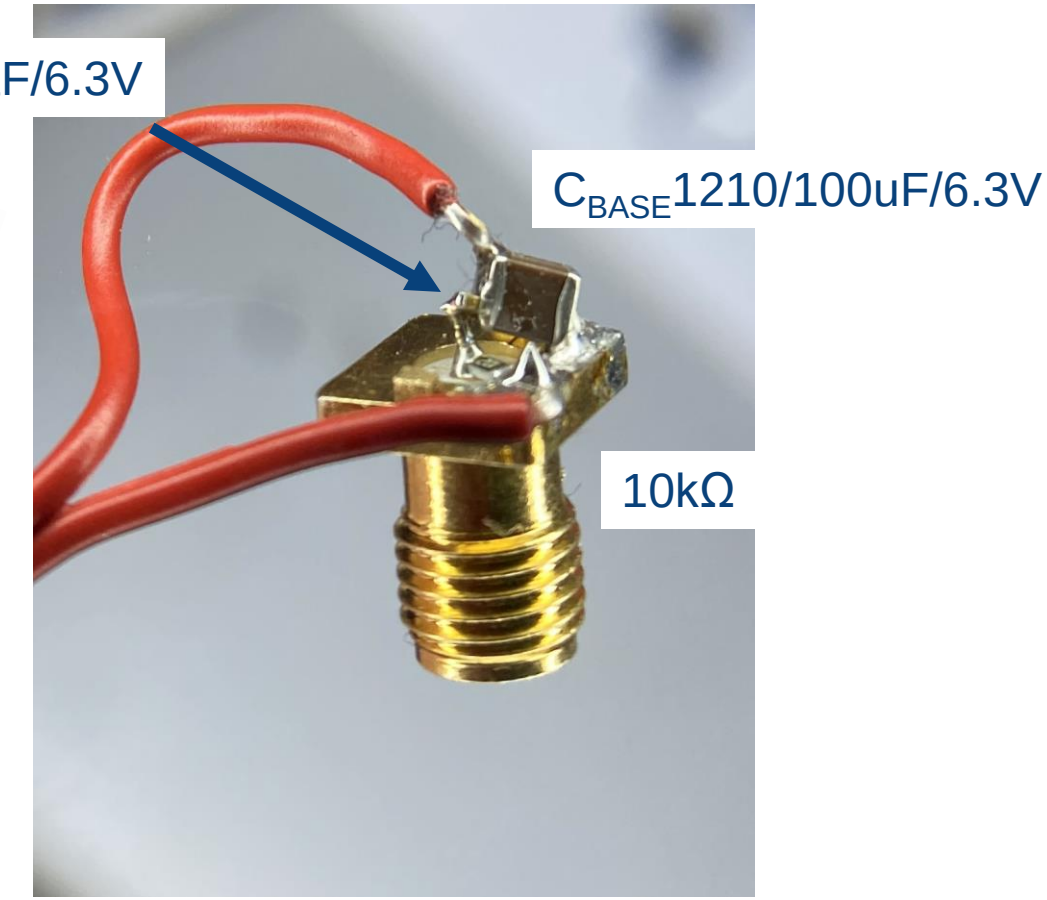
AC ripple plus DC-Bias - Test setup



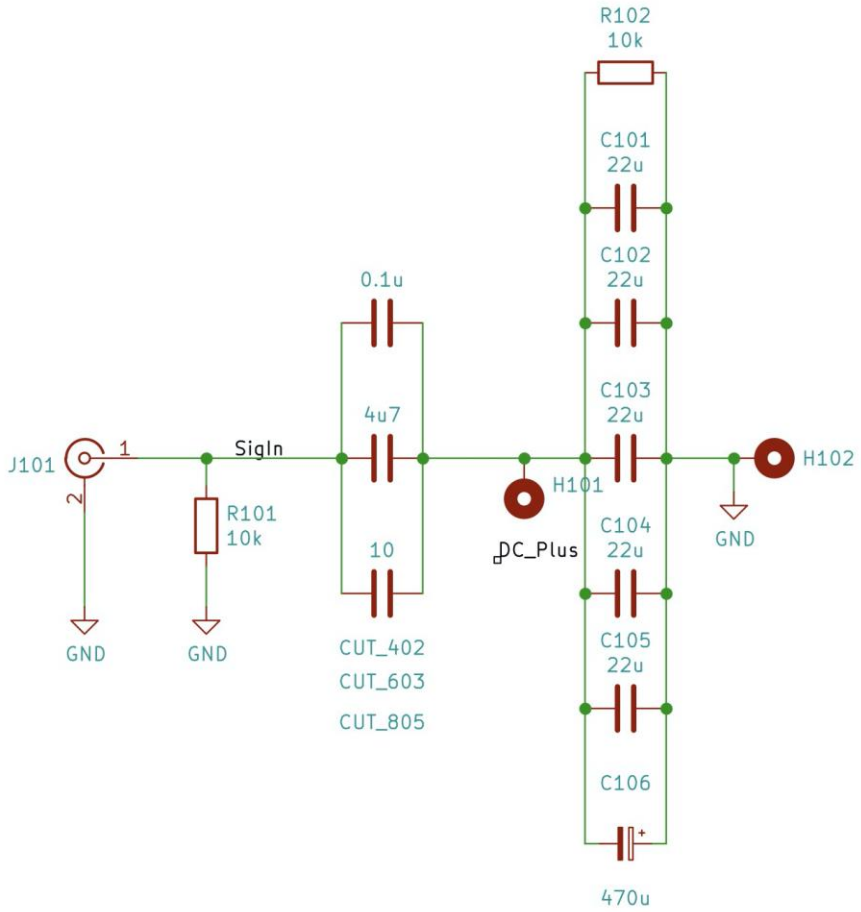


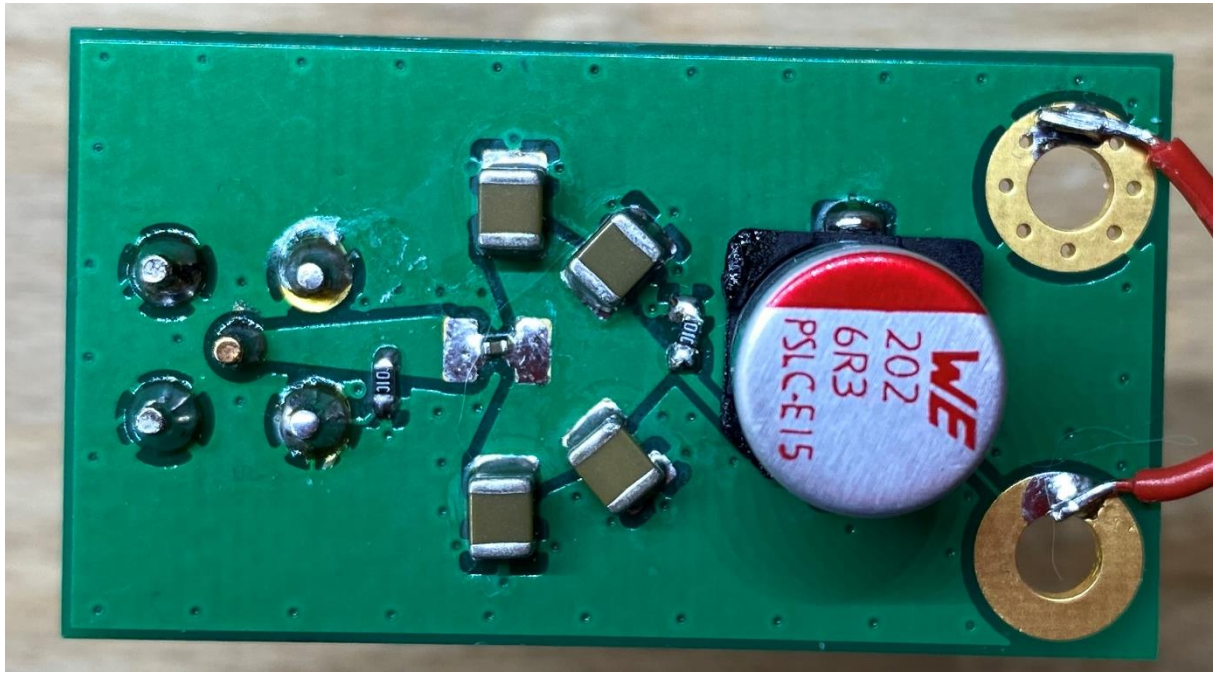
Test setup: How we started!





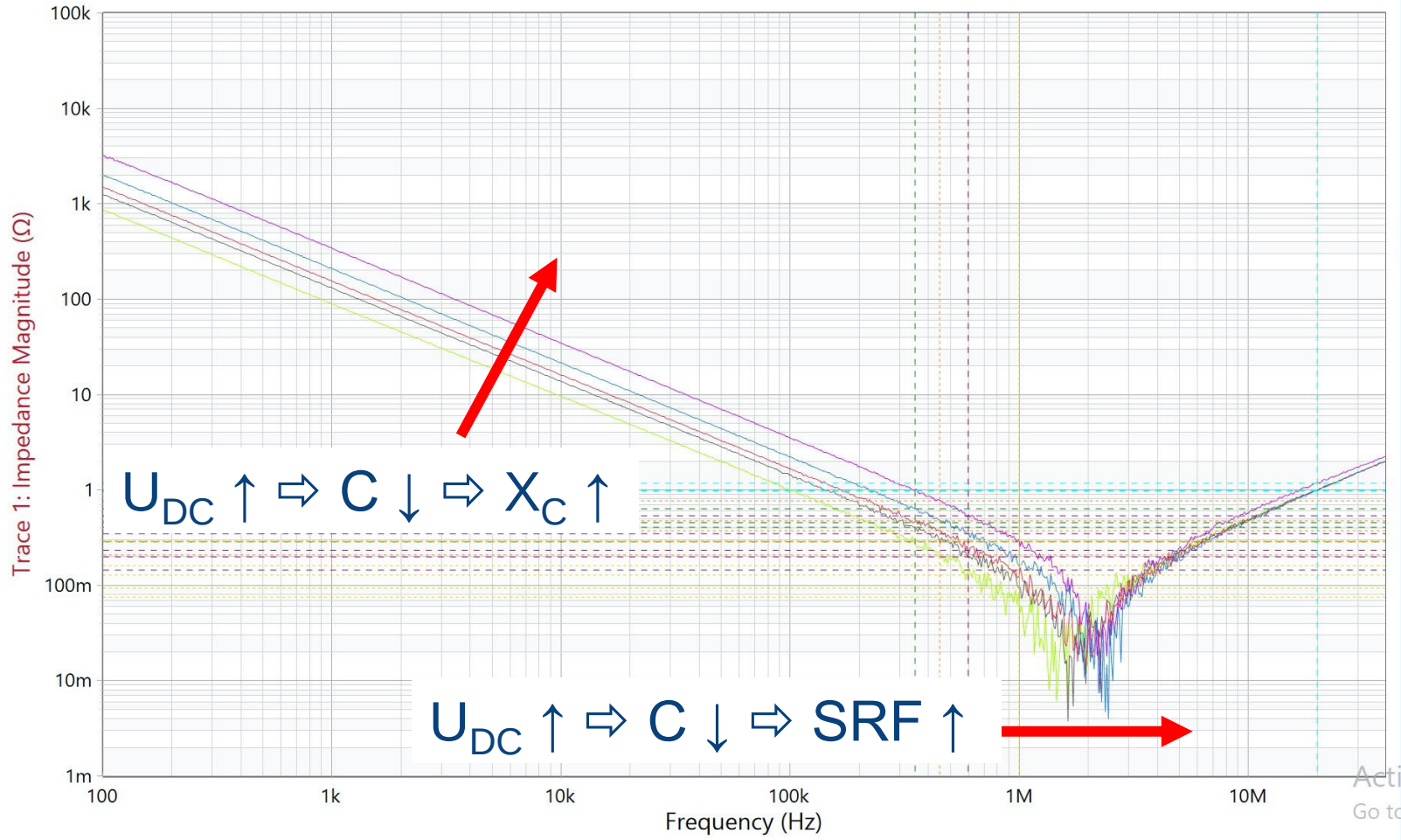
Schematic & PCB of the Testboard





Impedanz: Z = f(U_{DC}, freq)

	Frequency	0V -30dBm(18...	1V8 -30dBm(1...	2V3 -30dBm(1...	3V3 -30dBm(1...	5V -30dBm(-1...
Cursor 1	350 kHz	286,609 mΩ	405,507 mΩ	452,487 mΩ	632,542 mΩ	987,929 mΩ
Cursor 2	450 kHz	208,062 mΩ	285,436 mΩ	373,471 mΩ	475,012 mΩ	769,664 mΩ
Cursor 3	600 kHz	144,178 mΩ	198,817 mΩ	232,65 mΩ	347,51 mΩ	536,382 mΩ
Cursor 4	1 MHz	74,806 mΩ	93,568 mΩ	127,593 mΩ	160,316 mΩ	292,213 mΩ
Cursor 5	20 MHz	989,942 mΩ	978,568 mΩ	992,399 mΩ	973,015 mΩ	1,173 Ω



- Trace 1
- Trace 2
- 0V 10dBm(22dBm)...
- 1V8 10dBm(22) 040...
- 2V3 10dBm(22) 040...
- 3V3 10dBm(22) 040...
- 5V 10dBm(22) 0402...
- 0V -30dBm(18) 040...
- 1V8 -30dBm(18) 04...
- 2V3 -30dBm(18) 04...
- 3V3 -30dBm(18) 04...
- 0V -19dBm(-7) 0402...
- 1v8-19dBm(-7) 040...
- 2V3 -19dBm(-7) 040...
- 3V3 -19dBm(-7) 040...
- 5V -19dBm(-7) 0402...
- 0V -13dBm(-1) 0402...
- 1V8 -13dBm(-1) 040...
- 2V3 -13dBm(-1) 040...
- 3V3 -13dBm(-1) 040...
- 5V -30dBm(-18) 040...
- 5V -13dBm(-1) 0402...

Measurement → new memory

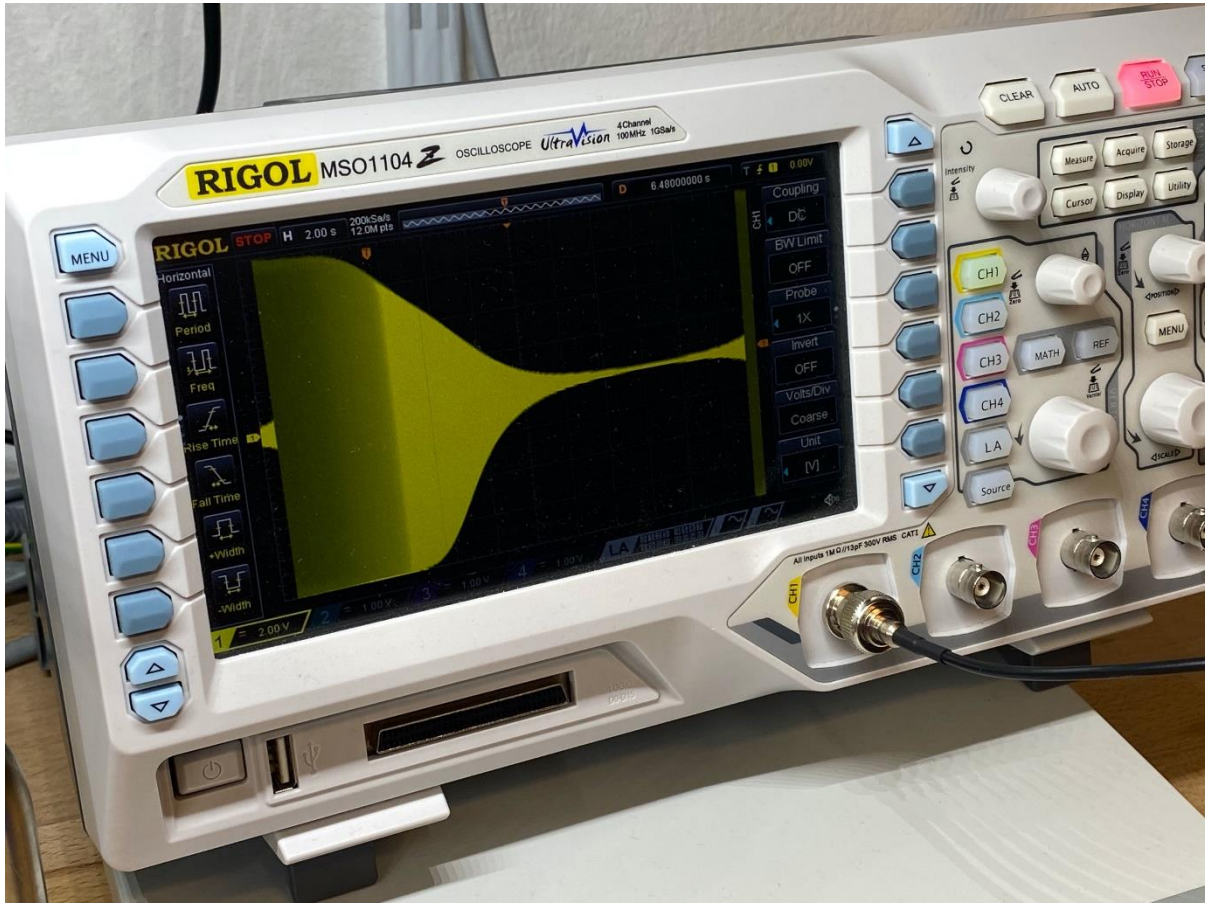
Capacity over Frequency and DC_{bias} ✓

Capacity over DC_{bias} and AC_{ripple} ?

Voltage across Capacitor

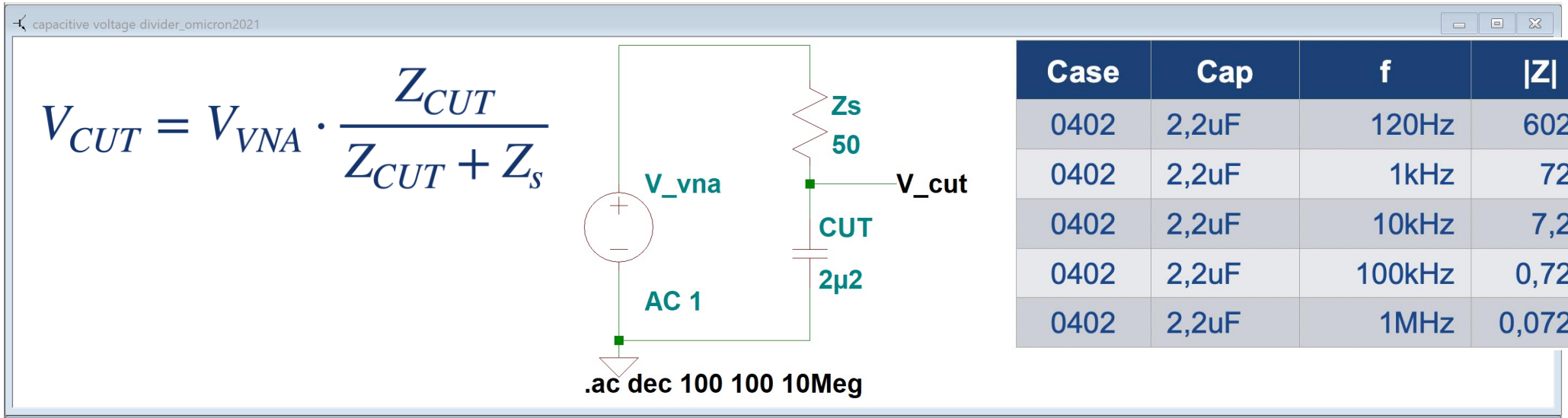
- Using 50Ω source: Bode 100
- Using our Test setup
- Frequency sweep
  - 100 Hz … 50MHz
- Shown voltage across CUT

Not constant at all!

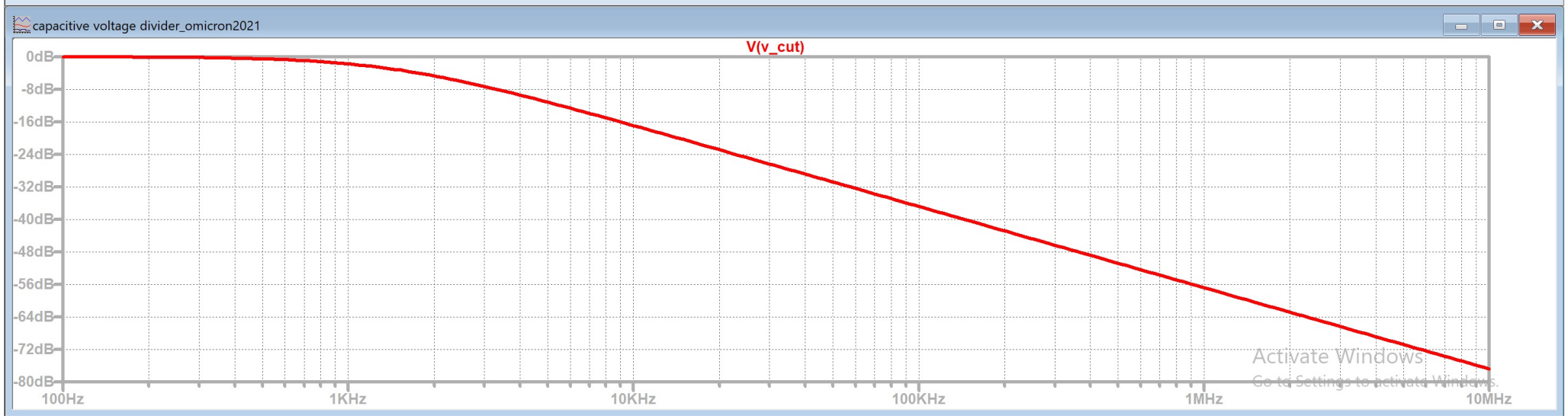


Voltage divider between Source impedance and CUT

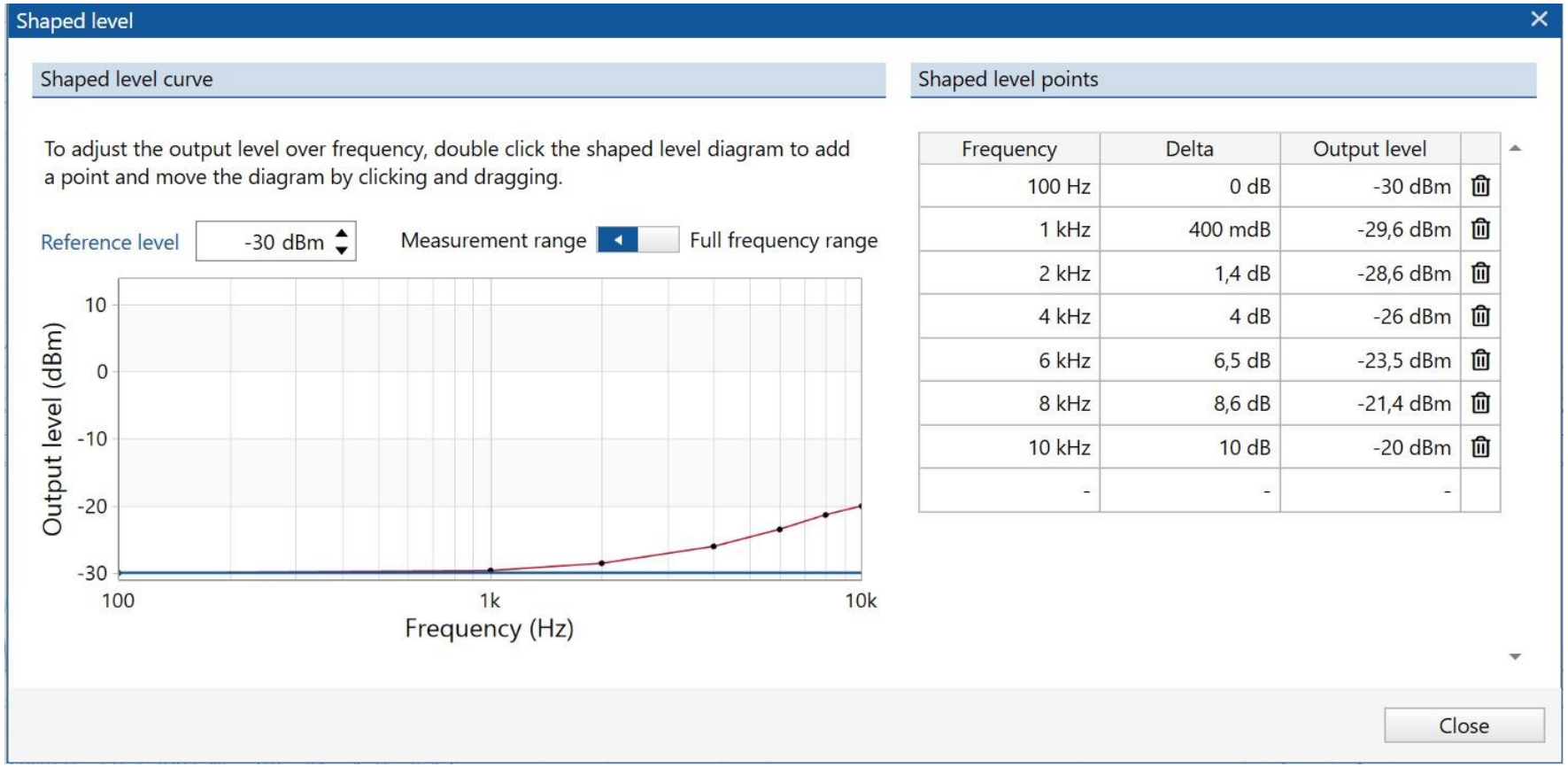
$$V_{CUT} = V_{VNA} \cdot \frac{Z_{CUT}}{Z_{CUT} + Z_s}$$



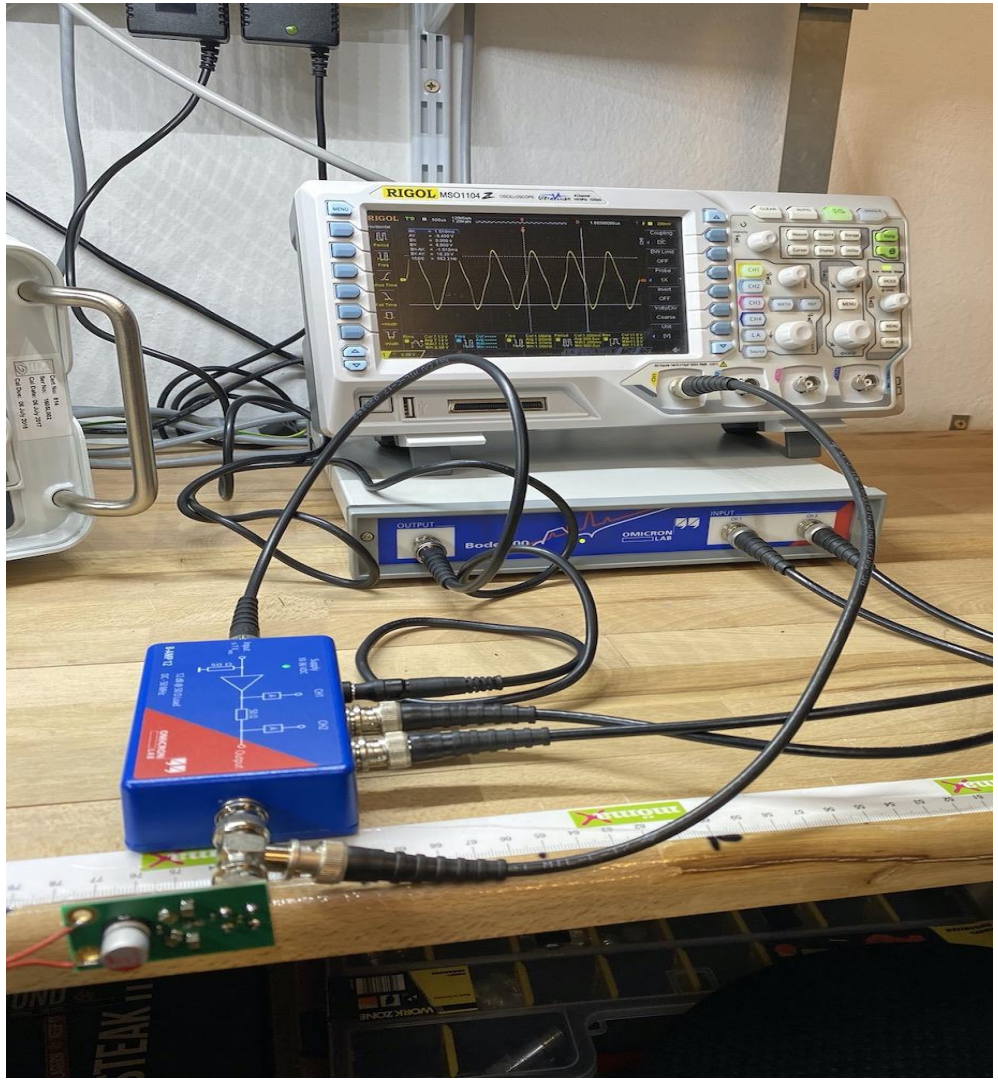
Case	Cap	f	|Z|	V_{CUT}
0402	2,2uF	120Hz	602Ω	0,923
0402	2,2uF	1kHz	72Ω	0,591
0402	2,2uF	10kHz	7,2Ω	0,126
0402	2,2uF	100kHz	0,72Ω	0,014
0402	2,2uF	1MHz	0,072Ω	0,001

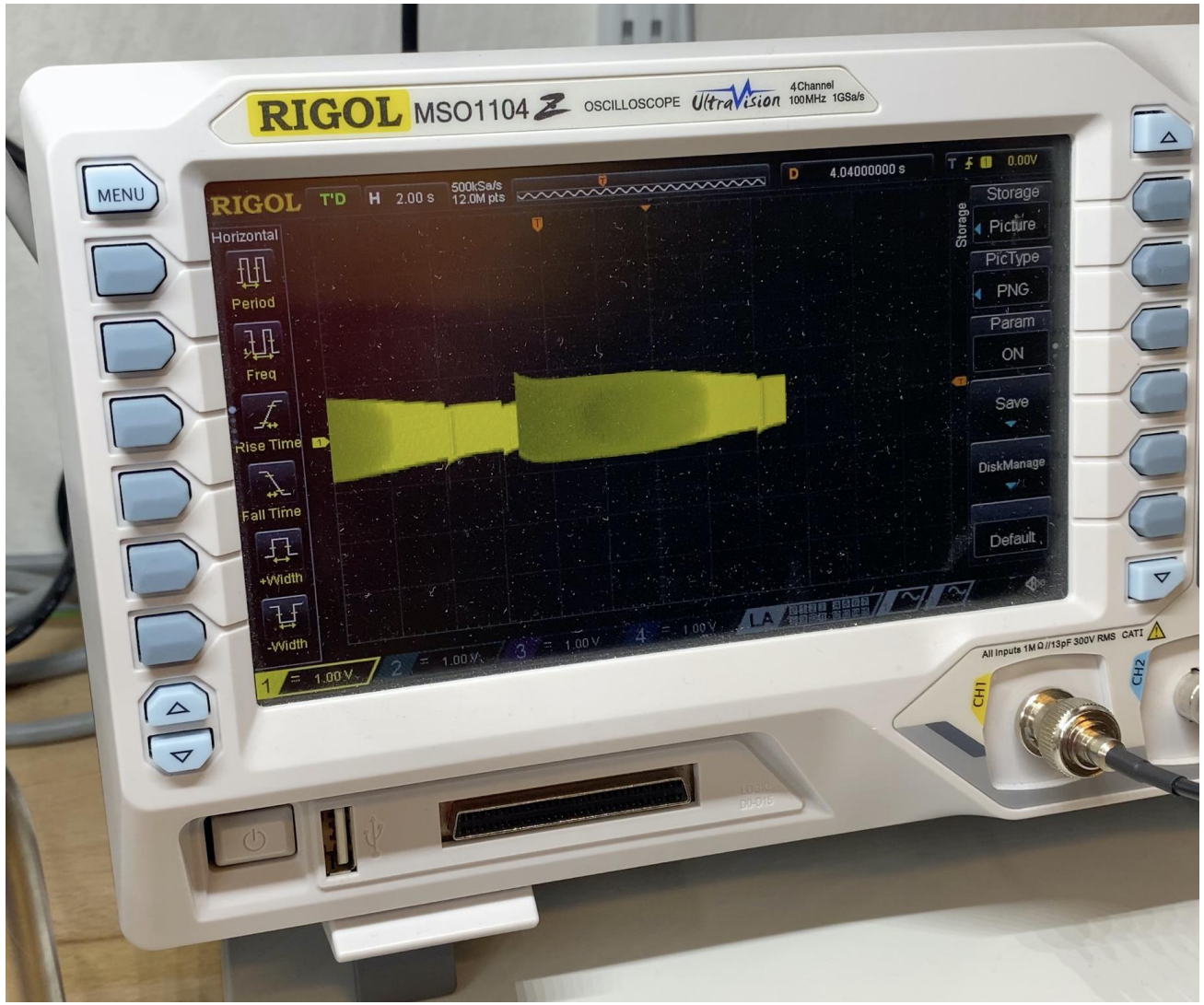


Level adjust over frequency



AC - Voltage across the capacitor

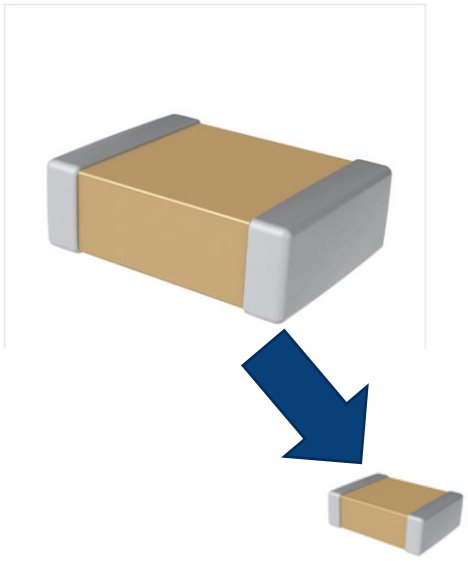




AC_ripple, 1210 vs 0402

- Bode 100 has not enough output power to test a 100µF on AC_ripple.
- Even with B-AMP 12 support:
  - Output power too low!
- Substitude MLCC 1210 by 0402:
  - C1210: 3.2 x 2.5 x 2.5 = 20mm³
  - C0402: 1.0 x 0.5 x 0.5 = 0.25mm³
- Volume ratio 80 : 1
- Let’s reduce Volume and Capacity similar:
  - C1210 ⇨ C0402
  - 100µF ⇨ 2.2µF

C1210C107M9PAC7210



C0402C225M9PACTU

(C0402C225M9PAC7867)

SMD Ceramic Commercial Grade

Power budget

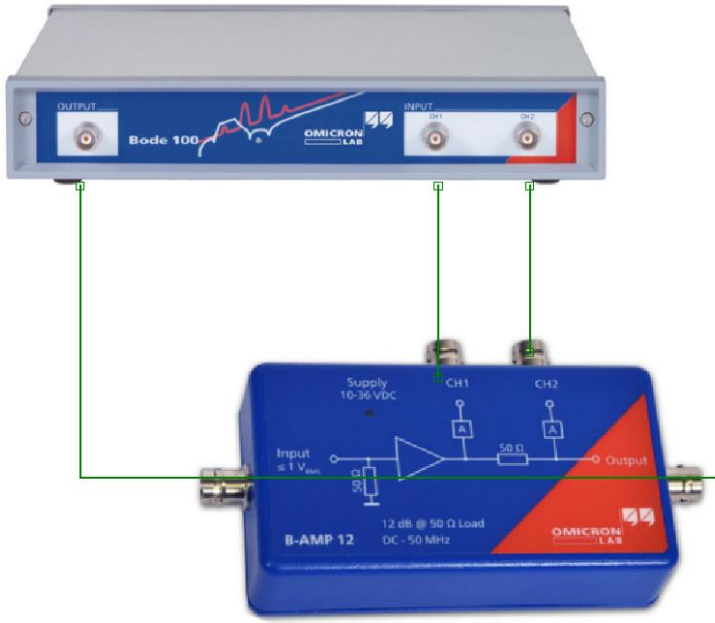
How much power (dBm) do I need to keep 1Vrms across CUT?

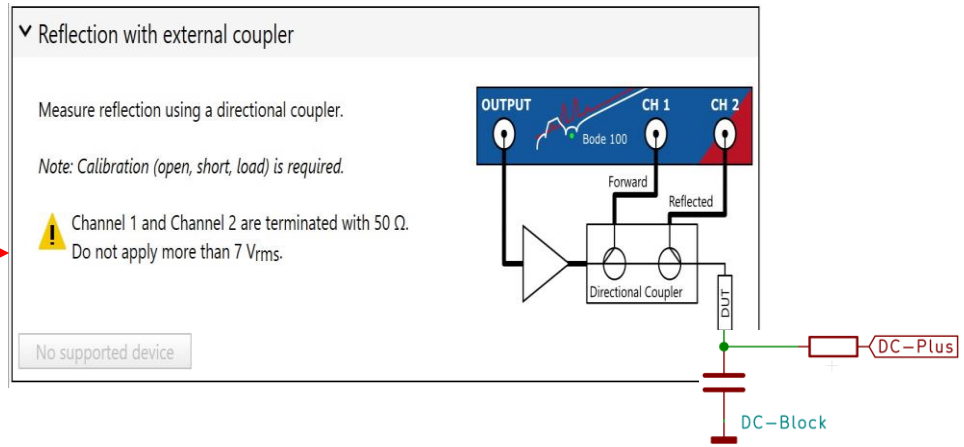
Freq	C	Xc	U_CUT	U_VNA	dBm_VNA
1.000	2,2E-06	72,343	1	1,69	18
10.000	2,2E-06	7,234	1	7,91	31
50.000	2,2E-06	1,447	1	35,56	44
100.000	2,2E-06	0,723	1	70,12	50
350.000	2,2E-06	0,207	1	242,90	61
650.000	2,2E-06	0,111	1	450,25	66
1.000.000	2,2E-06	0,072	1	692,15	70

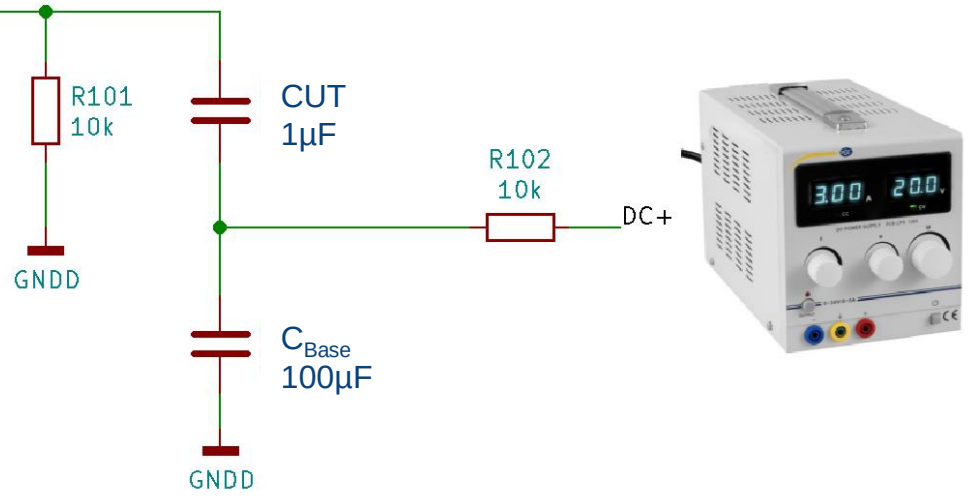
$$V = \sqrt{10^{\frac{dBm}{10}} \cdot Z \cdot 10^{-3}} \quad \Big| \quad Z = 50\Omega$$

$$dBm = 20 \cdot log_{10}(V) - 10 \cdot log_{10}(Z) + 30$$

Apply 25dBm AC and DC_{Bias}

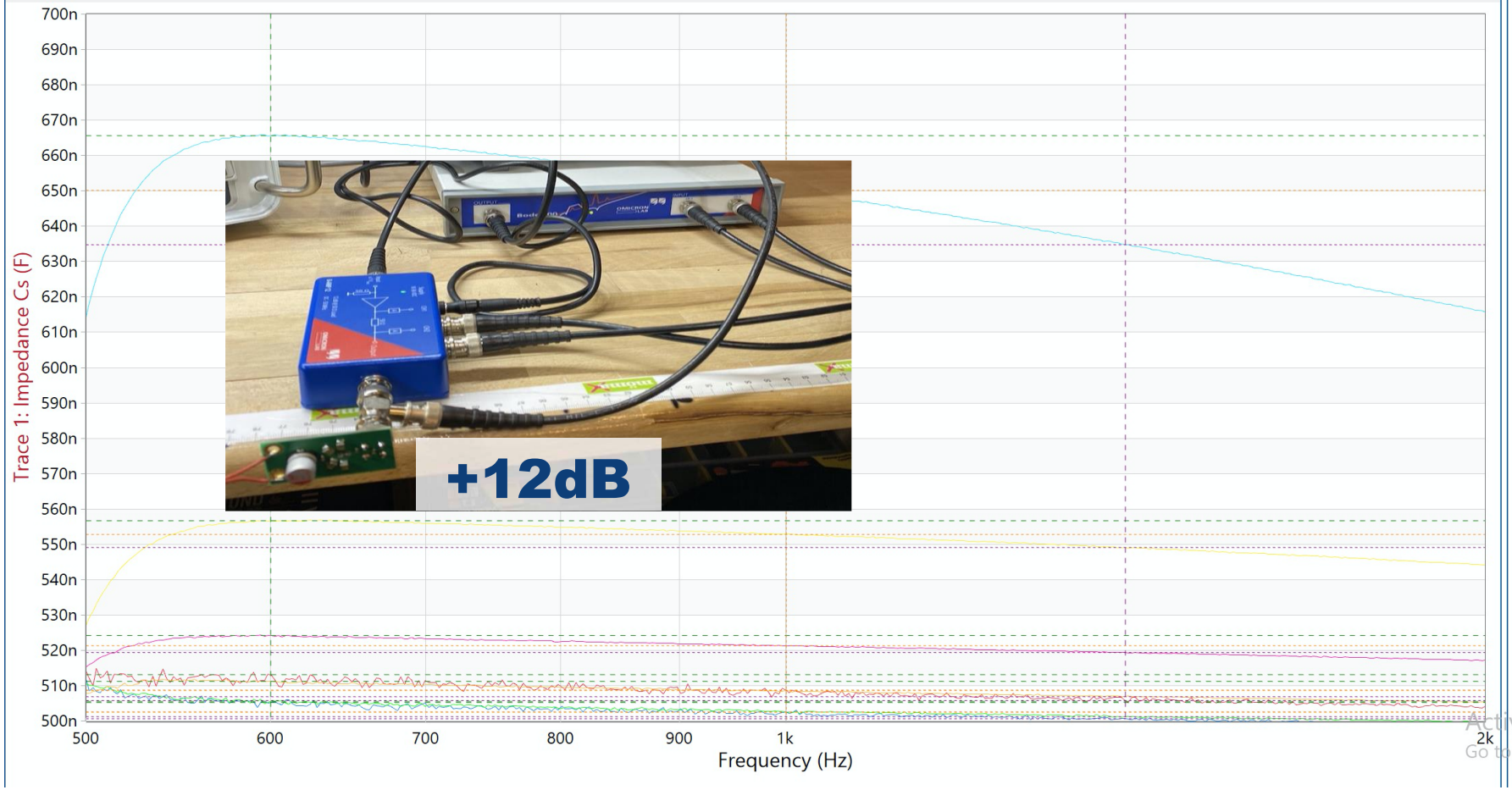






C = f(U_AC, freq) @ 5VDC

	Frequency	-30dBm, 5V0,...	-25dBm, 5V0,...	-19dBm, 5V0,...	-13dBm, 5V0,...	-7dBm, 5V0, ...	-1dBm, 5V0, ...	5dBm, 5V0, 0...	10dBm, 5V0, ...
Cursor 1	600 Hz	513,106 nF	505,229 nF	505,538 nF	511,206 nF	524,149 nF	556,67 nF	665,639 nF	880,355 nF
Cursor 2	1 kHz	508,748 nF	502,488 nF	502,598 nF	508,667 nF	521,319 nF	552,785 nF	650,117 nF	857,161 nF
Cursor 3	1,4 kHz	505,815 nF	500,651 nF	501,238 nF	506,87 nF	519,386 nF	549,08 nF	634,725 nF	824,951 nF



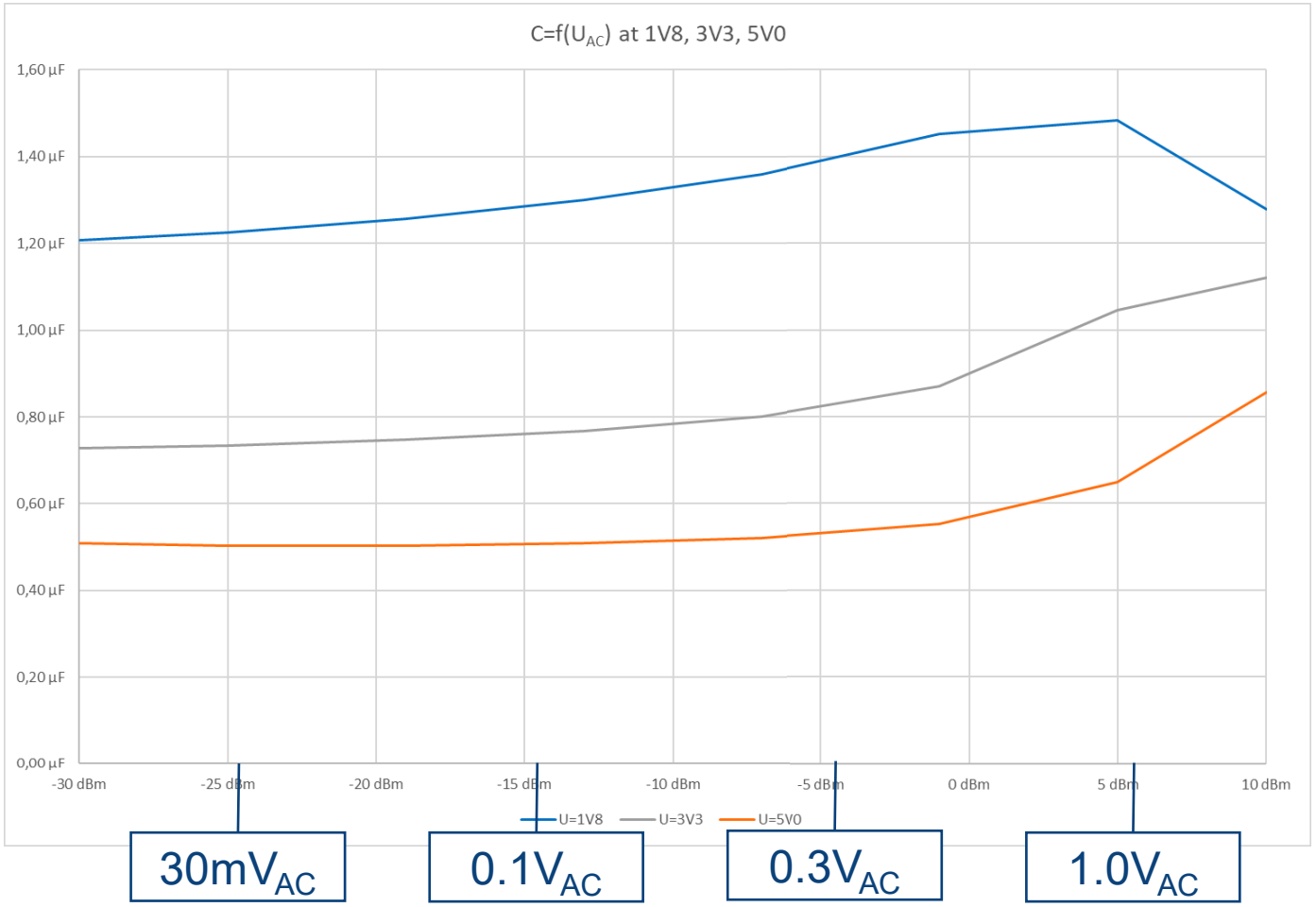
Trace 1
Trace 2
-30dBm, 1V8, 0402,...
-25dBm, 1V8, 0403,...
-19dBm, 1V8, 0403,...
-13dBm, 1V8, 0403,...
-7dBm, 1V8, 0403, 2...
-1dBm, 1V8, 0403, 2...
5dBm, 1V8, 0403, 2u2
10dBm, 1V8, 0403,...
-30dBm, 5V0, 0402,...
-25dBm, 5V0, 0402,...
-19dBm, 5V0, 0402,...
-13dBm, 5V0, 0403,...
-7dBm, 5V0, 0402, 2...
-1dBm, 5V0, 0402, 2...
5dBm, 5V0, 0402, 2u2
10dBm, 5V0, 0402,...

Measurement → new memory

C = f(U_{AC}) with various DC_{Bias}

Net capacitance

- Varies over U_{AC}
- Change is not steady
- On higher DC_{Bias} net capacitance may increase with increased U_{AC}
- A turn point may appear depending on DC_{Bias}, U_{AC}



Wrap up

- Simple superimpose the effects does not reflect the real behavior
- Measure according to standards does not reflect SMPS requirements
- Capacitor behave different in SMPS applications
- Consider the voltage conditions across the capacitor under test

One last thing

- We have 10 PCB left over
- If you are interested to do your own investigation send an email to

  axelschmidt@kemet.com

- We sell at cost the PCB plus the BNC connector