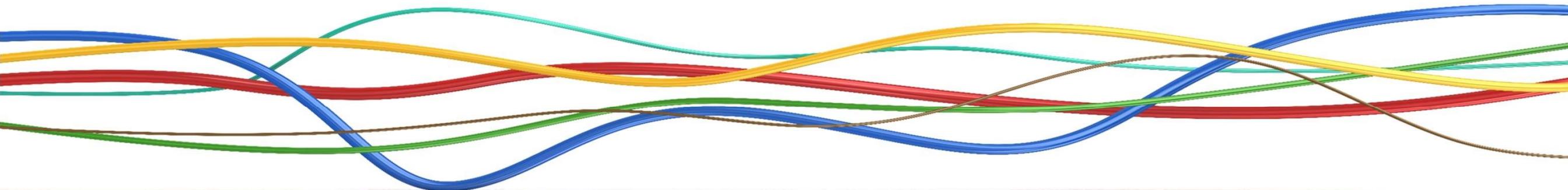


# 10<sup>th</sup> Power Analysis & Design Symposium

March 10<sup>th</sup>, 2021 - Worldwide (Virtual)

**Seamless Software Adaptation of High Performance Power Modules in Power Distribution Networks**  
by Andreas Reiter - Microchip Technology



# Seamless Software Adaptation of High- Performance Power Modules in Power Distribution Networks



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

Presented by **Andreas Reiter** – 10<sup>th</sup> March 2021  
10<sup>th</sup> Power Analysis & Design Symposium 2021

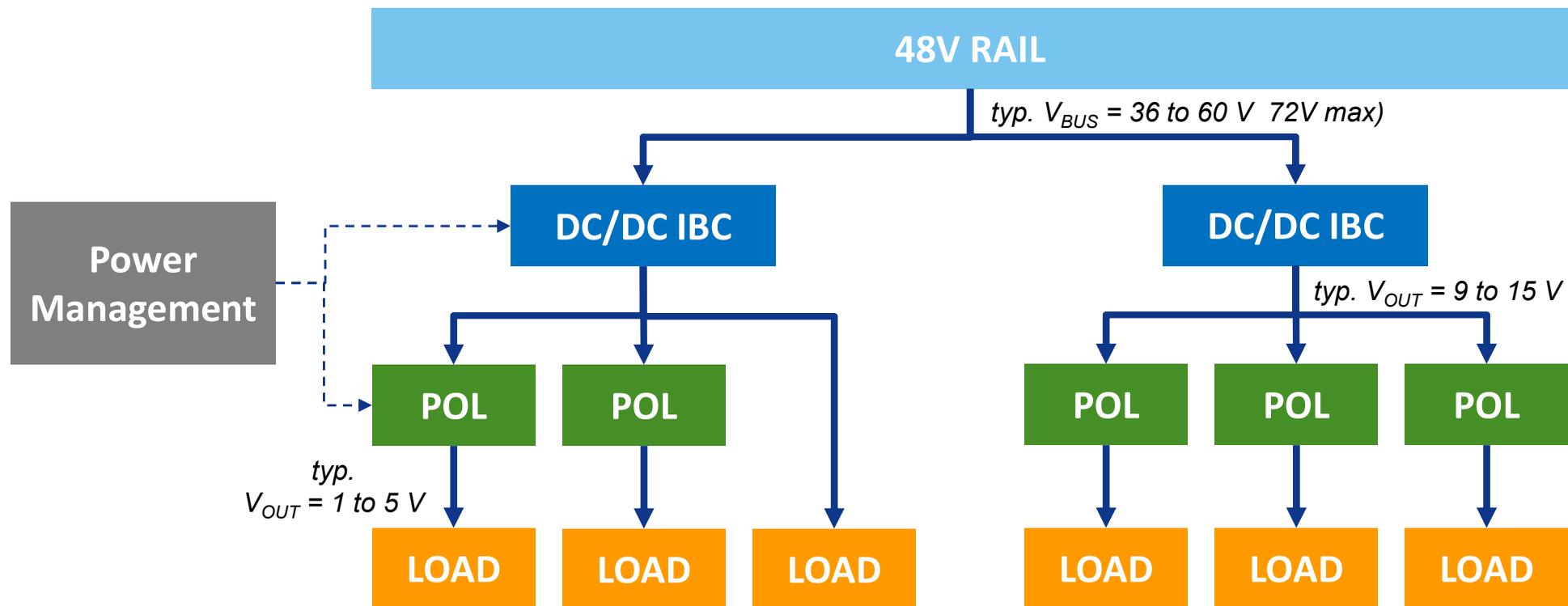
# Agenda

- **48V Rack Power Distribution Networks and Conversion Points**
- **300W 48V 1/16<sup>th</sup> Brick DC/DC Converter Power Module**
  - EPC9143: Unidirectional Power Module
  - EPC9151: Bi-Directional Power Module
- **High-Speed Multiphase Controller Design**
  - Type IV Adaptive Voltage Mode Control
  - PWM Steering and High-Speed Current Balancing
- **Summary**

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# Intermediary Bus Converters (IBC)



# Market Driver for High Power Density IBCs



- **5G Systems require up to three times more power than their 4G/LTE counterpart**
  - Majority of power consumption by 64T64R MIMO array vs. 4T4R of 4G/LTE
  - Higher Transmitter and Receiver Bandwidth requires faster data processing with more/faster CPUs/FPGAs
- 
- **The cost of a 5G Base Station is ~4x of 4G/LTE**
  - Increased cost pressure

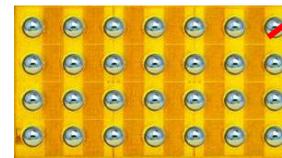
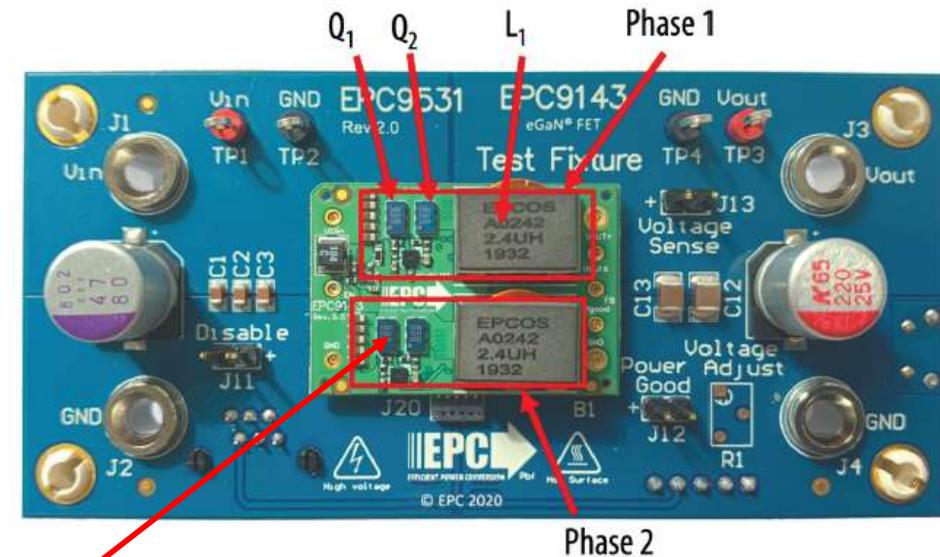
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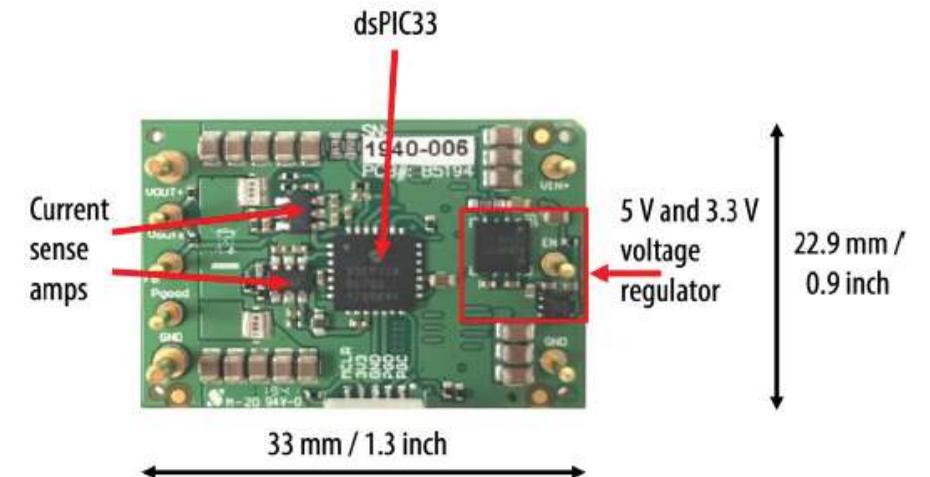
# EPC's 300W 1/16th Brick IBC Converters

## Reference Design Features

- Microchip dsPIC33CK digital signal controller
- EPC2053 eGaN<sup>®</sup> FETs with 3.2 mΩ RDS(on)
- Two-phase synchronous buck topology
- 48 V in -> 5 to 15 V out
- 25 A maximum I out
- Power density: 650 to 748 W/in<sup>3</sup>
- Output power: 300 W
- Peak efficiency: 94.8 – 96.3 %
- Size: (33 x 22.9 x 9) mm  
(1.3 x 0.9 x 0.35)"



**EPC2053**  
**eGaN<sup>®</sup> FET**  
100 V, 3.2 mΩ  
3.5 mm x 2.0 mm



# EPC9143 Reference Design vs. Off-The-Shelf Silicon MOSET Module

- EPC9143
- $V_{IN}$ : 10...61 V DC <sup>(1)</sup>
- $V_{OUT}$ : 3.3 ... 15 V DC
- $I_{OUT}$ : 25 A max (23 A @ 15 V DC)  
@ 800 LFM airflow
- Power Density: **748** W/in<sup>3</sup> <sup>(2)</sup>



- (1): 73 V max, not operational
- (2): max. power density @  $V_{OUT}$ =15 V, 23 A  
650 W/in<sup>3</sup> @  $V_{OUT}$ =12 V, 25 A

- Vendor T Module
- $V_{IN}$ : 9...53 V DC
- $V_{OUT}$ : 3.3 ... 15 V DC
- $I_{OUT}$ : 20 A max <sup>(3)</sup>  
@ 800 LFM airflow
- Power Density: **483** W/in<sup>3</sup>



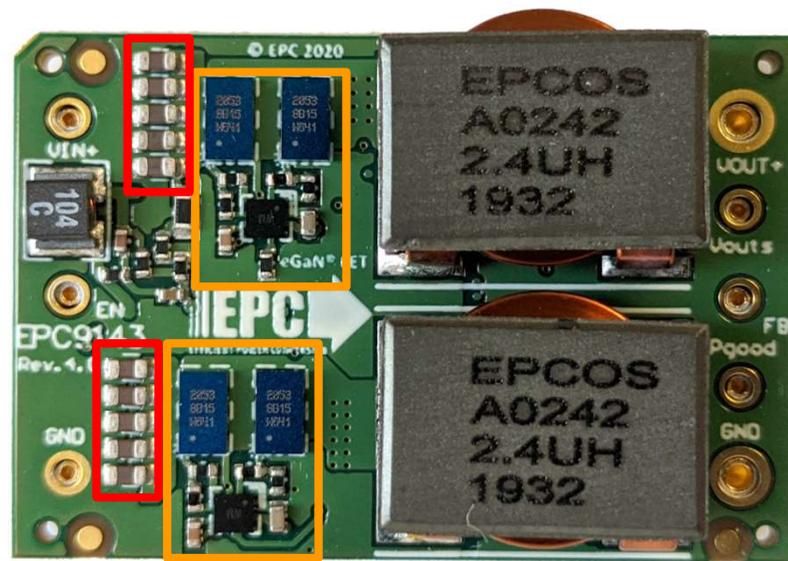
- (3): data sheet value, but power density limited to max. 480 W/in<sup>3</sup>

# EPC's 300W 1/16th Brick IBC Converters

## Two modules tailored for different applications

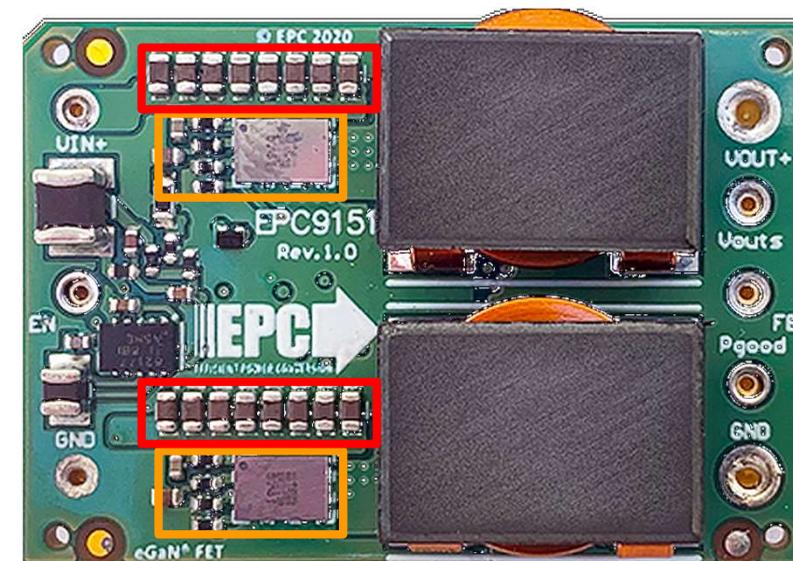
- **EPC9143 Unidirectional 16<sup>th</sup> Brick**

- Discrete half-bridge design
- uP1966A gate driver +  
2x EPC2053 100V eGaN FET
- Peak Efficiency > 96%
- Target Applications: Telecom IBC



- **EPC9151 Bi-Directional 16<sup>th</sup> Brick**

- Integrated half-bridge design
- EPC2152 ePower™ stage
- Peak Efficiency > 95%
- Target Applications:  
Automotive, Aerospace

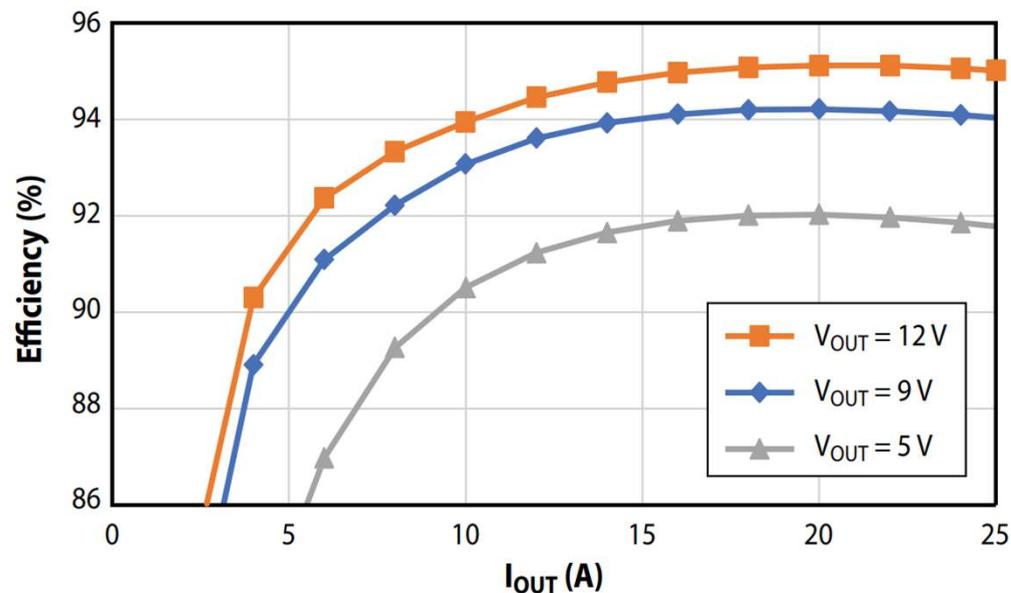


# EPC's 300W 1/16th Brick IBC Converters

## Two modules tailored for different applications

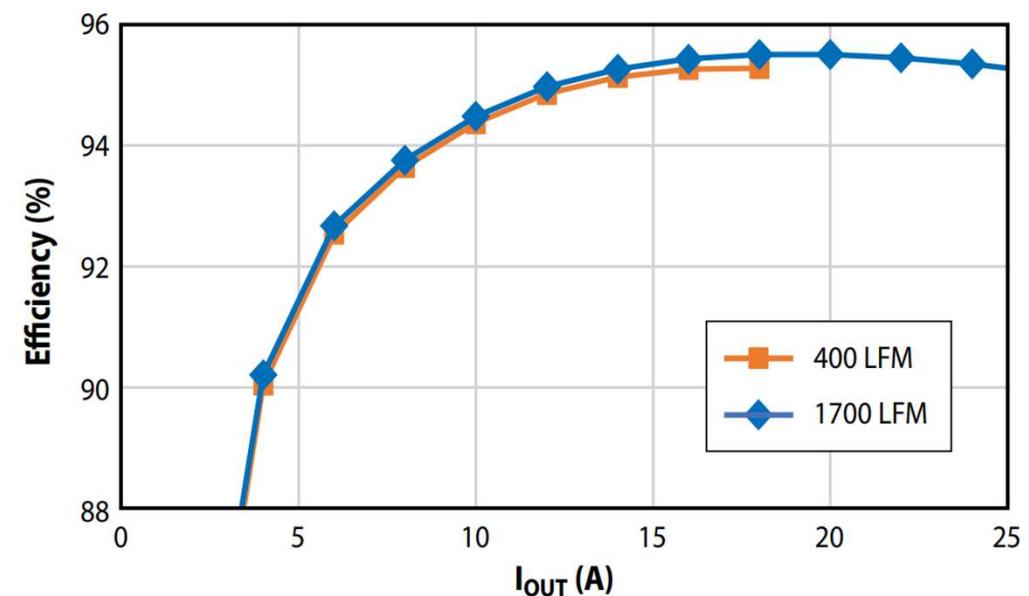
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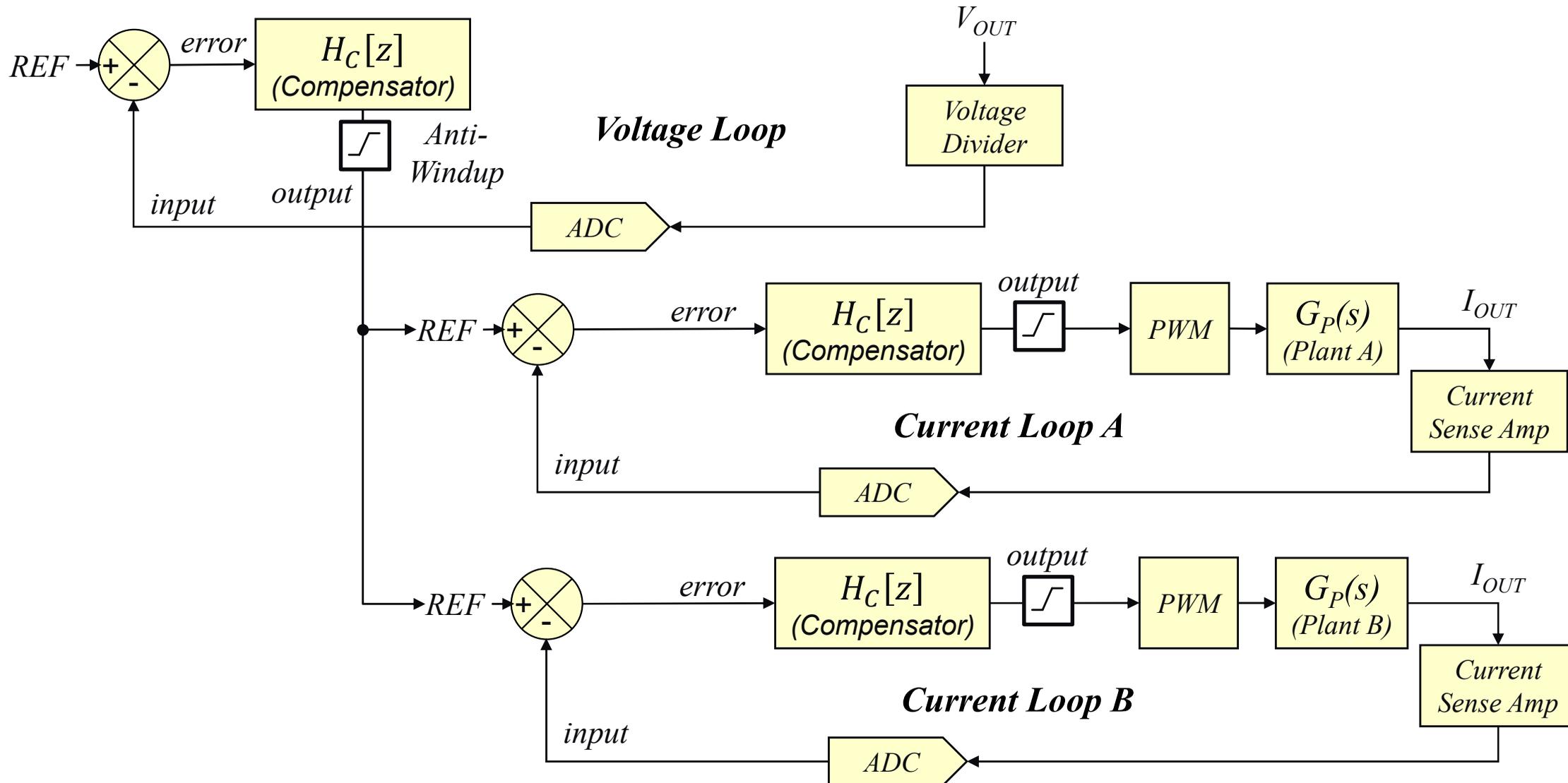


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# Average Current Mode Control

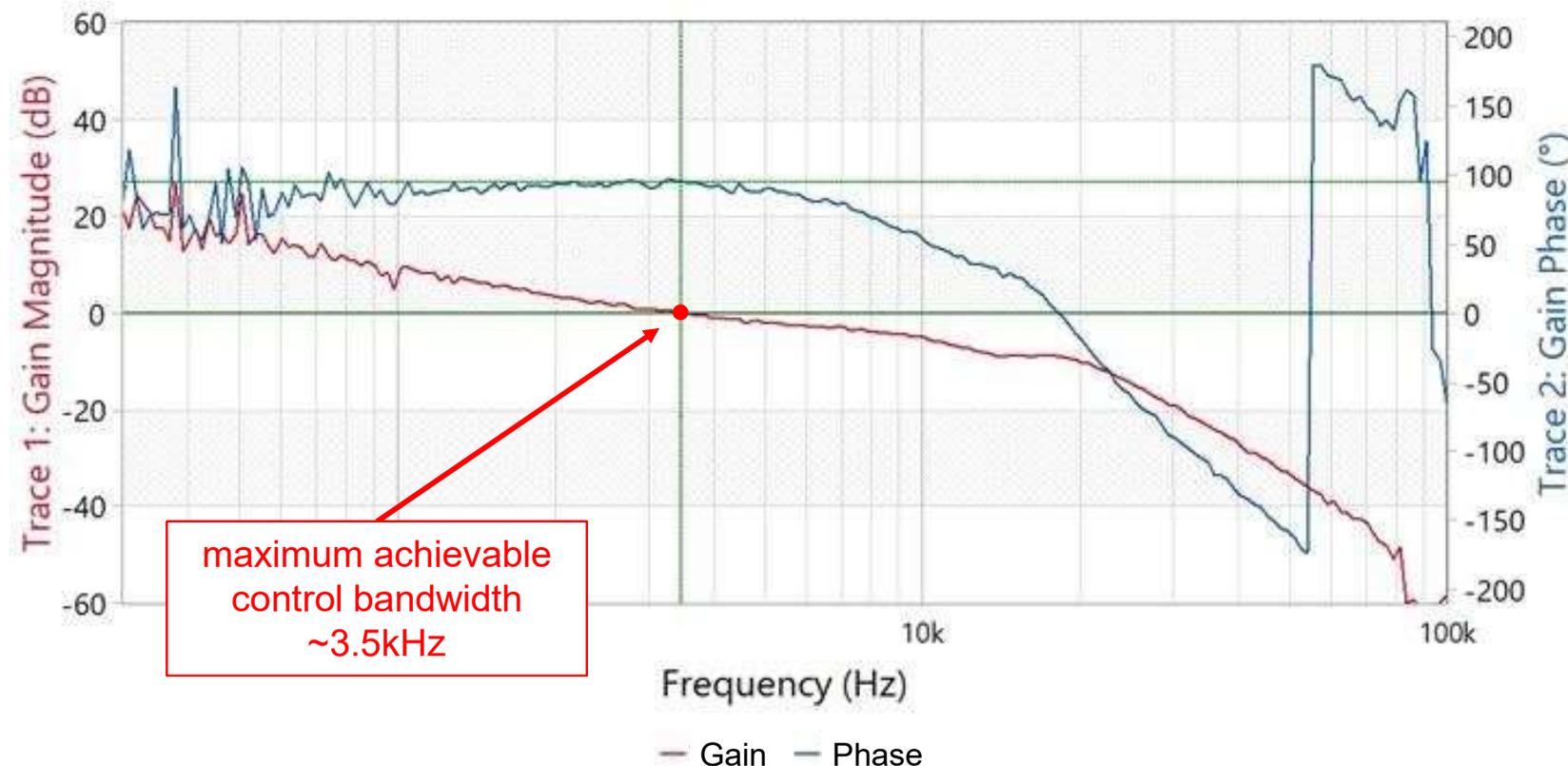
## Conventional Multiphase Converter Control Scheme



# Average Current Mode Control

## Conventional Multiphase Converter Control Scheme

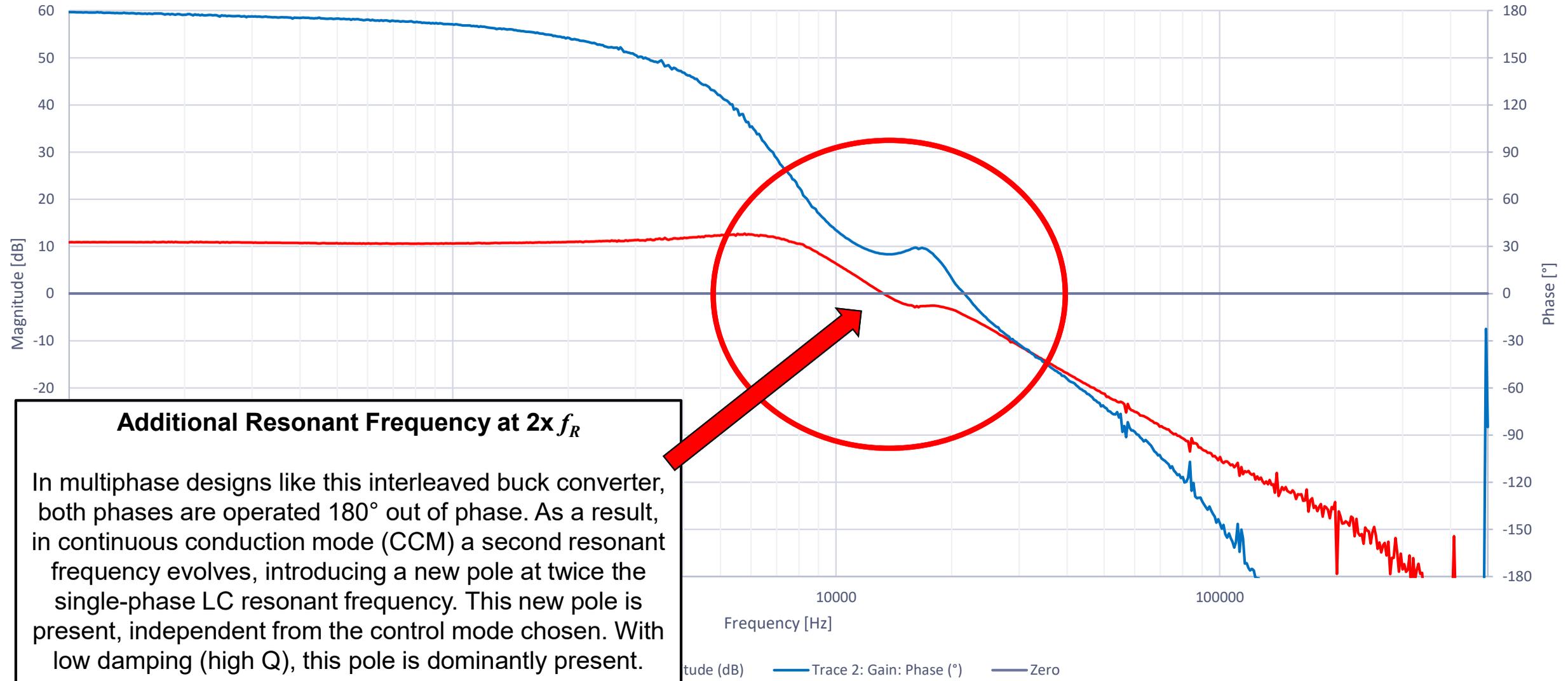
In average current mode control (ACMC), the total achievable bandwidth is limited by the maximum allowed perturbation frequency of the reference provided to the two, independent inner current loops in relation to their maximum cross-over frequency (here  $\sim 10\text{kHz}$ ). Outer voltage loop and inner current loop are executed at the same frequency. The ratio of their respective cross-over frequencies  $f_X$  is adjusted to limit the maximum perturbation frequency. As a result, the second resonant pole occurs in a negative gain region, where it is uncritical.



$f_{sw} = 500\text{ kHz}$   
 $f_X = 3.5\text{ kHz}$   
 $\Phi_{PM} > 90^\circ$   
 $GM < -12\text{ dB}$

# High Efficiency Multiphase Plant

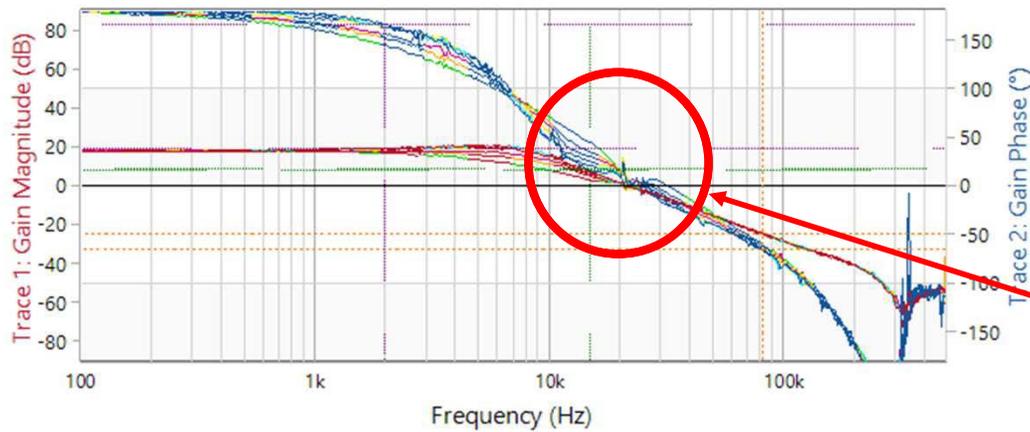
EPC9143 Plant Transfer Function



# EPC's 300W 1/16<sup>th</sup> Brick IBC Converters

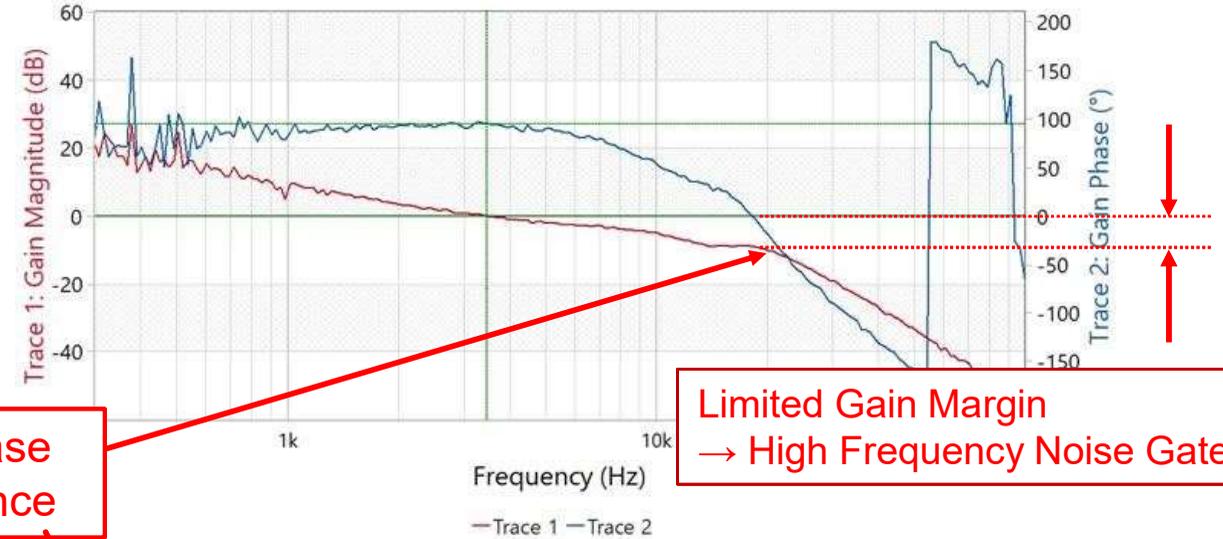
## Why Type IV Control in AVMC?

Plant Transfer Functions



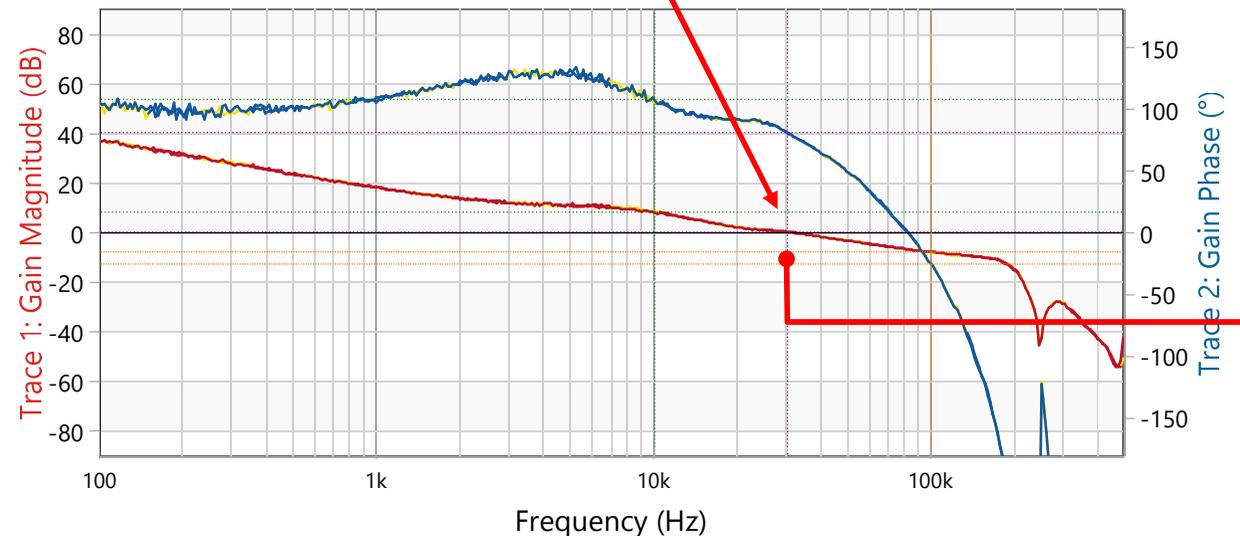
Multiphase Resonance

Open Loop TF Average Current Mode Control (ACMC)



Limited Gain Margin  
→ High Frequency Noise Gate

Open Loop TF Adaptive Voltage Mode Control (AVMC)



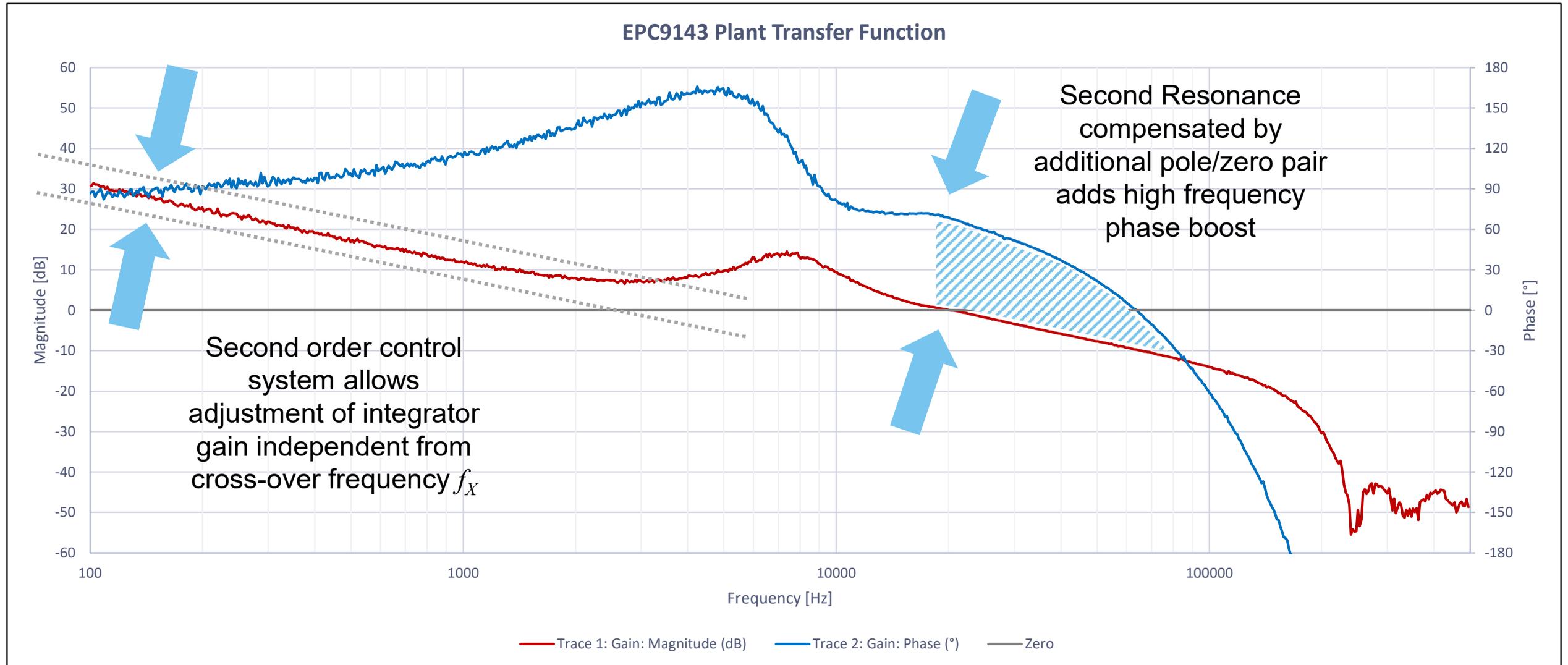
Pushing cross-over frequency beyond 20 kHz results in flat gain region near 0 dB (conditional stability)

Higher order systems allow placements of additional poles and zeros. In digital loops, these can either be real or complex conjugate poles and zeros.

One additional pole/zero pair is used to damp the second resonant bump.

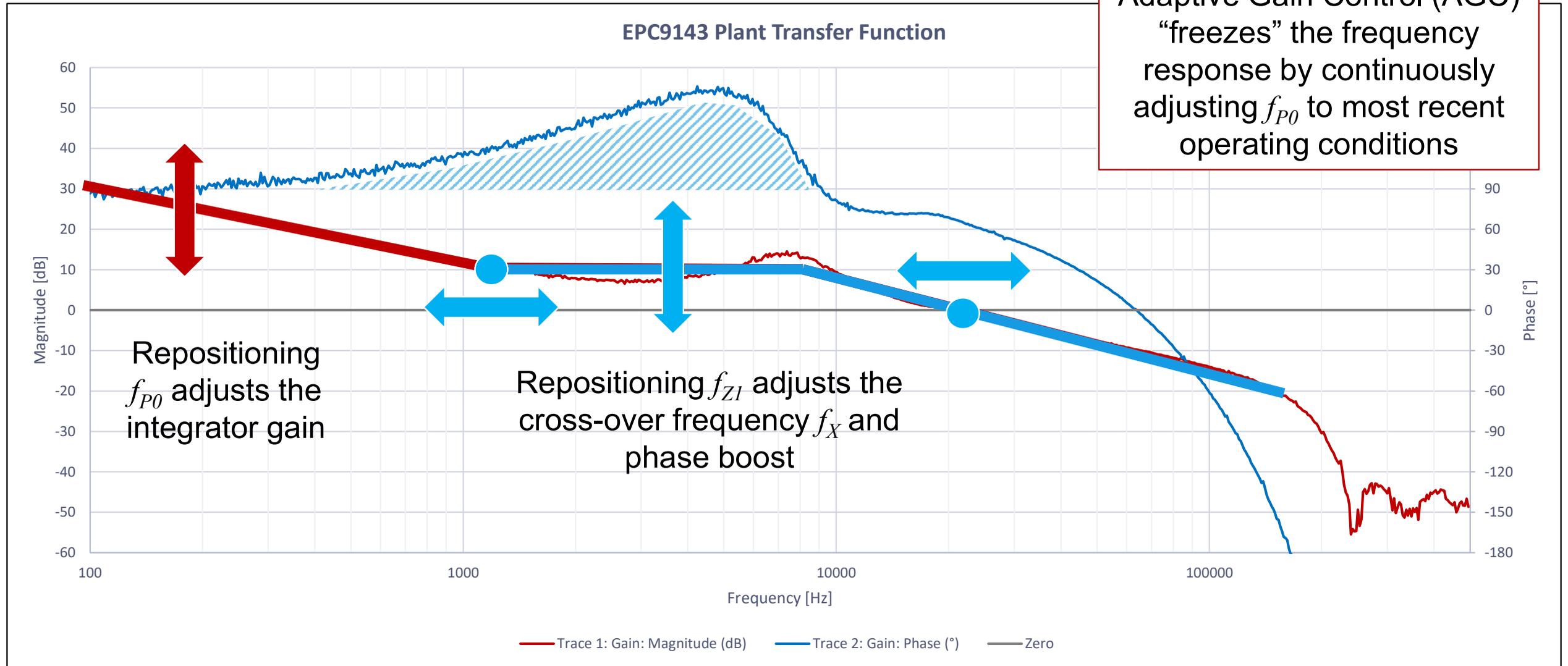
# Type IV Adaptive Voltage Mode Control

## Frequency Response Adjustment



# Type IV Adaptive Voltage Mode Control

## Frequency Response Adjustment



# Type IV Adaptive Voltage Mode Control

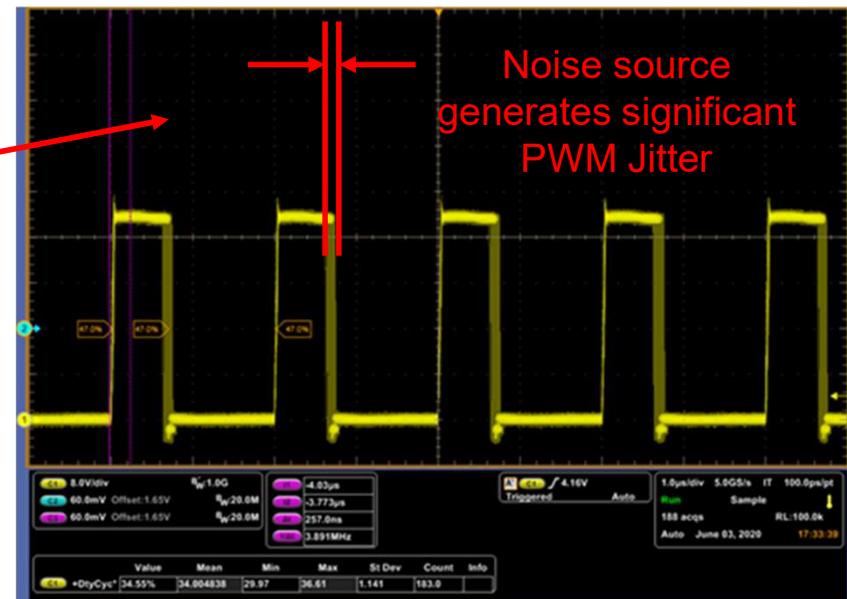
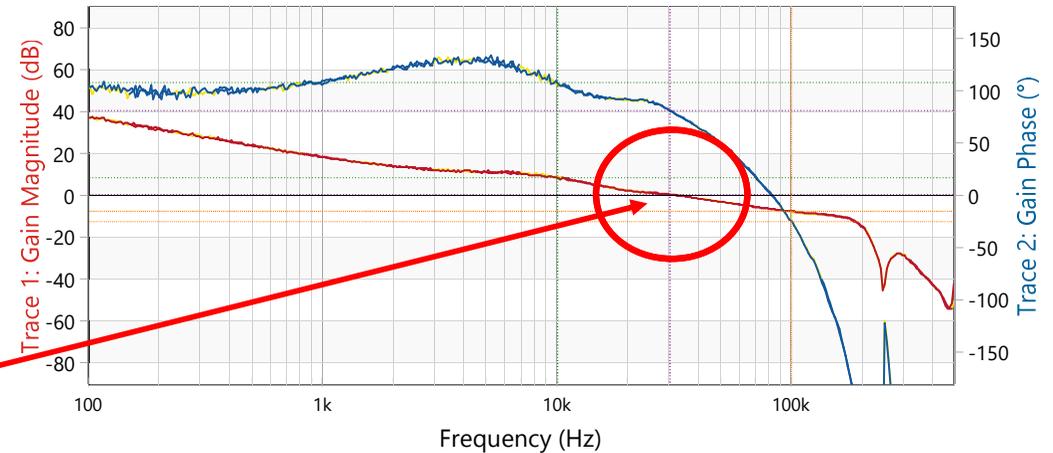
## Adjustment Limits

Theoretically there is no limitation of the maximum cross-over frequency  $f_X$  other than the physical limitations given by the switching frequency. Hence, high control bandwidth can be achieved.

However, in this design, if the cross-over frequency  $f_X$  matches the location of the second resonant frequency, **a conditionally stable region appears.**

This conditionally stable region results in poor noise rejection in this flat area region. This noise is picked up by the ADC, passes the control loop at a gain close to =1 and gets amplified at the PWM output as **observable jitter.**

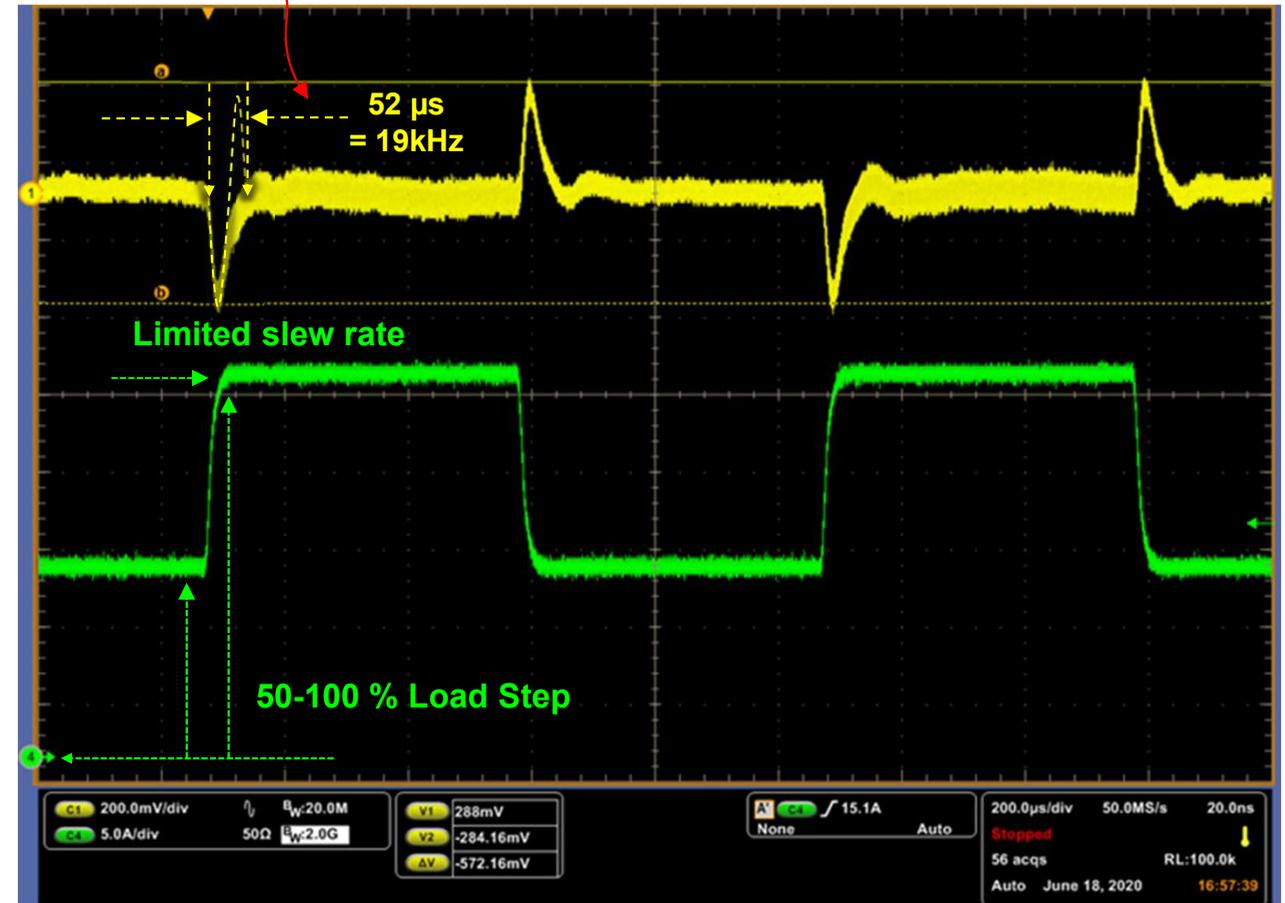
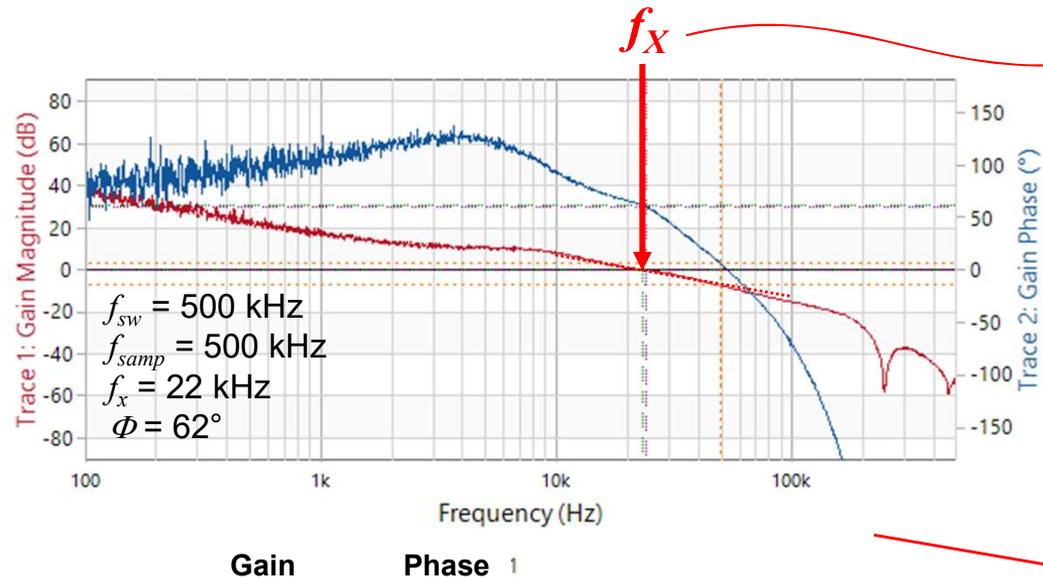
Open Loop TF Adaptive Voltage Mode Control (AVMC)





# Type IV Adaptive Voltage Mode Control

## Large Signal Validation of Type IV AVMC



After introducing adaptive gain modulation and the additional pole-zero-pair, the loop got adjusted for better phase margin of  $\Phi > 60^\circ$ . At  $f_x$ , the gain slope meets exact -20 dB/dec and then rolls off softly at higher frequencies.

The measured  $f_x = 22 \text{ kHz}$  in the frequency domain correlates sufficiently with the step response frequency in the time domain of  $f_{STEP} = 19 \text{ kHz}$ .

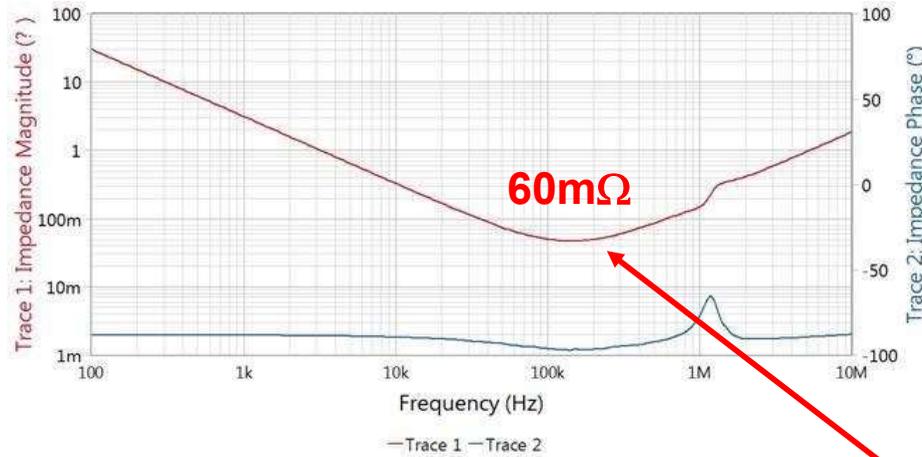
# Type IV Adaptive Voltage Mode Control

## Impedance Tuning

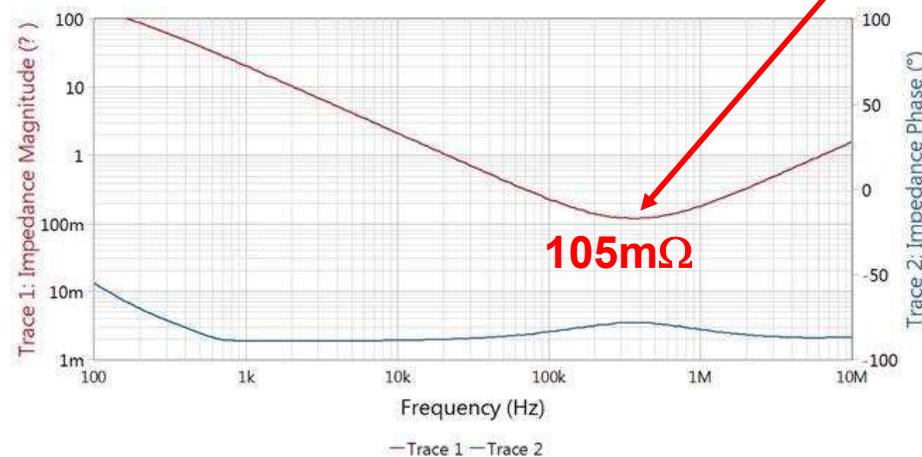
Recommended:  
Check component  
values independent  
from circuit for verification



EPC9531 Test Fixture

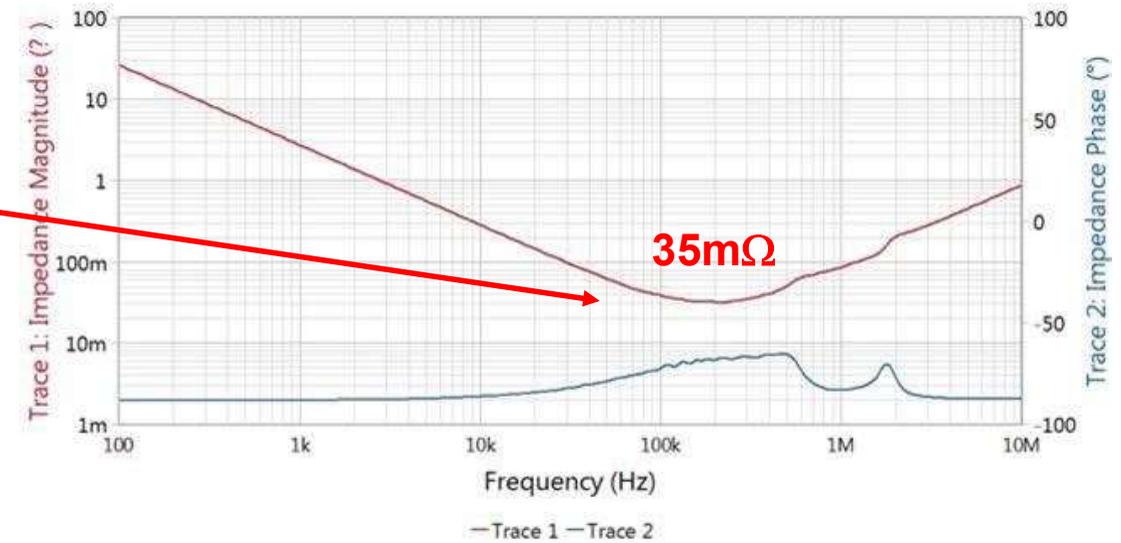


EPC9143 16<sup>th</sup> brick Power Module



Effective  
Capacitor  
ESR

EPC9143 mounted on EPC9531



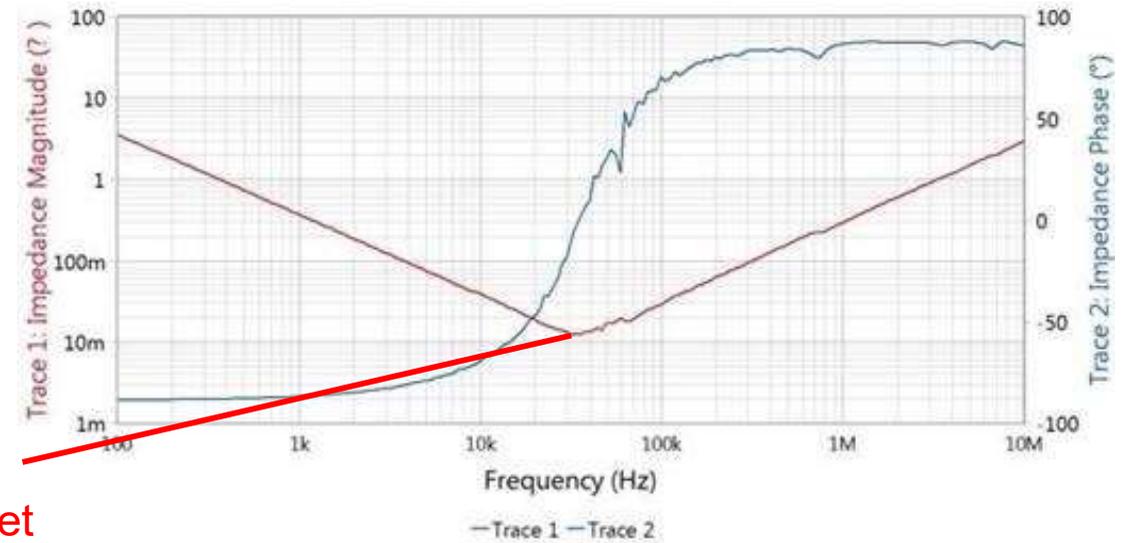
Measurements are taken at board terminals. Value Effective Capacitor ESR therefore includes additional resistance of traces.

# Type IV Adaptive Voltage Mode Control

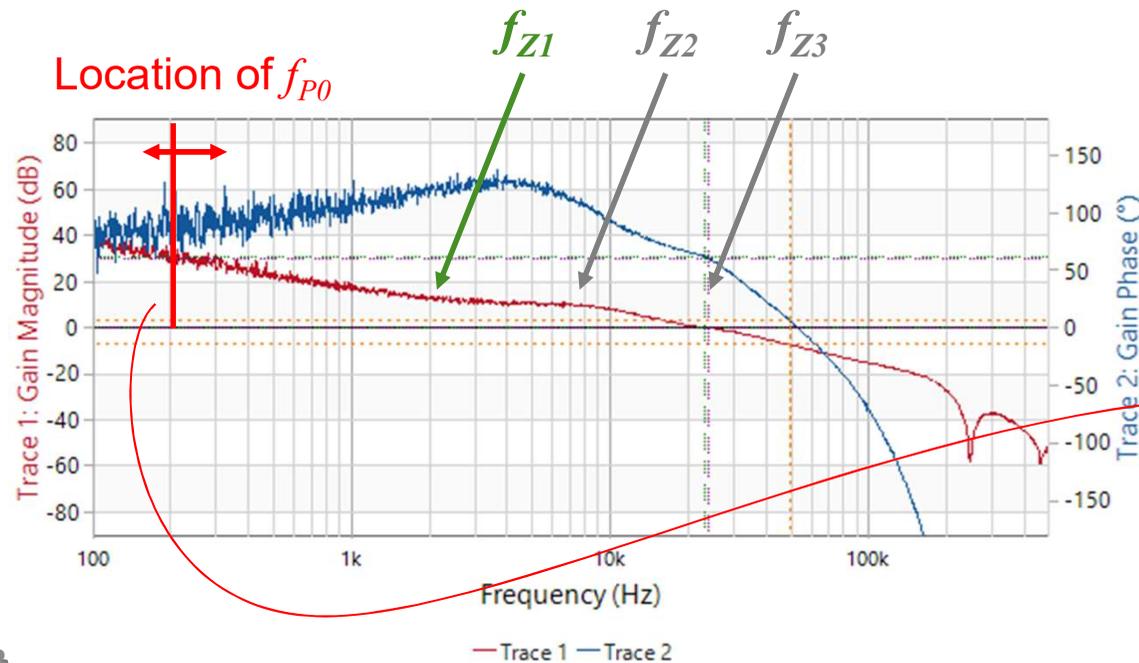
## AVMC Output Impedance Tuning

With a second order control system, the gain characteristic can be shaped in multiple ways. For output impedance tuning the location of the cross-over frequency of the pole at the origin is used to adjust the low frequency loop gain, while the location of the first zero  $f_{Z1}$  is used to set the open loop gain cross-over frequency  $f_X$  and loop phase boost region.

Unpowered

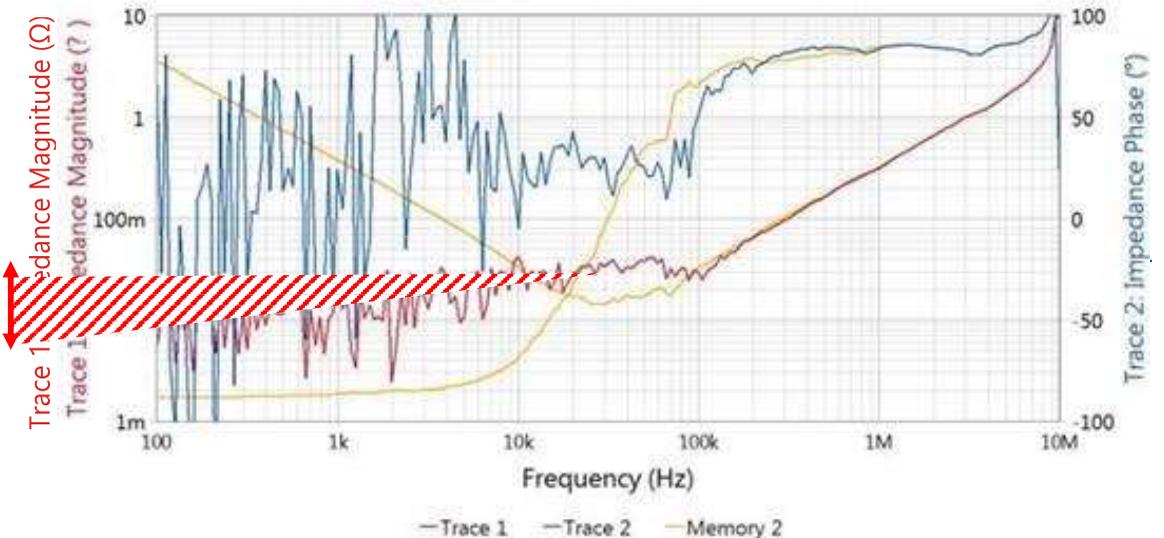


Impedance  
Matching Target

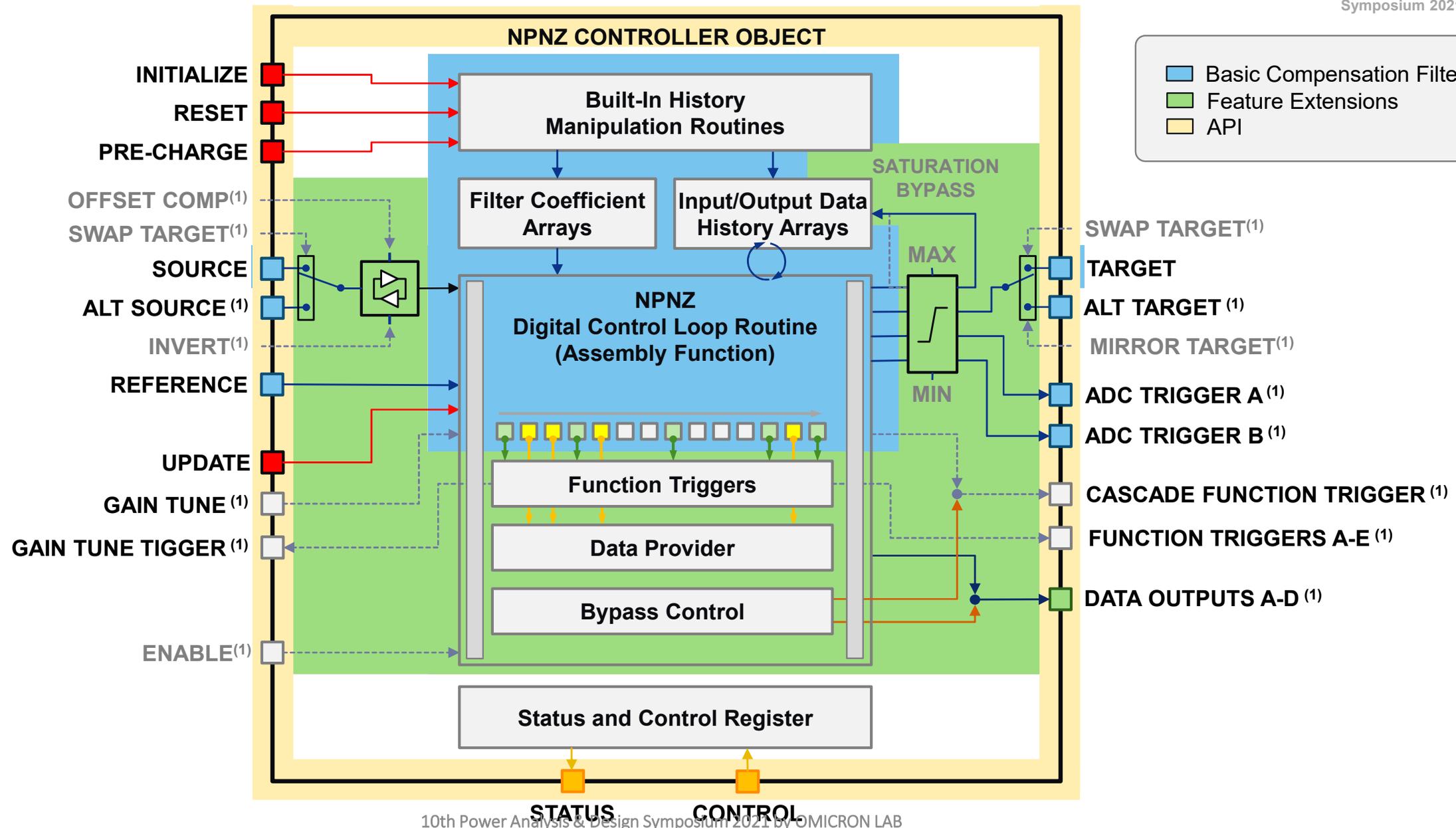


Integrator  
Gain

Powered



# Controller Block Diagram



# PowerSmart™ Digital Control Library Designer

PowerSmart™ - Digital Control Library Designer v0.9.12.672

File View Tools ?

Configuration Open Save Coefficients Bode Settings Timing Refresh Charts Update Code Export Files Help

MPLAB® X Project: \_\_\_\_\_

Frequency Domain

Controller Selection

Controller Type: 3P3Z - Basic Voltage Mode Compensator

Scaling Mode: 1 - Single Bit-Shift Scaling

Number Space: Q15

Normalize Input Gain

Total Input Data Length (Resolution): 12 Bit

Input Signal Gain: 1.000000

Feedback Offset Compensation/Bi-directional Feedback

Enable Singal Rectification Control

Compensation Settings

Sampling Frequency: 250k Hz

Cross-over Frequency of Pole At Origin: 650 Hz

Pole 1: 30k Hz Zero 1: 3.2k Hz

Pole 2: 125k Hz Zero 2: 5.9k Hz

Frequency Domain | Time Domain | Block Diagram | Source Code Output | Info

Cursor (off): Frequency: 0 Hz Magnitude: 0 dB Phase: 0° Phase Errosion 0

Legend: Gain (z) Phase (z) Gain (s) Phase (s) Pole Locations Zero Locations

Filter Coefficients

Coefficient	Float	Bsft-Scaler	Scaled Float	Fractional	FP Error	Int
<b>A-Coefficients</b>						
A1	1.230411252445470	-1	0.615205626222737	0.615234375000000	0.005%	20,160
A2	-0.129955086686779	-1	-0.064977543343389	-0.064971923828125	-0.009%	-2,129
A3	-0.100456165758697	-1	-0.050228082879348	-0.050201416015625	-0.053%	-1,645
<b>B-Coefficients</b>						
B0	0.512188742154475	-1	0.256094371077237	0.256103515625000	0.004%	
B1	-0.401881832140273	-1	-0.200940916070137	-0.200927734375000	-0.007%	
B2	-0.506722005089363	-1	-0.253361002544682	-0.253356933593750	-0.002%	
B3	0.407348569205385	-1	0.203674284602692	0.203674316406250	0.000%	

Number Analysis Settings History

Refresh Period: 123 ms Table Options

1

Configuration

2

Output/Analysis

25

10<sup>th</sup> Power Analysis & Design Symposium 2021 by OMICRON LAB

# PowerSmart™ Digital Control Library Designer

The screenshot displays the PowerSmart Digital Control Library Designer v0.9.12.672 interface. The left sidebar (labeled '1' in a blue circle) contains the 'Configuration' panel, which is highlighted with a red box and labeled 'Configuration'. The main window (labeled '2' in a blue circle) shows the 'Time Domain' view, which is highlighted with a red box and labeled 'Time Domain'. Below the graph is an 'Execution Timing' table.

**Configuration Panel (1):**

- Name Prefix: c3p3z
- Context Management:
  - Save/Restore Shadow Registers
  - Save/Restore MAC Working Registers
  - Save/Restore Accumulators
    - Save/Restore Accumulator A
    - Save/Restore Accumulator B
  - Save/Restore DSP Core Configuration
  - Save/Restore Core Status Register
- Used Resources: WREG 0,1,2,3,4,6,8,10/ACC AB
- Basic Feature Extensions:
  - Store/Reload Result Accumulator
  - Add DSP Core Configuration
  - Add Enable/Disable Feature
  - Always read from source when disabled
  - Add Error Normalization
  - Add Automatic Placement of Primary ADC Trigger A
  - Add Automatic Placement of Secondary ADC Trigger B
- Estimated Data Interface
- Data Provider Sources
- Anti-Windup
- Output to Positive Numbers
- Number Range: -32768...32767
- Maximum
- Generate Upper Saturation Status Flag Bit
- Clamp Control Output Minimum
- Force Values below Minimum Threshold to Zero
- Generate Lower Saturation Status Flag Bit

**Time Domain View (2):**

Cursor (off): Absolute: 0 nsec Relative to ADC S&H Event: 0 nsec Relative To Falling Edge: 0 nsec Trigger at: 50% On-Time

Signal Level [L]

Time [nsec]

CPU LOAD: 24.3%

Legend: Main PWM Pulse (blue), ADC Activity (orange), Control Loop Execution (red)

**Execution Timing Table:**

Control Loop Call Event:	0 - PWM Interrupt Trigger	
CPU Clock:	100 MHz	Total Number of Instructions: 84
PWM Frequency:	250 kHz	Normalized Runtime Instruction Cycles: 80
Duty Cycle:	30 %	Instruction Cycles until DATA READ: 30
ADC Latency:	310 nsec	Instruction Cycles until DATA WRITEBACK: 54
Control Interrupt Latency:	170 nsec	Execution Period (Loop Trigger to Exit Control Routine): 0.970 μsec
User Trigger Delay:	120 nsec	Data Capture Delay (ADC Trigger to DATA READ): 0.470 μsec
		Response Delay (ADC Trigger to DATA WRITEBACK): 0.710 μsec
		Relative CPU Load: 24.3 %

# PowerSmart™ Digital Control Library Designer

**Block Domain**

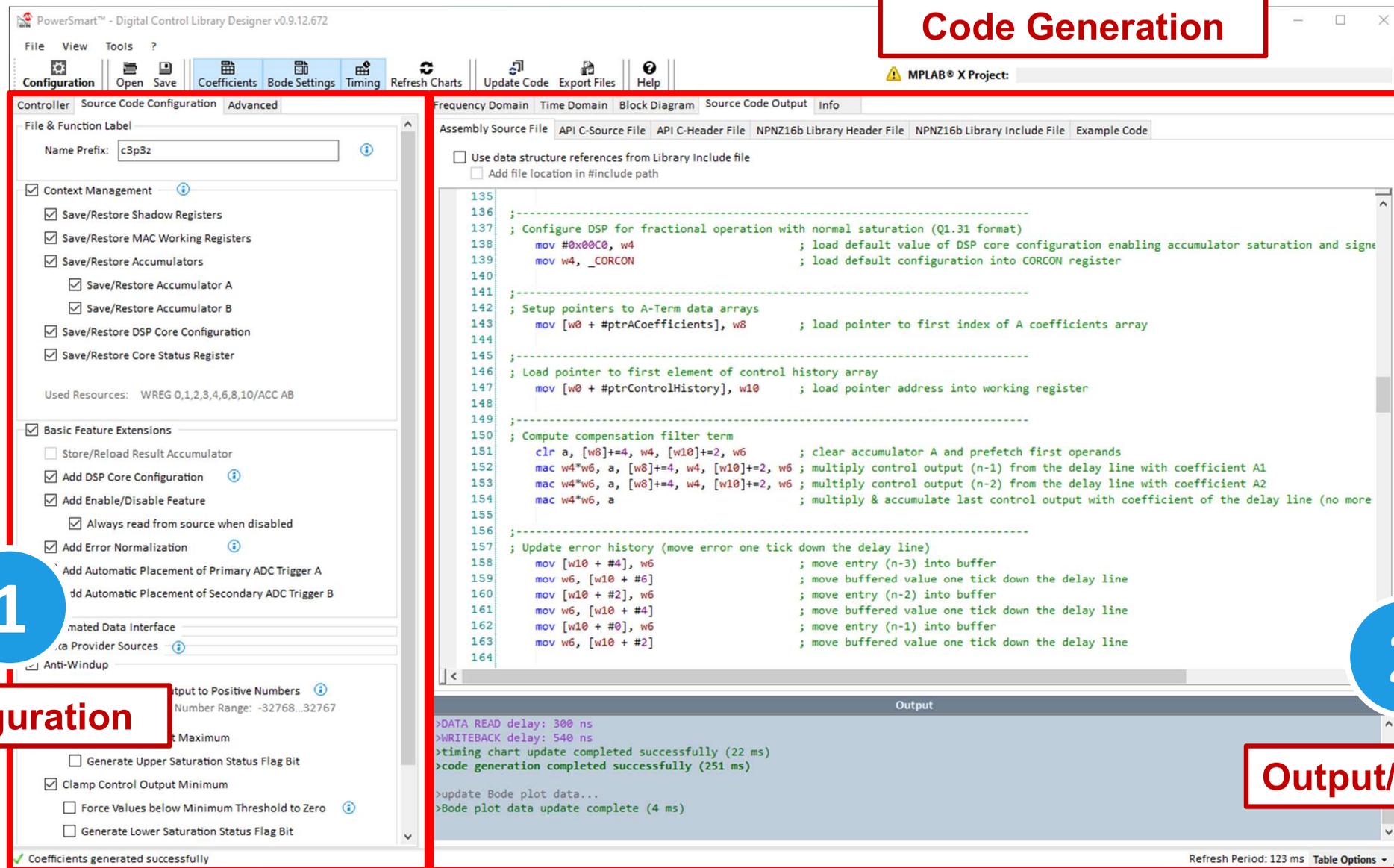
**1**

**Configuration**

**2**

**Output/Analysis**

# PowerSmart™ Digital Control Library Designer



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**Code Generation**

```
135  
136 ;-----  
137 ; Configure DSP for fractional operation with normal saturation (Q1.31 format)  
138 mov #0x00C0, w4 ; load default value of DSP core configuration enabling accumulator saturation and sign  
139 mov w4, _CORCON ; load default configuration into CORCON register  
140  
141 ;-----  
142 ; Setup pointers to A-Term data arrays  
143 mov [w0 + #ptrACoefficients], w8 ; load pointer to first index of A coefficients array  
144  
145 ;-----  
146 ; Load pointer to first element of control history array  
147 mov [w0 + #ptrControlHistory], w10 ; load pointer address into working register  
148  
149 ;-----  
150 ; Compute compensation filter term  
151 clr a, [w8]+4, w4, [w10]+2, w6 ; clear accumulator A and prefetch first operands  
152 mac w4*w6, a, [w8]+4, w4, [w10]+2, w6 ; multiply control output (n-1) from the delay line with coefficient A1  
153 mac w4*w6, a, [w8]+4, w4, [w10]+2, w6 ; multiply control output (n-2) from the delay line with coefficient A2  
154 mac w4*w6, a ; multiply & accumulate last control output with coefficient of the delay line (no more  
155  
156 ;-----  
157 ; Update error history (move error one tick down the delay line)  
158 mov [w10 + #4], w6 ; move entry (n-3) into buffer  
159 mov w6, [w10 + #6] ; move buffered value one tick down the delay line  
160 mov [w10 + #2], w6 ; move entry (n-2) into buffer  
161 mov w6, [w10 + #4] ; move buffered value one tick down the delay line  
162 mov [w10 + #0], w6 ; move entry (n-1) into buffer  
163 mov w6, [w10 + #2] ; move buffered value one tick down the delay line  
164
```

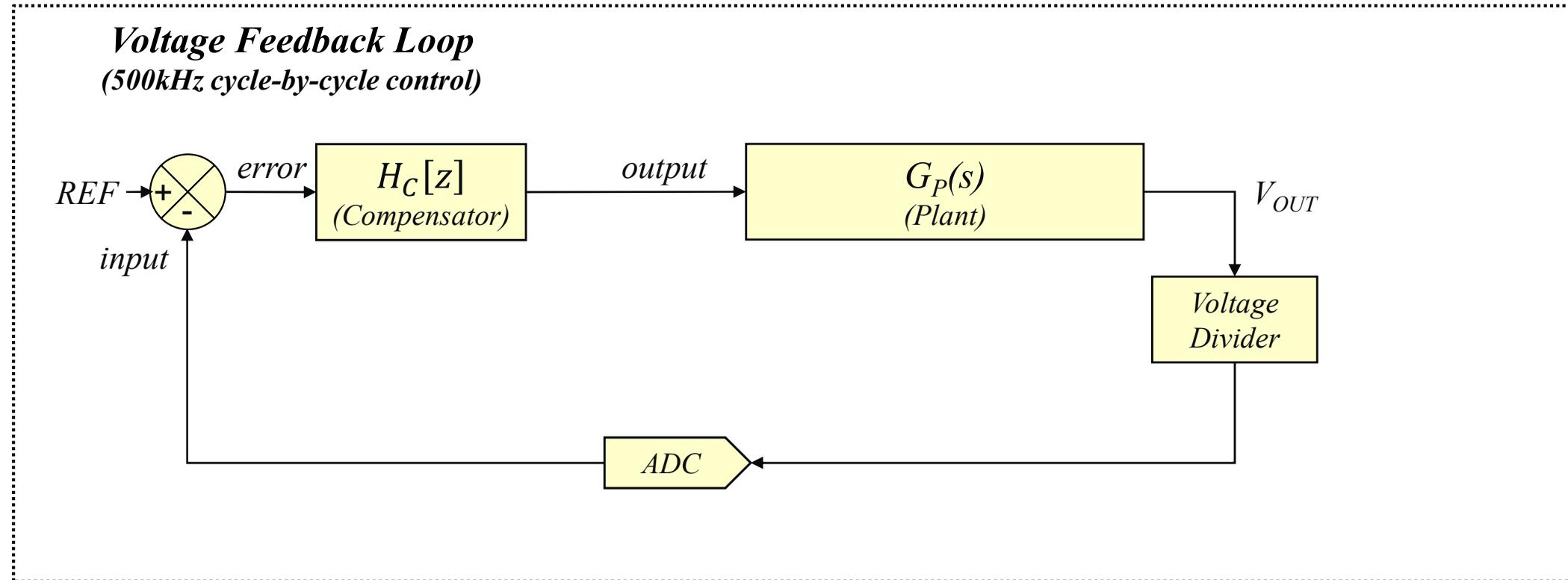
**Configuration**

**Output/Analysis**

```
>DATA READ delay: 300 ns  
>WRITEBACK delay: 540 ns  
>timing chart update completed successfully (22 ms)  
>code generation completed successfully (251 ms)  
  
>update Bode plot data...  
>Bode plot data update complete (4 ms)
```

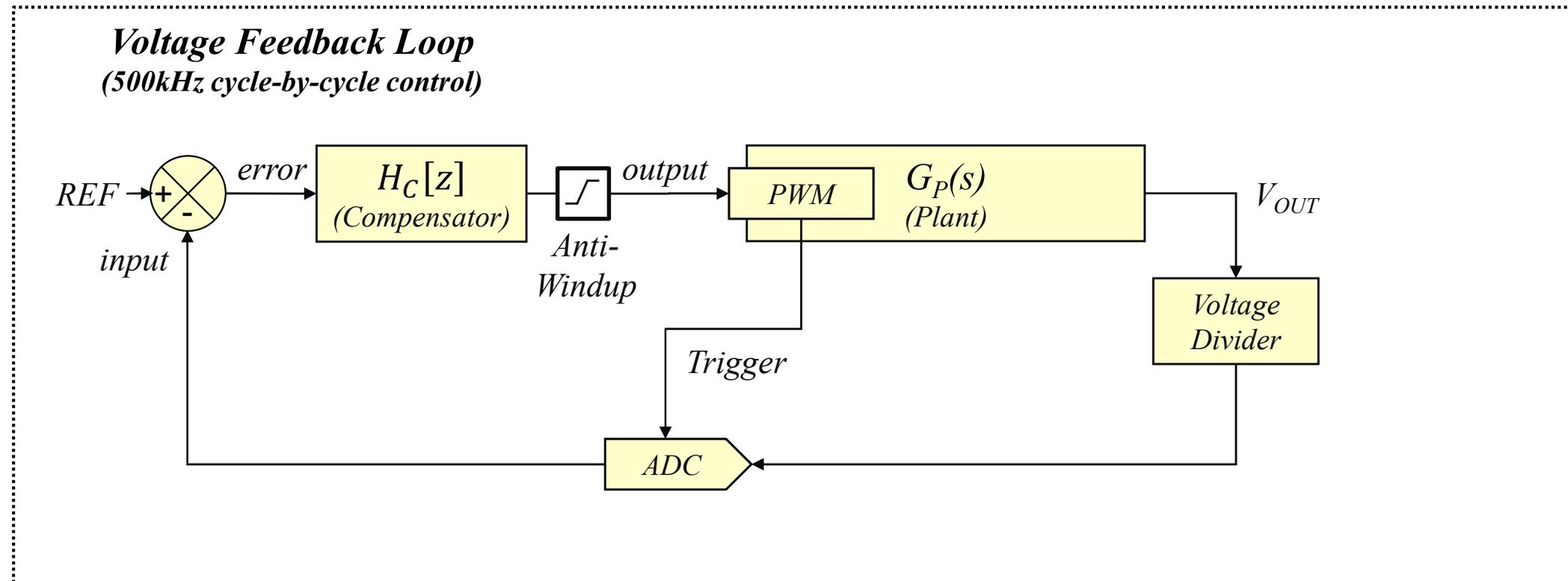
# Building the Control System

## Basic Voltage Mode Control Implementation



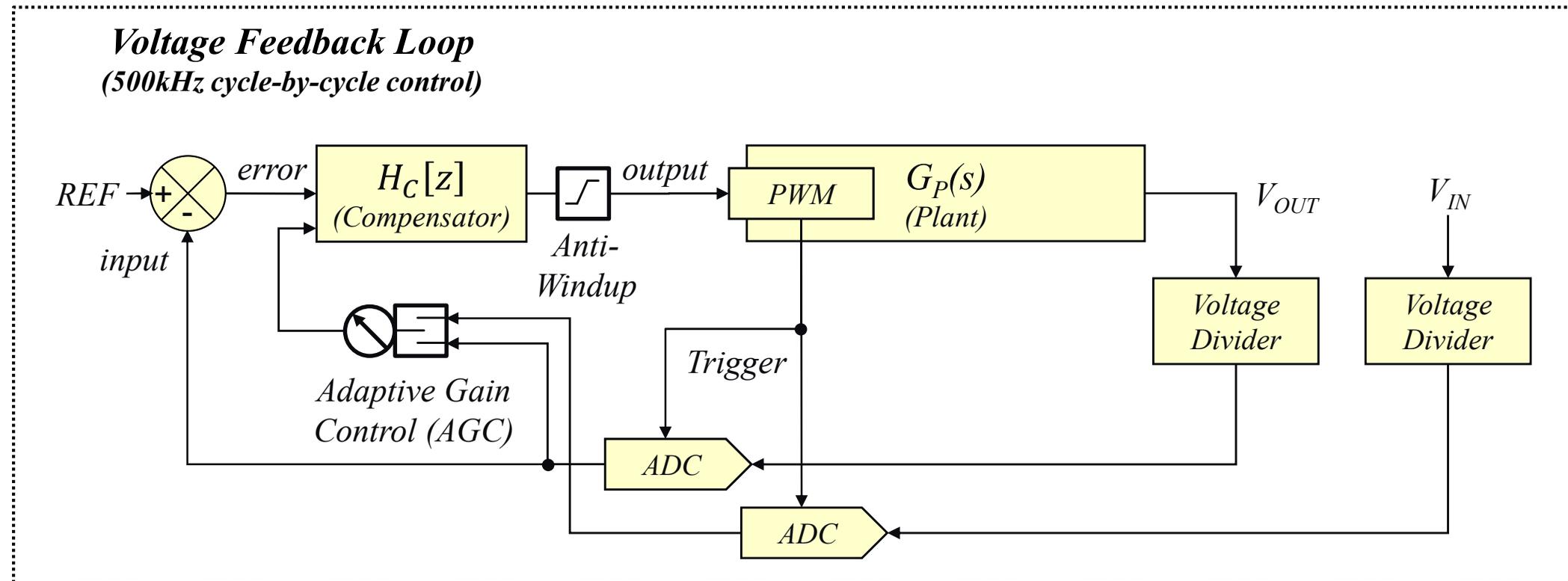
# Building the Control System

## Peripheral Interconnections



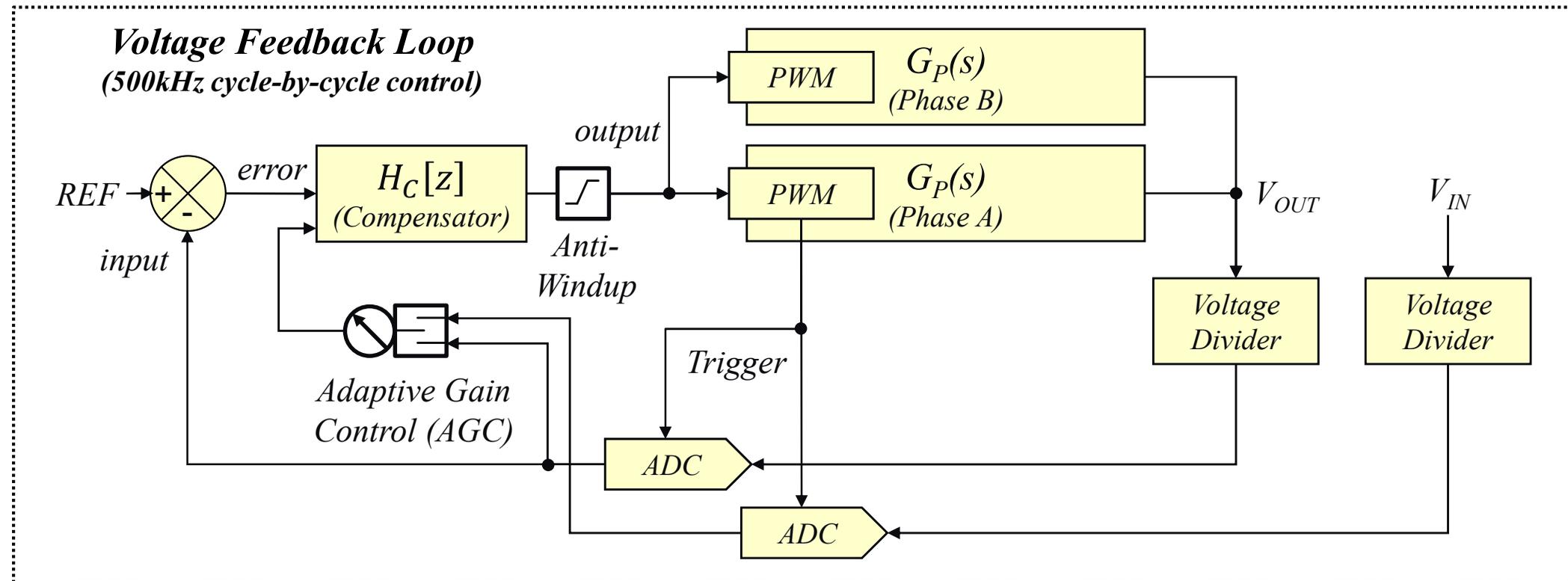
# Building the Control System

## Adaptive Gain Control Implementation



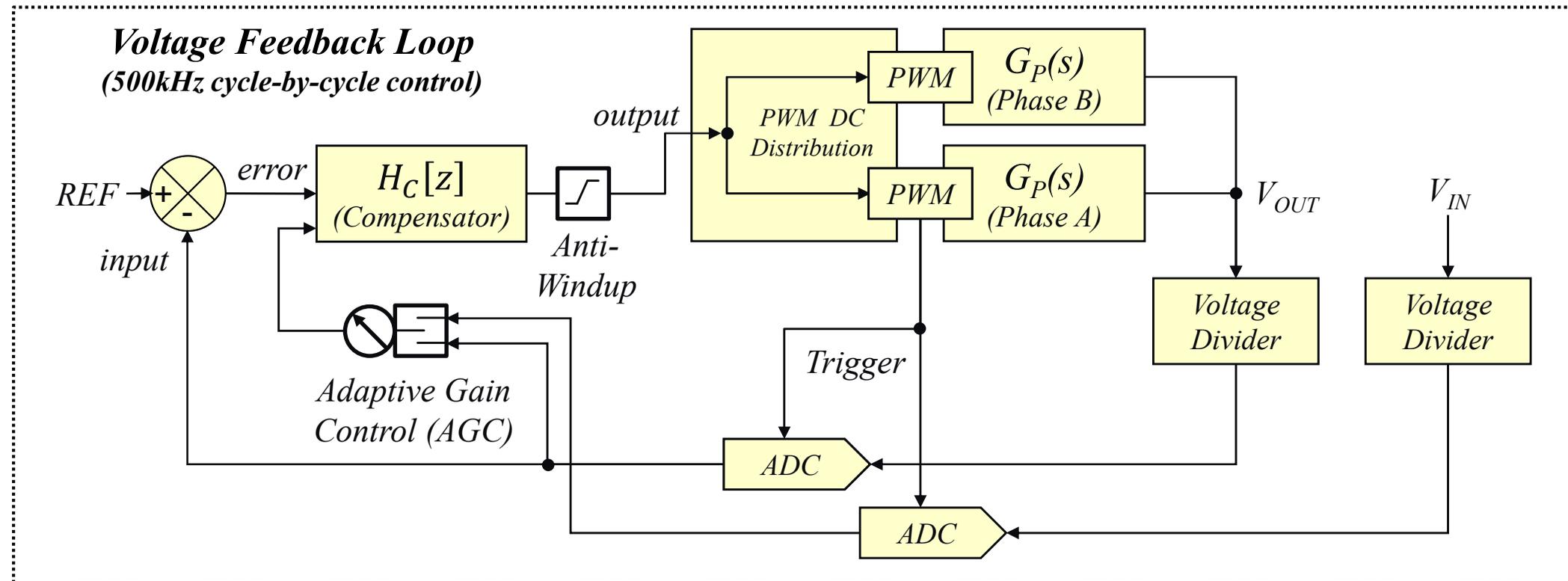
# Building the Control System

## PWM Mirroring with Phase Shift



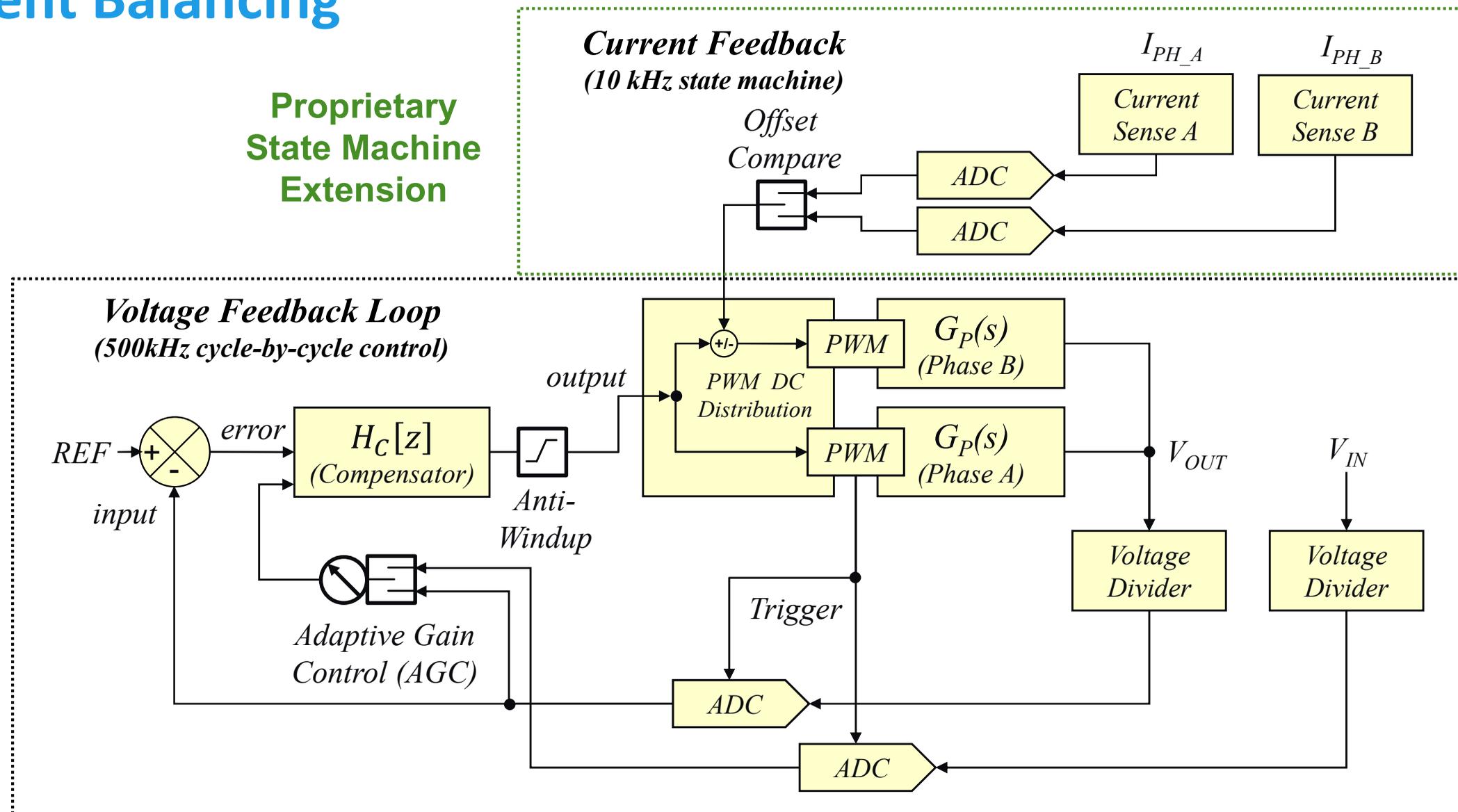
# Building the Control System

## PWM Duty Cycle Distribution



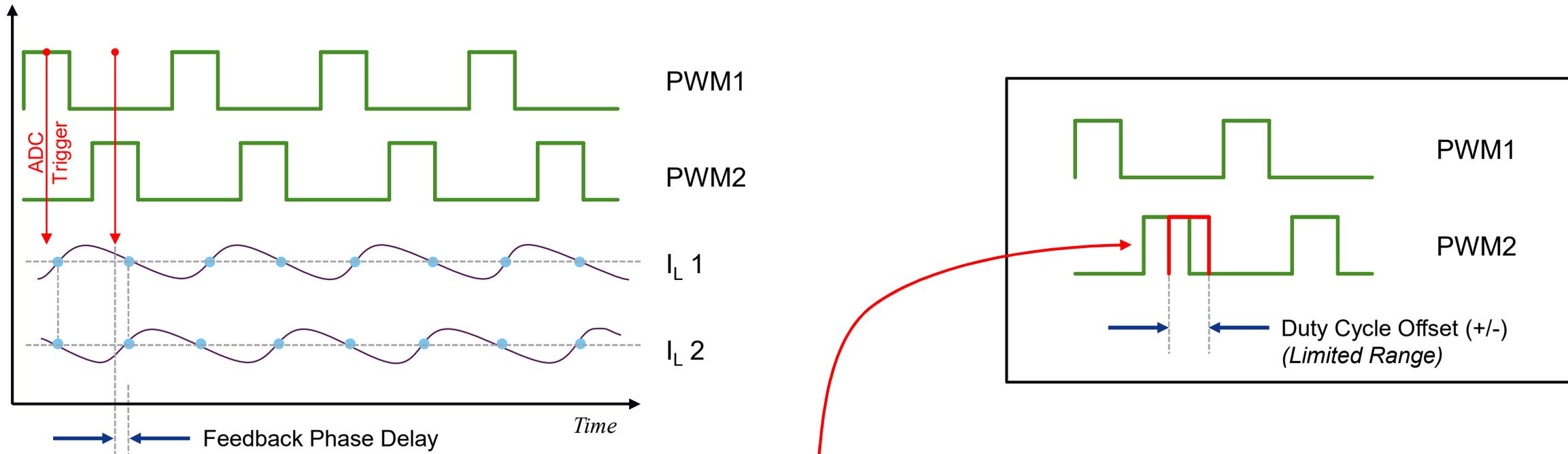
# Building the Control System

## Current Balancing



# Current Balancing Implementation

## Simple Bit Tracker Implementation



$$\Delta I_L = I_{L1} - I_{L2}$$

Sign-Bit of result is OR'ed with 0x0001 and added to duty cycle of PWM2 every 100 us (=10 kHz) resulting in adjustment in 250 ps increments/decrements

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  - EPC9143: Unidirectional Power Module
  - EPC9151: Bi-Directional Power Module
- High-Speed Multiphase Controller Design
  - Type IV Adaptive Voltage Mode Control
  - PWM Steering and High-Speed Current Balancing
- **Summary**

# Summary

- **Digital control loops allows**
  - Using real and complex poles and zeros to overcome complex frequency domain limitations
  - Independent pole and zero locations allow runtime tuning
  - Runtime tuning allows adaptation of loop gain to operating conditions
  - Higher order control systems allow independent tuning of output impedance and bandwidth
- **Impedance and Bandwidth Tuning**
  - simplifies system integration
  - Improves overall system stability
  - Minimizes cost and size



# Thank You!

May the Power be with you!

**POWER**  
YOUR IDEAS!





# Appendix

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# Digital Power

- **Getting Started in Digital Power**

- Intelligent Power Design Center:

<https://www.microchip.com/power>

- **How-2 Starter Kits**

- Digital Power Starter Kit 3 (Part-No. DM330017-3):

<https://www.microchip.com/dm330017-3>

- **Training:**

- Microchip University (Virtual Training Platform):

<https://secure.microchip.com/mu>

## Please note:

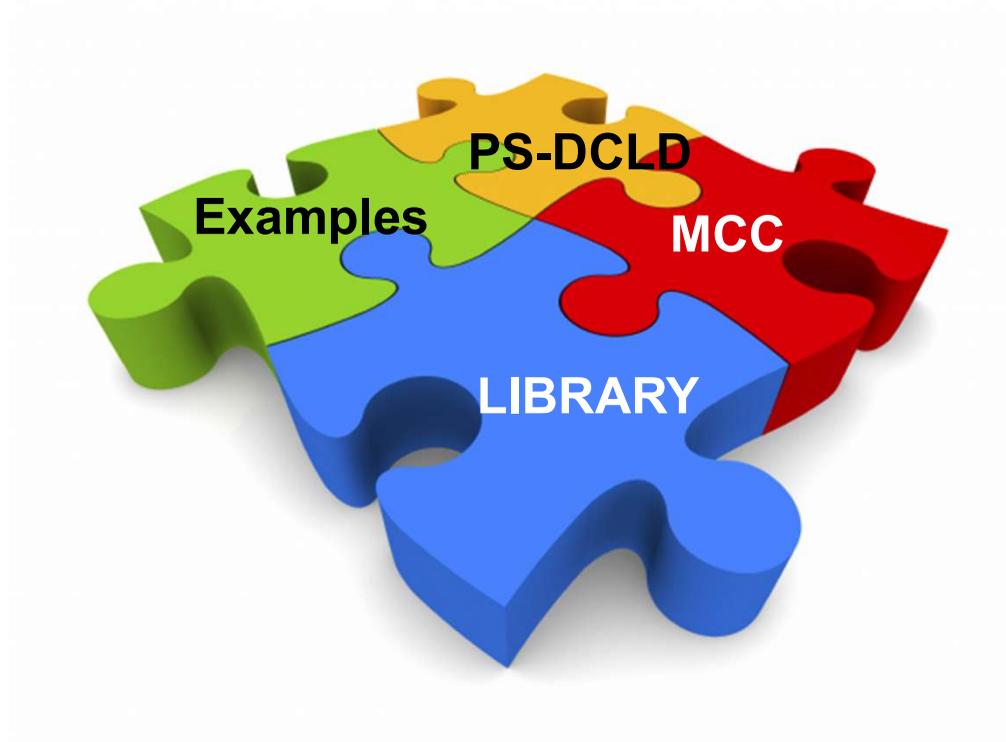
All Face-2-Face workshops have been suspended in early 2020, including the well-known MASTERS conferences usually conducted in 9 nations around the globe. For the time being all available trainings have been moved to our new virtual training platform ***Microchip University***.



# Digital Power Design Resources



- Find hundreds of code examples and design tools on <https://discover.microchip.com>



The screenshot shows the MPLAB DISCOVER website interface. The browser address bar displays <https://mplab-discover.microchip.com>. The page features a search bar and a navigation menu on the left under 'Offerings' and 'IDE Examples'. The main content area displays a project configuration for 'dsPIC33CK/CH-MP PWM Configuration: Complementary PWM Output'. The project details include 'EPC9143 300W 16th Brick Non-Isolated Step Down Converter Advanced Voltage Mode Control Firmware' and 'dsPIC33C High-Resolution PWM Configuration I'. Below the text, there are two images of the EPC9143 PCB: a 'Top View' showing the EPCOS A0242 2.4UH 1932 inductors and a 'Bottom View' showing the PCB components and labels like '2014-003' and 'PCB#: B5194'. The Microchip logo is visible in the top right corner of the page.

# Product Websites



- **dsPIC33CK32MP102: Digital Signal Controller for SMPS Applications**  
<https://www.microchip.com/dsPIC33CK32MP102>
- **MCP6C02: 65 V Shunt Current Sense Amplifier**  
<https://www.microchip.com/mcp6c02>
- **EPC9143: 300 W 48 V Unidirectional 16<sup>th</sup> Brick Reference Design**  
<https://www.microchip.com/EPC9143>
- **EPC9151: 300 W 48 V Bidirectional 16<sup>th</sup> Brick Reference Design**  
<https://www.microchip.com/EPC9151>

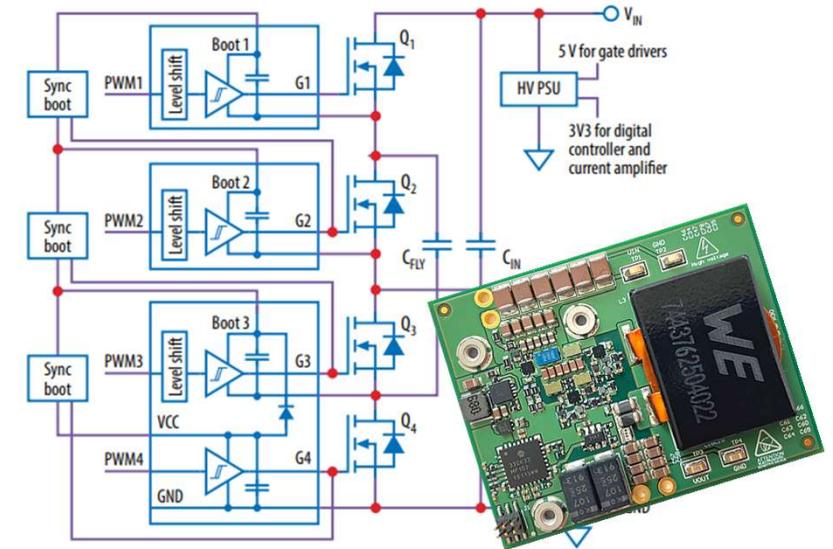
# Related Product Websites



- **EPC9148: 250 W 48 V Three-level Synchronous Buck Converter**

Ultra-Thin, multi-level converter for high performance computing systems

<https://www.microchip.com/EPC9148>



- **EPC9153: 250 W 48 V High Efficiency, Thin Power Module**

Thin Power Module for high performance computing systems with 200% over-power capability

<https://www.microchip.com/EPC9153>

