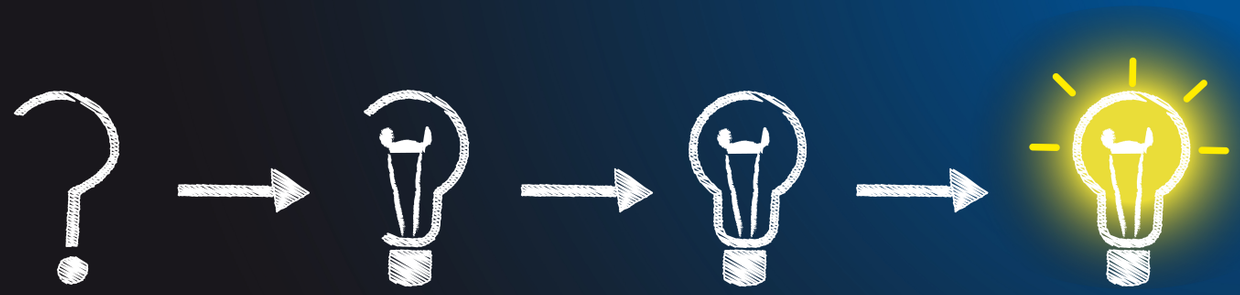

10th Power Analysis & Design Symposium

March 10th, 2021 - Worldwide (Virtual)

Seamless Software Adaptation of High Performance Power Modules in Power Distribution Networks

by Andreas Reiter - Microchip Technology

OMICRON LAB

Seamless Software Adaptation of

High- Performance Power Modules in Power Distribution Networks

MICROCHIP

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

SMART | CONNECTED | SECURE

Presented by Andreas Reiter – 10th March 2021

10th Power Analysis & Design Symposium 2021

Agenda

- **48V Rack Power Distribution Networks and Conversion Points**
- **300W 48V 1/16th Brick DC/DC Converter Power Module**
  - EPC9143: Unidirectional Power Module
  - EPC9151: Bi-Directional Power Module
- **High-Speed Multiphase Controller Design**
  - Type IV Adaptive Voltage Mode Control
  - PWM Steering and High-Speed Current Balancing
- **Summary**

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MICROCHIP @ OMICRON LAB
10th Power Analysis & Design Symposium 2021

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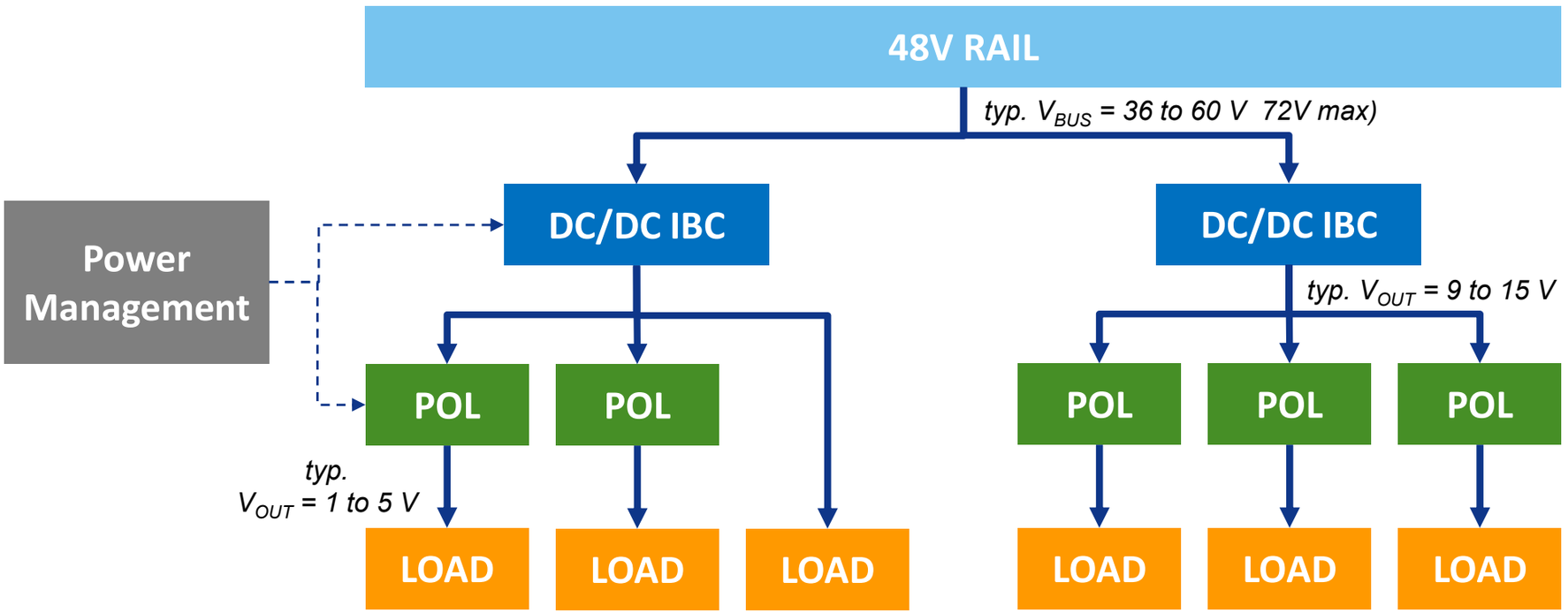
Intermediary Bus Converters (IBC)



Market Driver for High Power Density IBCs

- **5G Systems require up to three times more power than their 4G/LTE counterpart**
  - Majority of power consumption by 64T64R MIMO array vs. 4T4R of 4G/LTE
  - Higher Transmitter and Receiver Bandwidth requires faster data processing with more/faster CPUs/FPGAs
- **The cost of a 5G Base Station is ~4x of 4G/LTE**
  - Increased cost pressure

Agenda

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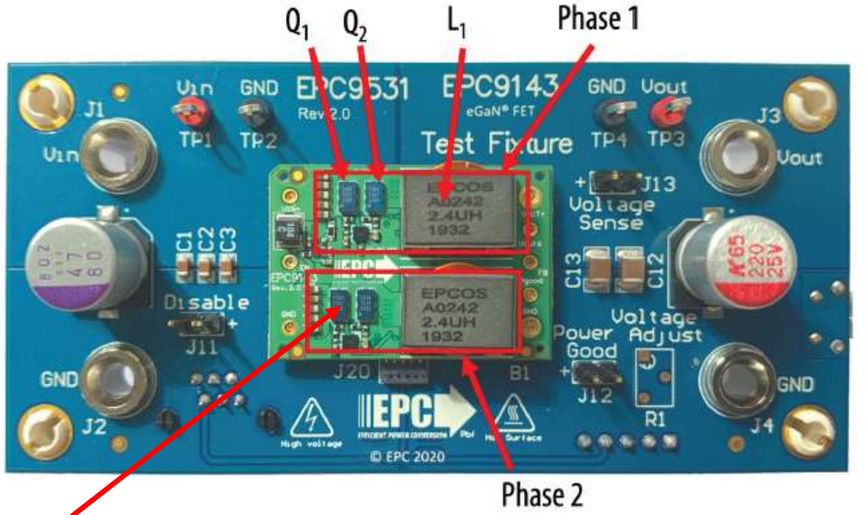
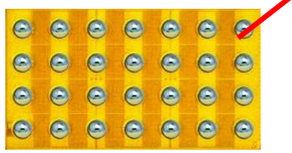
EPC's 300W 1/16th Brick IBC Converters

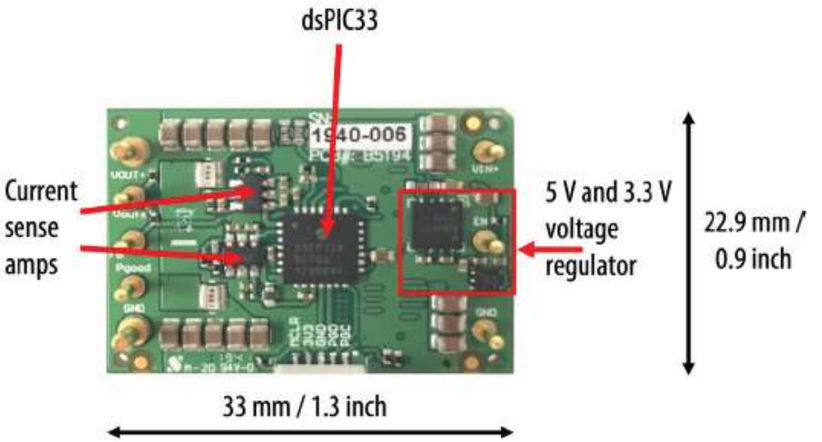
Reference Design Features

- Microchip dsPIC33CK digital signal controller
- EPC2053 eGaN® FETs with 3.2 mΩ RDS(on)
- Two-phase synchronous buck topology
- 48 V in -> 5 to 15 V out
- 25 A maximum I out
- Power density: 650 to 748 W/in^3
- Output power: 300 W
- Peak efficiency: 94.8 – 96.3 %
- Size: (33 x 22.9 x 9) mm
  (1.3 x 0.9 x 0.35)"



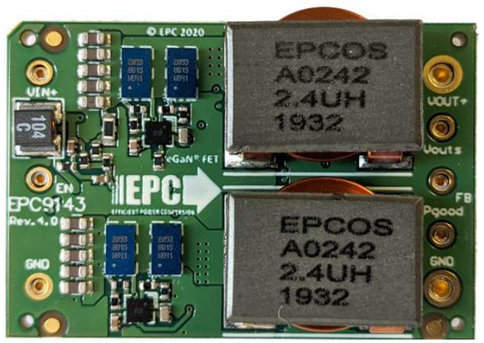


EPC2053
eGaN® FET
100 V, 3.2 mΩ
3.5 mm x 2.0 mm



EPC9143 Reference Design vs. Off-The-Shelf Silicon MOSET Module

- EPC9143
- V_{IN}: 10…61 V DC (1)
- V_{OUT}: 3.3 … 15 V DC
- I_{OUT}: 25 A max (23 A @ 15 V DC)
  @ 800 LFM airflow
- Power Density: 748 W/in³ (2)



(1) : 73 V max, not operational
(2) : max. power density @ V_{OUT}=15 V, 23 A
650 W/in³ @ V_{OUT}=12 V, 25 A

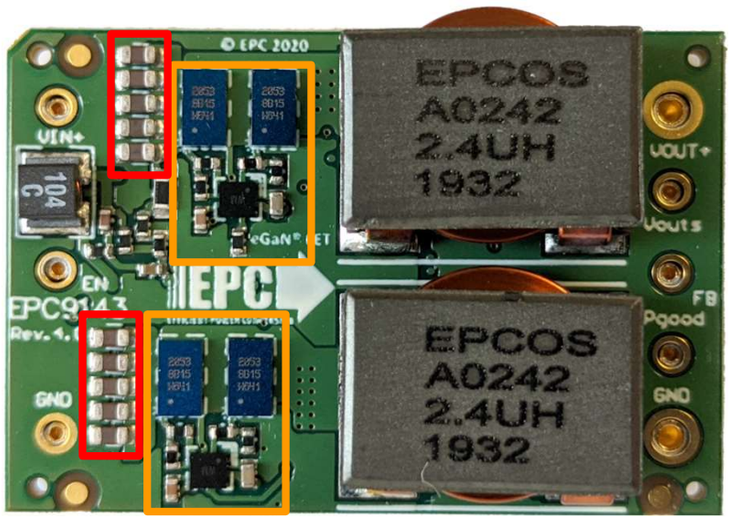
- Vendor T Module
- V_{IN}: 9…53 V DC
- V_{OUT}: 3.3 … 15 V DC
- I_{OUT}: 20 A max (3)
  @ 800 LFM airflow
- Power Density: 483 W/in³

(3) : data sheet value, but power density limited to max. 480 W/in³

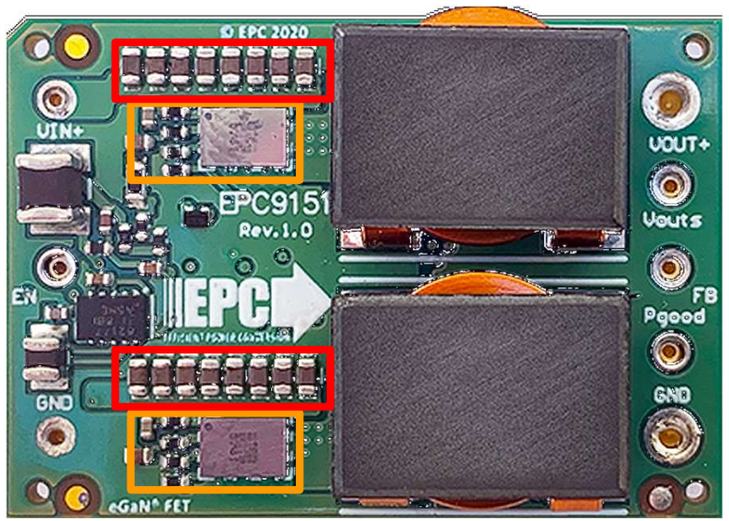
EPC's 300W 1/16th Brick IBC Converters

Two modules tailored for different applications

- **EPC9143 Unidirectional 16th Brick**
  - Discrete half-bridge design
  - uP1966A gate driver +
    2x EPC2053 100V eGaN FET
  - Peak Efficiency > 96%
  - Target Applications: Telecom IBC



- **EPC9151 Bi-Directional 16th Brick**
  - Integrated half-bridge design
  - EPC2152 ePower™ stage
  - Peak Efficiency > 95%
  - Target Applications:
    Automotive, Aerospace



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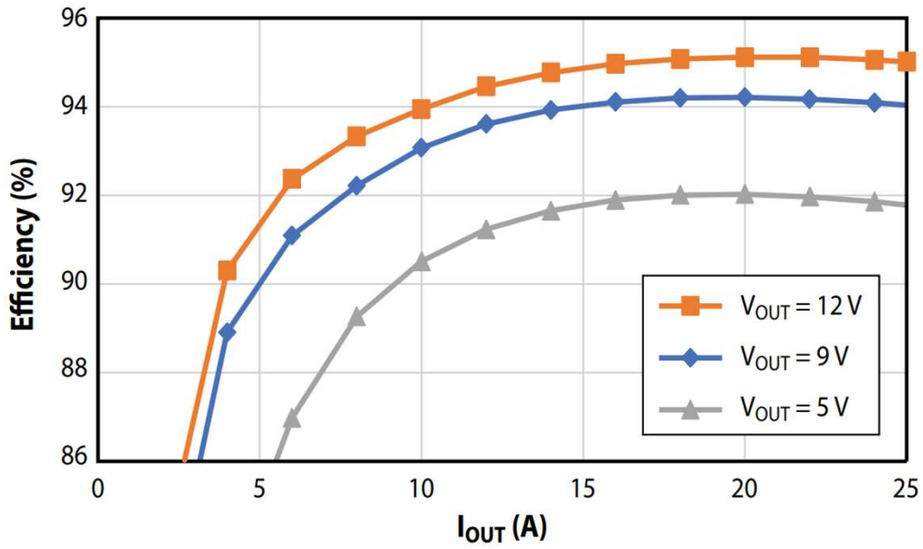

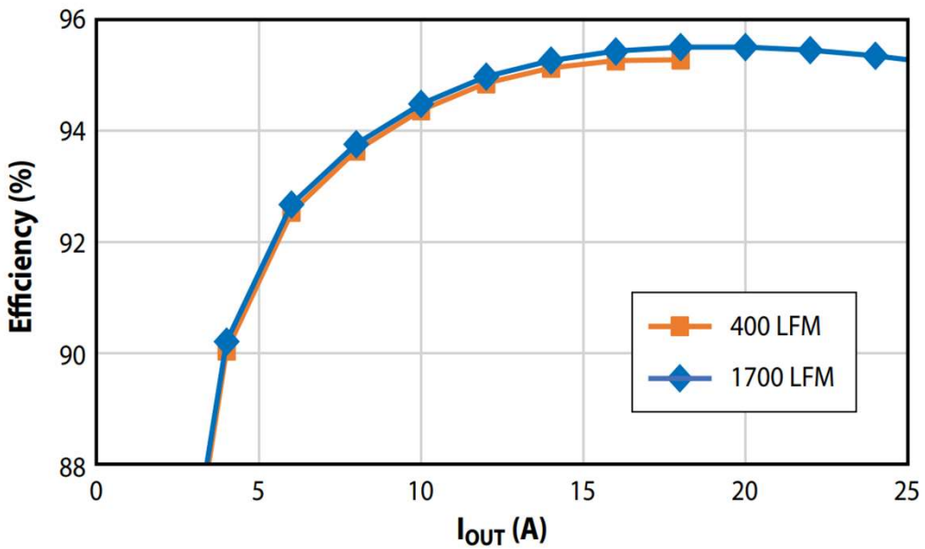

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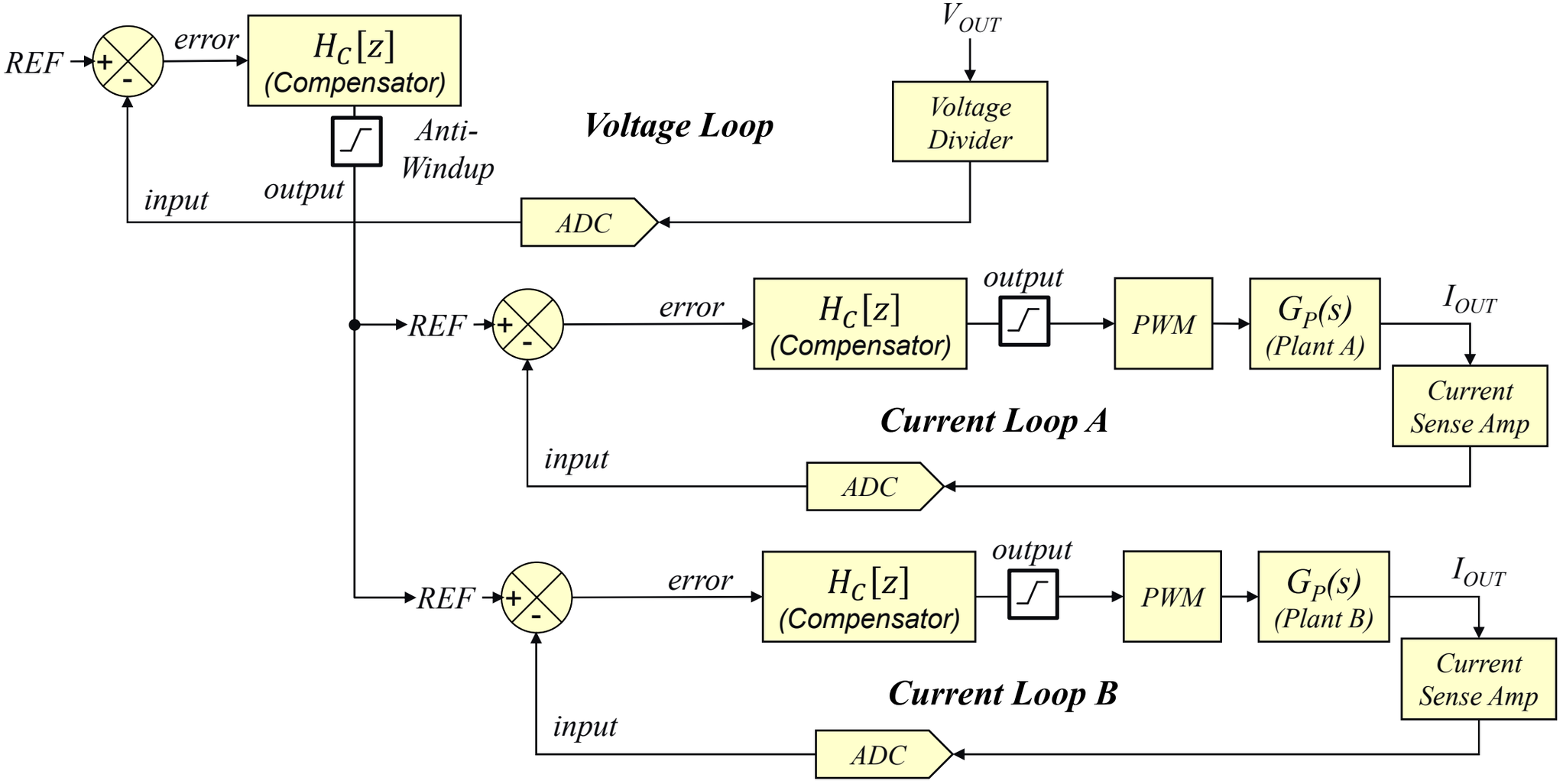
Average Current Mode Control

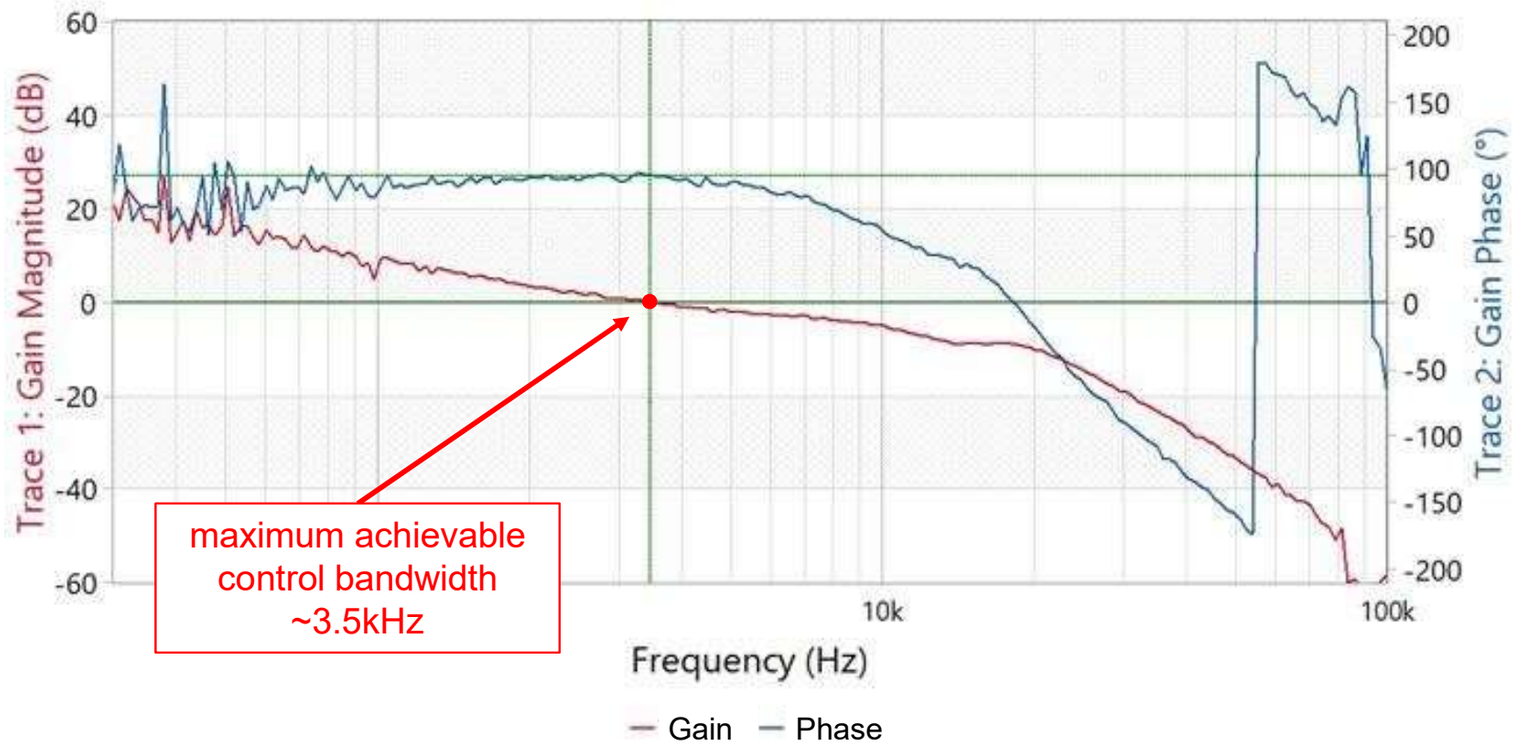
Conventional Multiphase Converter Control Scheme



Average Current Mode Control

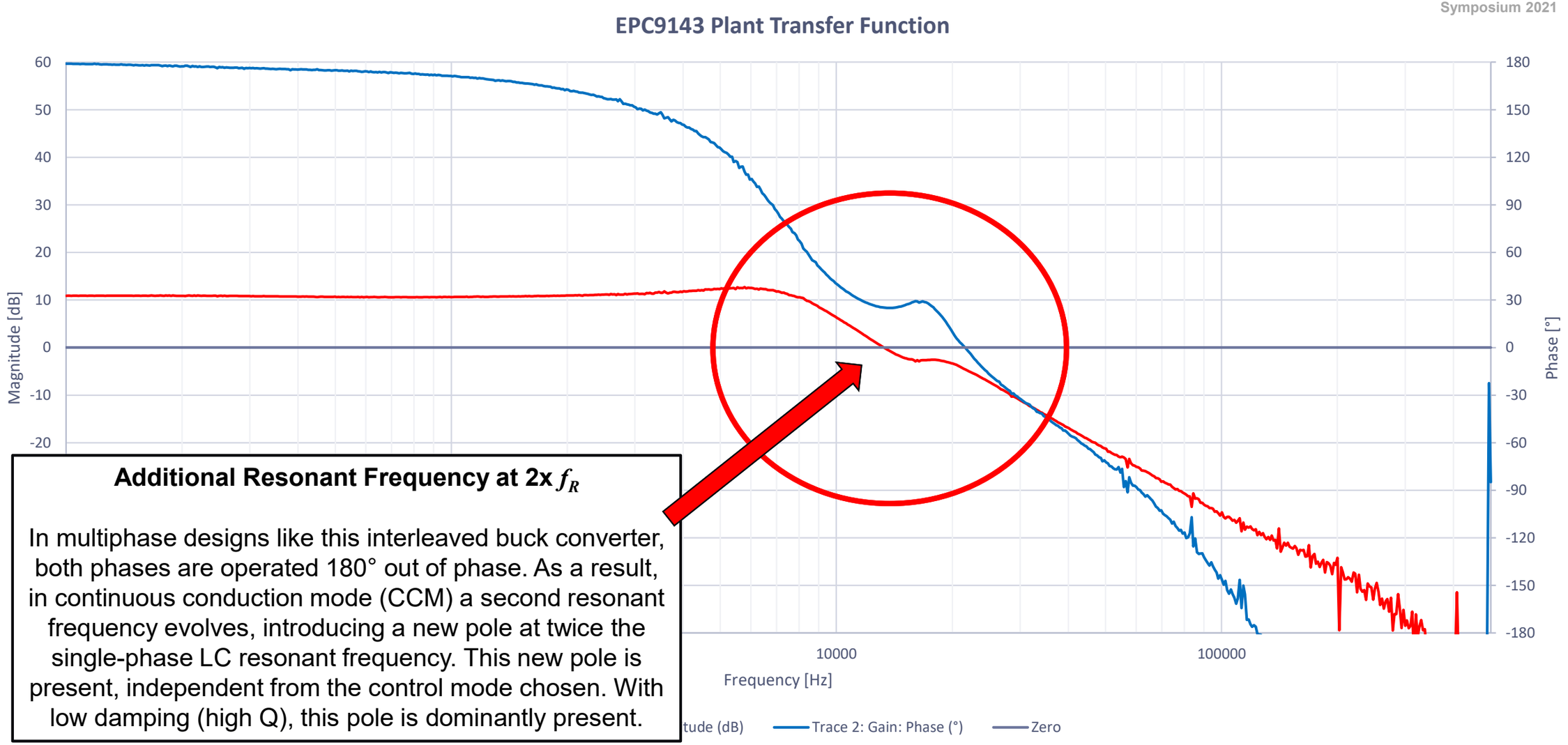
Conventional Multiphase Converter Control Scheme

In average current mode control (ACMC), the total achievable bandwidth is limited by the maximum allowed perturbation frequency of the reference provided to the two, independent inner current loops in relation to their maximum cross-over frequency (here ~10kHz). Outer voltage loop and inner current loop are executed at the same frequency. The ratio of their respective cross-over frequencies f_X is adjusted to limit the maximum perturbation frequency. As a result, the second resonant pole occurs in a negative gain region, where it is uncritical.



f_{SW} = 500 kHz
f_X = 3.5 kHz
Φ_{PM} > 90°
GM < -12 dB

High Efficiency Multiphase Plant



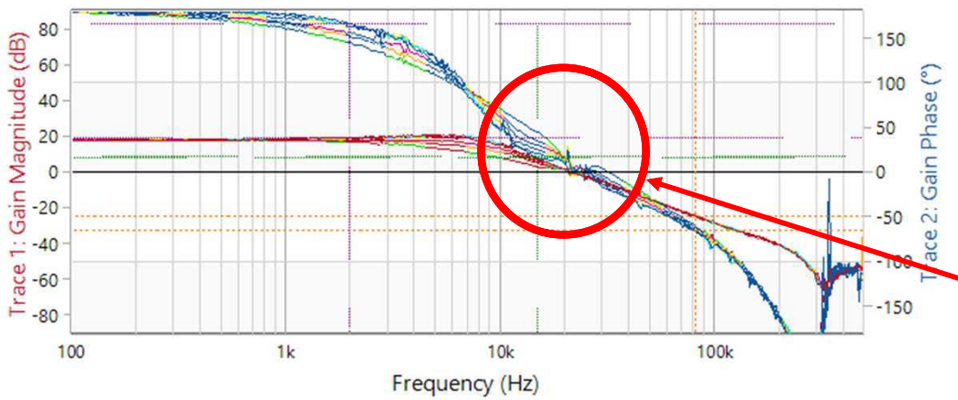
Additional Resonant Frequency at 2x f_R

In multiphase designs like this interleaved buck converter, both phases are operated 180° out of phase. As a result, in continuous conduction mode (CCM) a second resonant frequency evolves, introducing a new pole at twice the single-phase LC resonant frequency. This new pole is present, independent from the control mode chosen. With low damping (high Q), this pole is dominantly present.

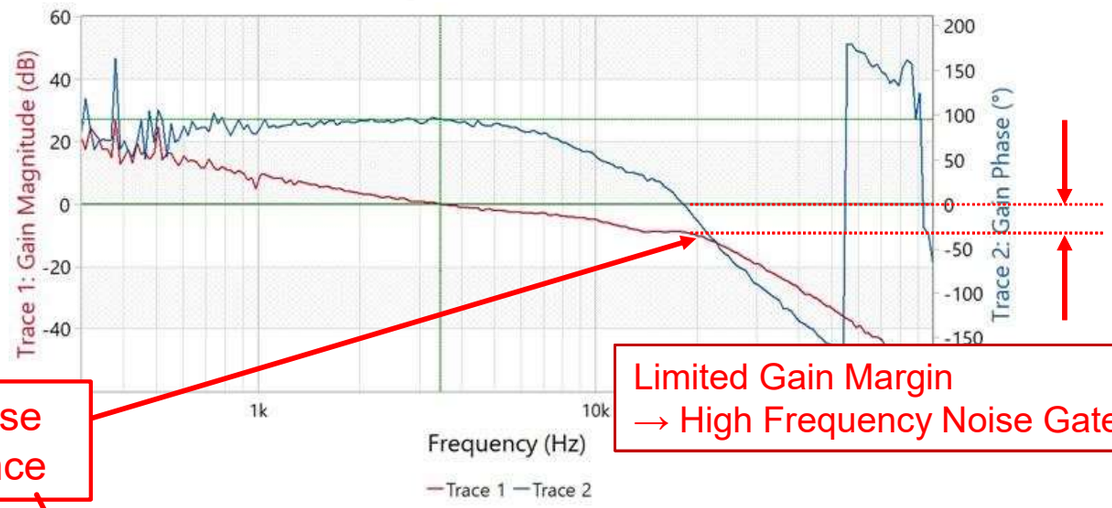
EPC's 300W 1/16th Brick IBC Converters

Why Type IV Control in AVMC?

Plant Transfer Functions



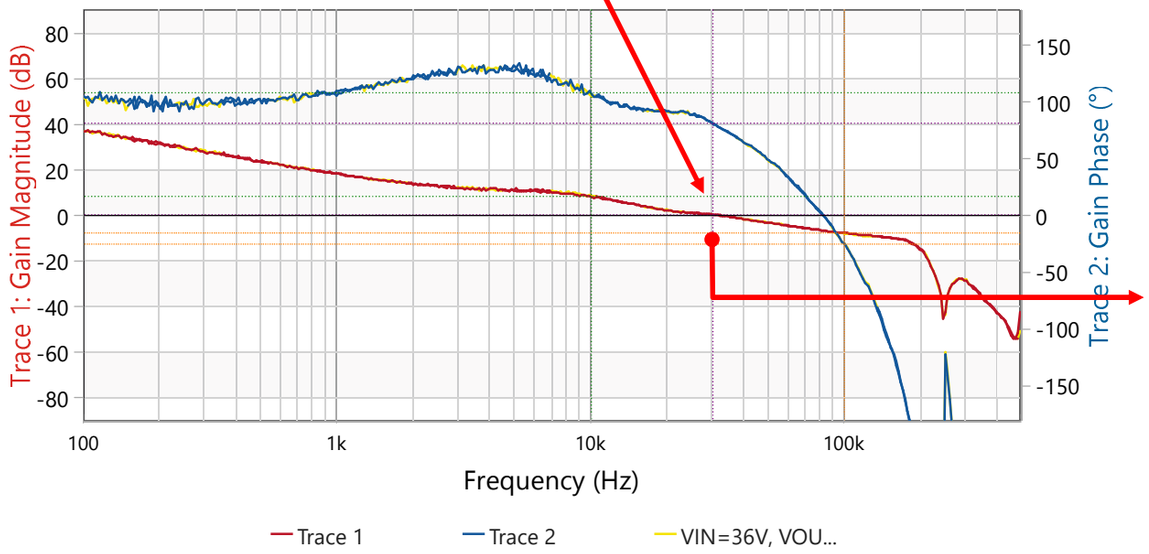
Open Loop TF Average Current Mode Control (ACMC)



Multiphase Resonance

Limited Gain Margin
→ High Frequency Noise Gate

Open Loop TF Adaptive Voltage Mode Control (AVMC)



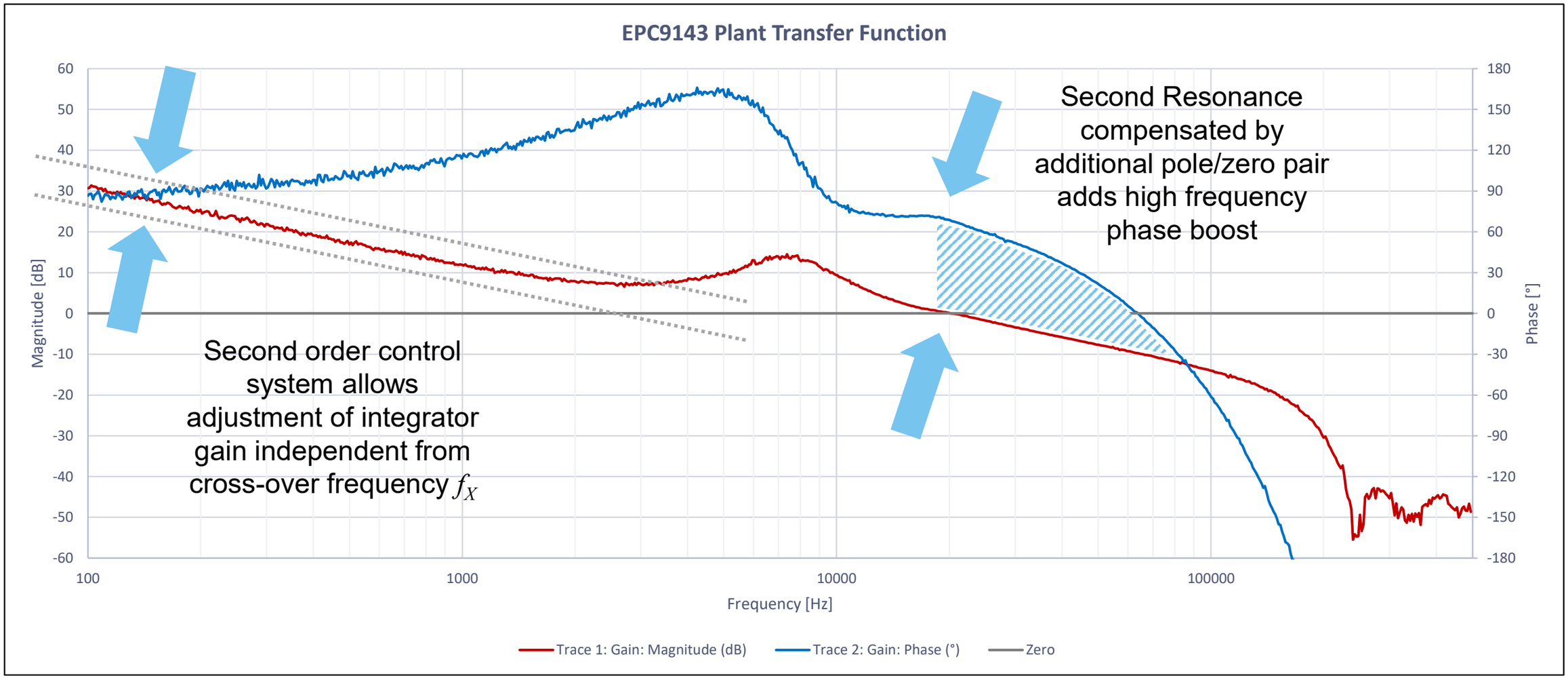
Higher order systems allow placements of additional poles and zeros. In digital loops, these can either be real or complex conjugate poles and zeros.

One additional pole/zero pair is used to damp the second resonant bump.

Pushing cross-over frequency beyond 20 kHz results in flat gain region near 0 dB (conditional stability)

Type IV Adaptive Voltage Mode Control

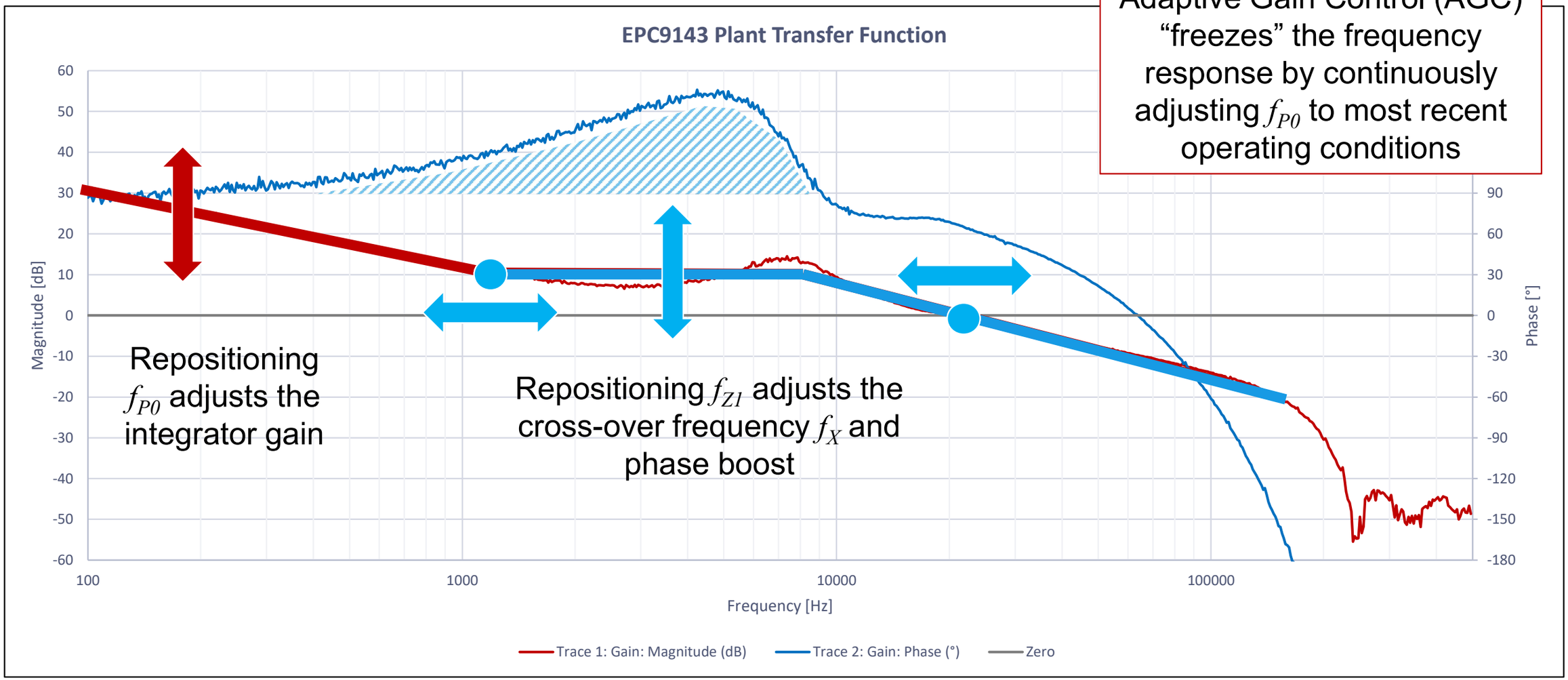
Frequency Response Adjustment



Type IV Adaptive Voltage Mode Control

Frequency Response Adjustment

Adaptive Gain Control (AGC) "freezes" the frequency response by continuously adjusting f_{P0} to most recent operating conditions



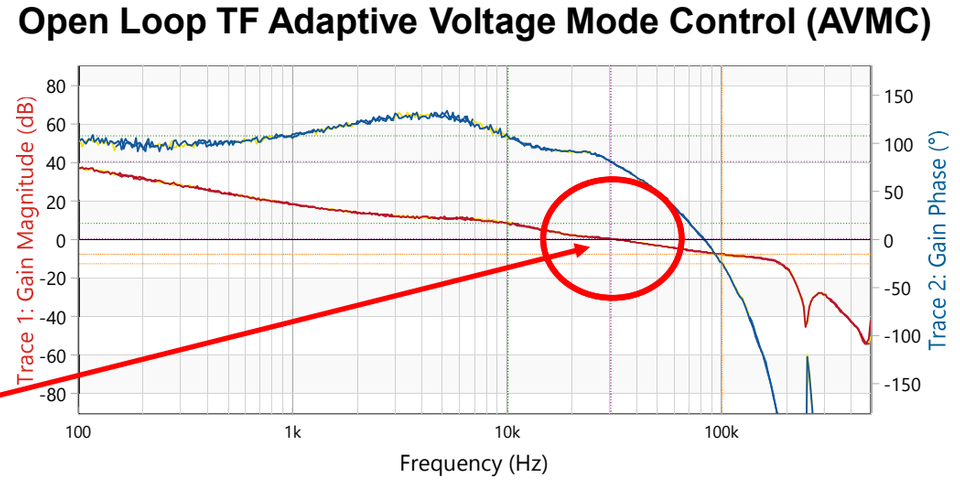
Type IV Adaptive Voltage Mode Control

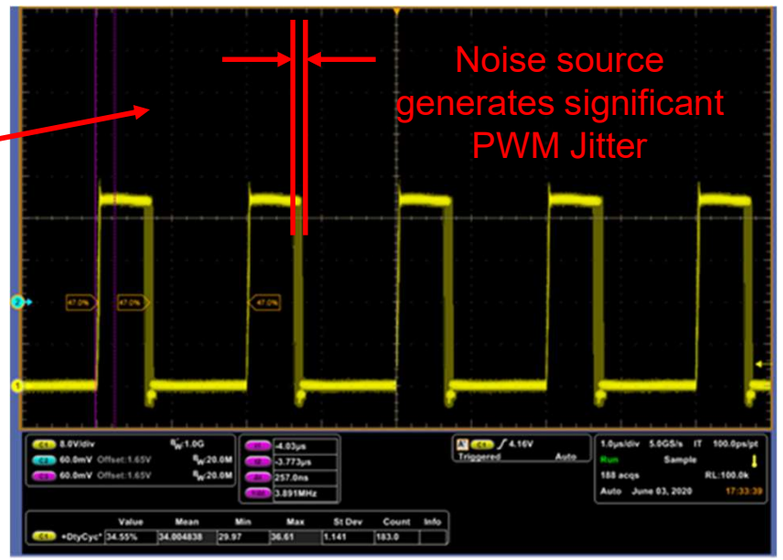
Adjustment Limits

Theoretically there is no limitation of the maximum cross-over frequency f_X other than the physical limitations given by the switching frequency. Hence, high control bandwidth can be achieved.

However, in this design, if the cross-over frequency f_X matches the location of the second resonant frequency, a conditionally stable region appears.

This conditionally stable region results in poor noise rejection in this flat area region. This noise is picked up by the ADC, passes the control loop at a gain close to =1 and gets amplified at the PWM output as observable jitter.



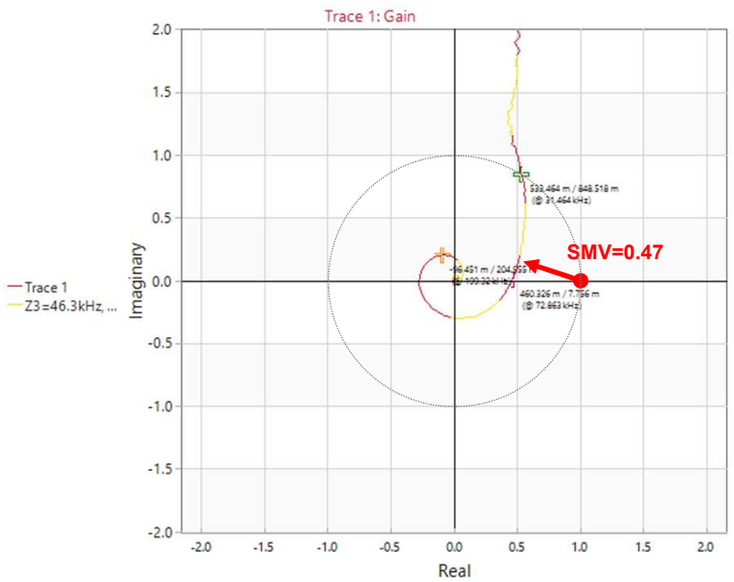


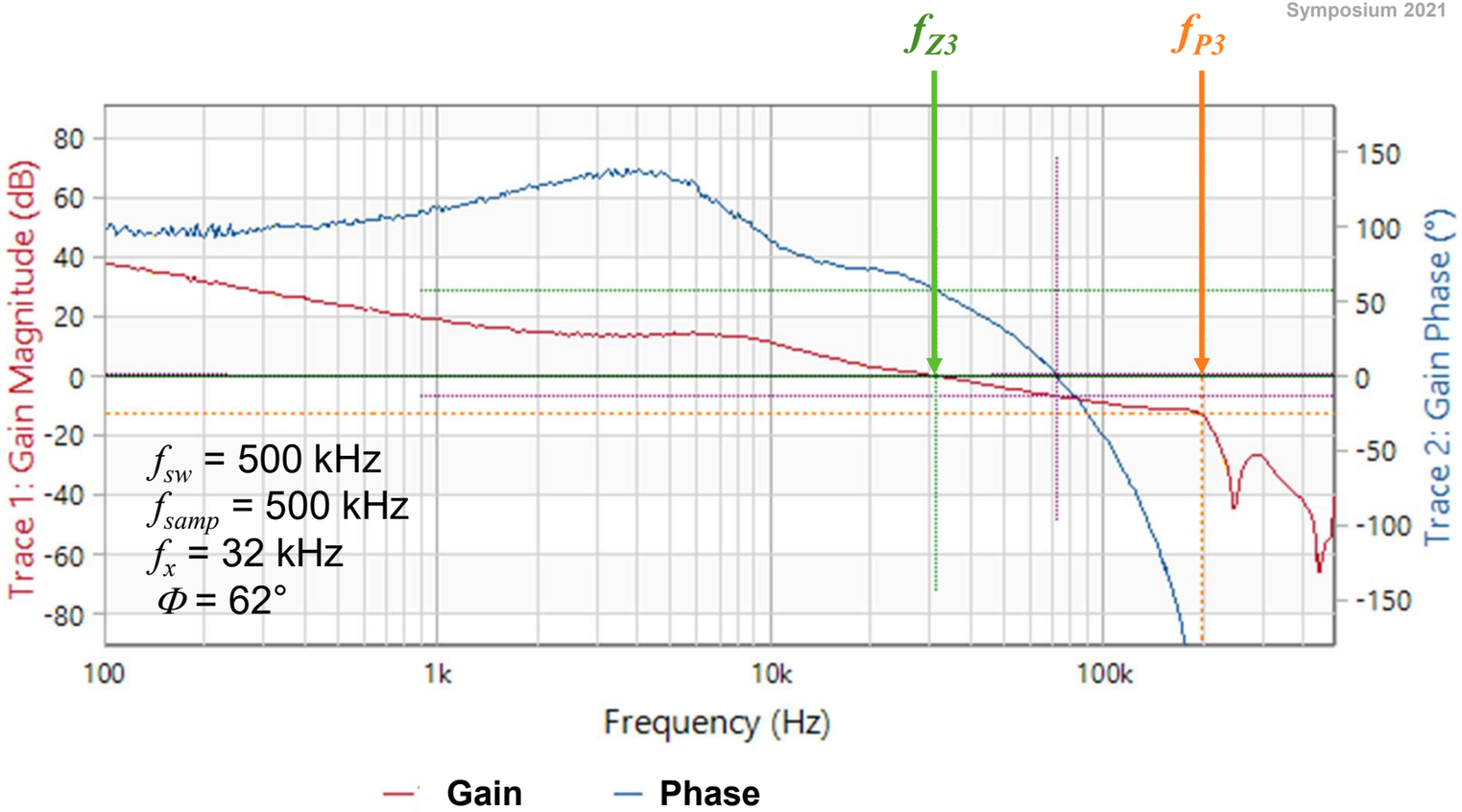
Type IV Adaptive Voltage Mode Control

Adjustment Limits

Solution:

By introducing one additional pole-zero pair, the zero is used to compensate the second resonant frequency pole while the second pole is used to improve high frequency noise rejection.

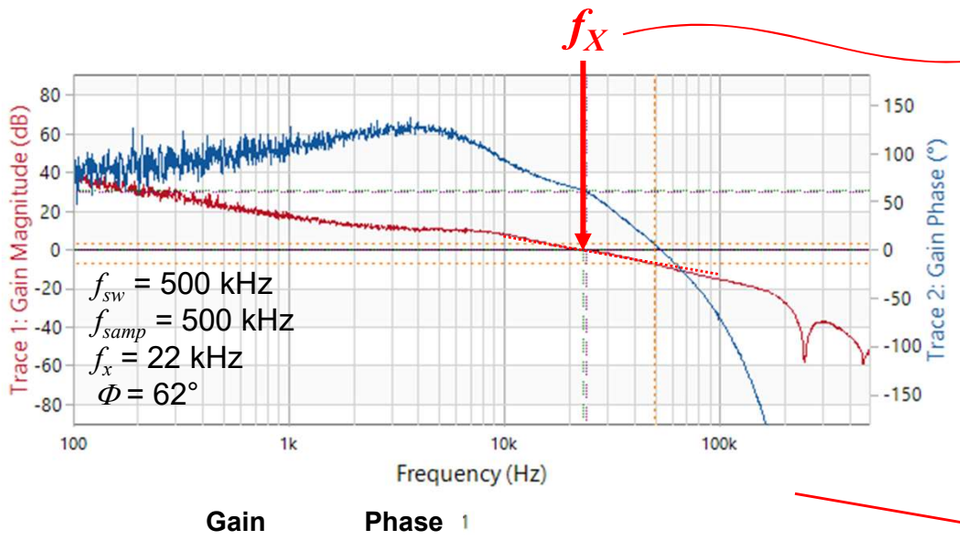


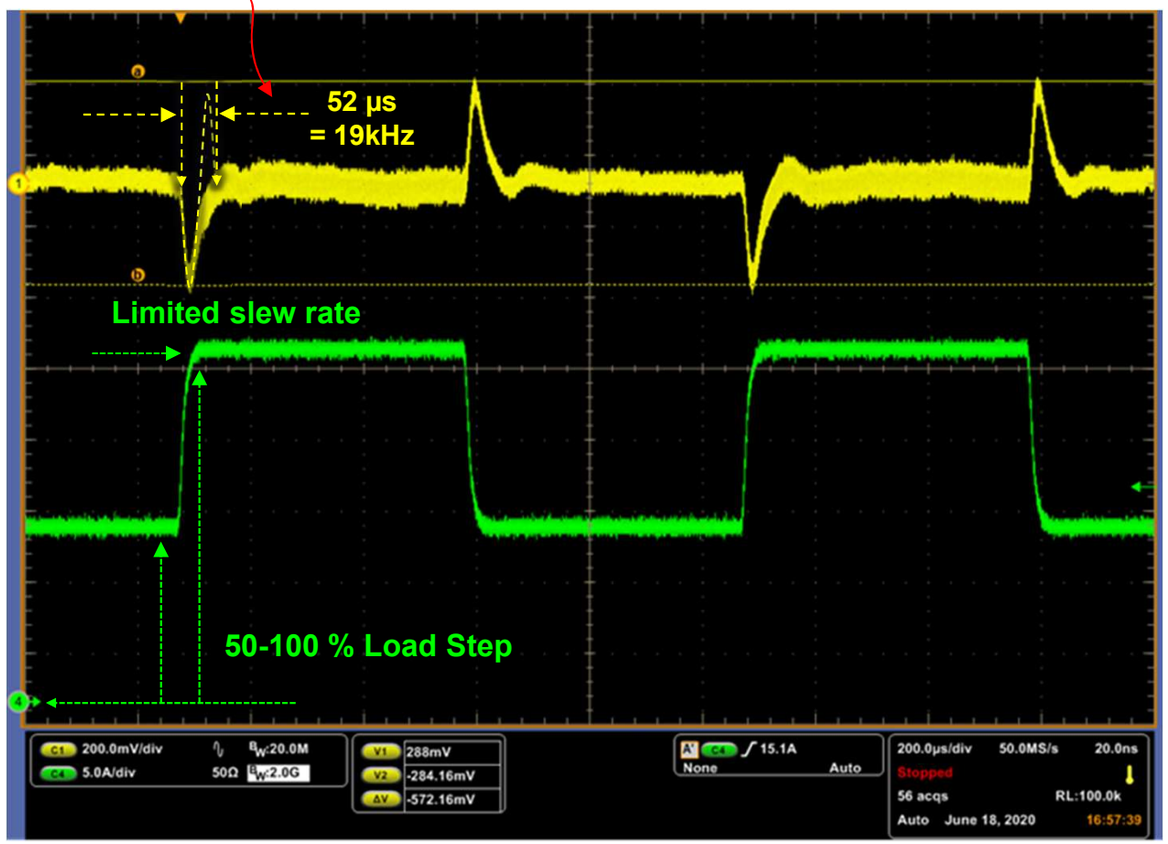


Once the loop is adjusted, Adaptive Loop Gain Modulation (AGC) is used to stabilize and fix the overall loop gain when operating conditions divert from the nominal conditions of V_{IN}=48 V / V_{OUT}=12 V DC

Type IV Adaptive Voltage Mode Control

Large Signal Validation of Type IV AVMC





After introducing adaptive gain modulation and the additional pole-zero-pair, the loop got adjusted for better phase margin of $\Phi > 60°$. At fx, the gain slope meets exact -20 dB/dec and then rolls off softly at higher frequencies.

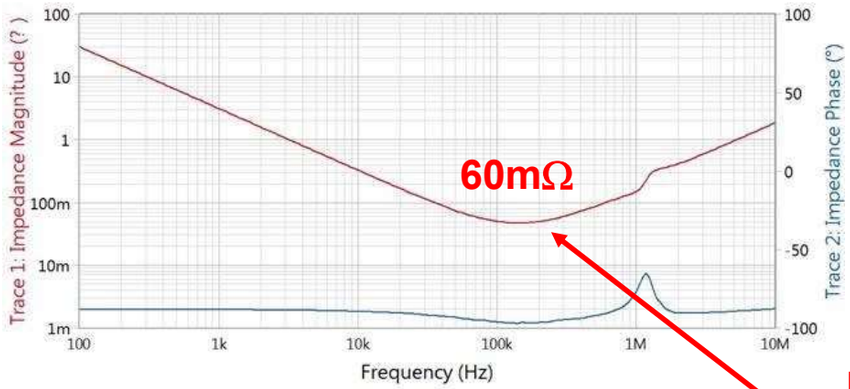
The measured fx = 22 kHz in the frequency domain correlates sufficiently with the step response frequency in the time domain of f_{STEP} =19 kHz.

Type IV Adaptive Voltage Mode Control

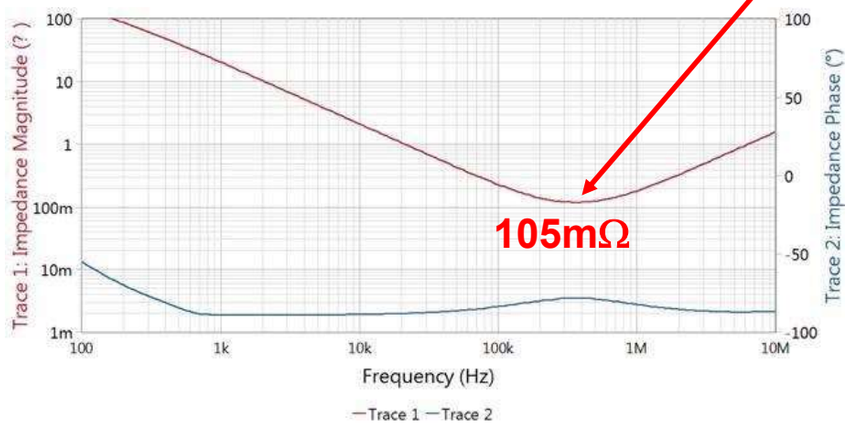
Impedance Tuning

Recommended:
Check component values independent from circuit for verification

EPC9531 Test Fixture

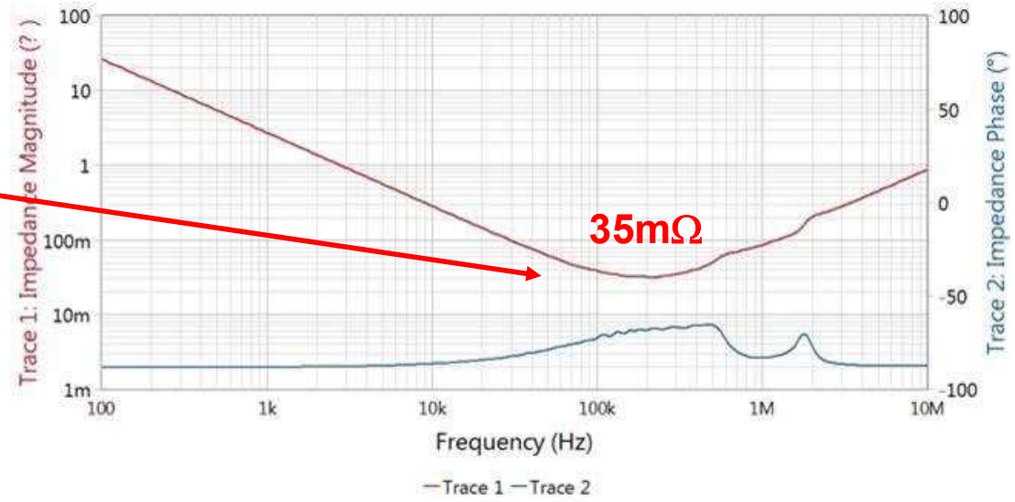


EPC9143 16th brick Power Module



Effective Capacitor ESR

EPC9143 mounted on EPC9531



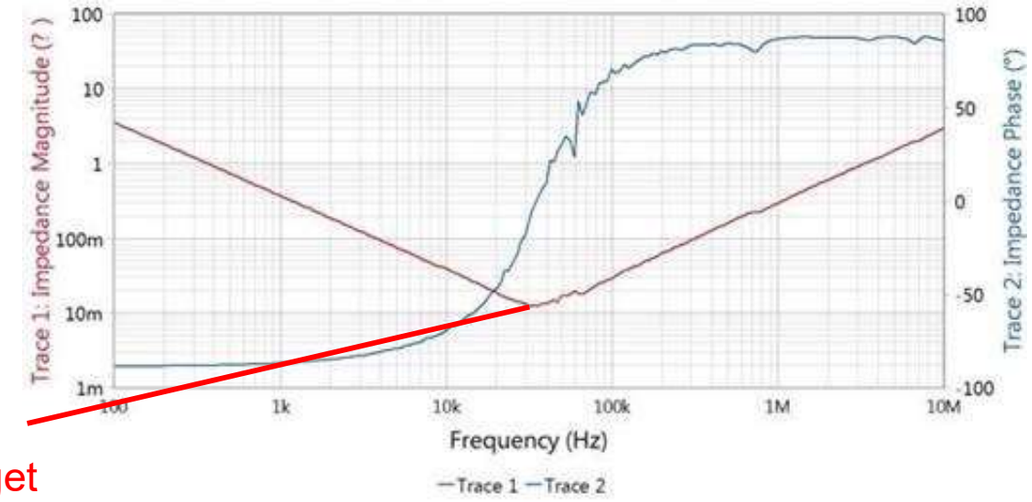
Measurements are taken at board terminals. Value Effective Capacitor ESR therefore includes additional resistance of traces.

Type IV Adaptive Voltage Mode Control

AVMC Output Impedance Tuning

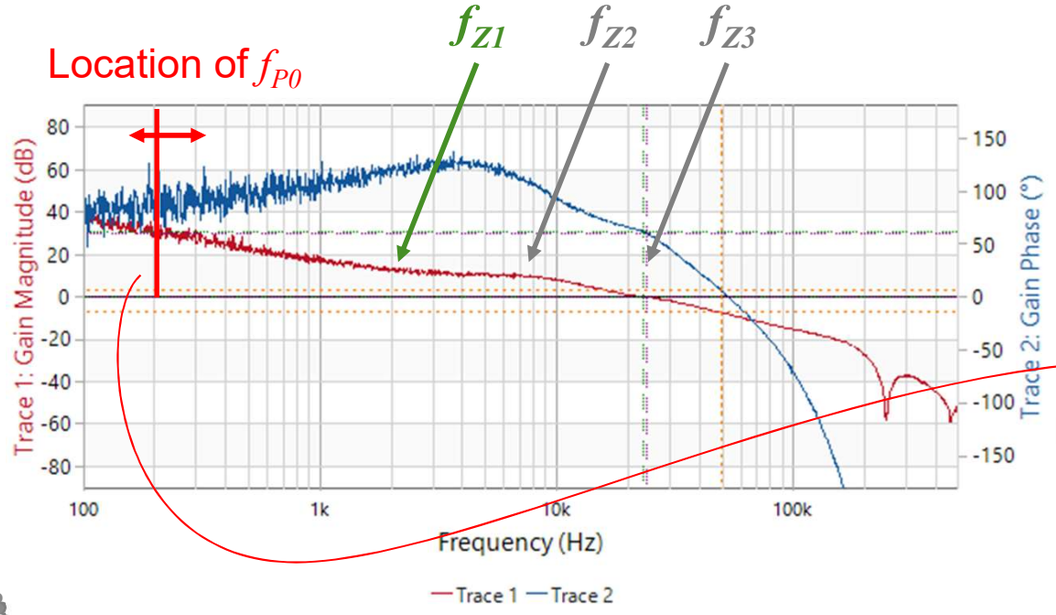
With a second order control system, the gain characteristic can be shaped in multiple ways. For output impedance tuning the location of the cross-over frequency of the pole at the origin is used to adjust the low frequency loop gain, while the location of the first zero f_{Z1} is used to set the open loop gain cross-over frequency f_X and loop phase boost region.

Unpowered



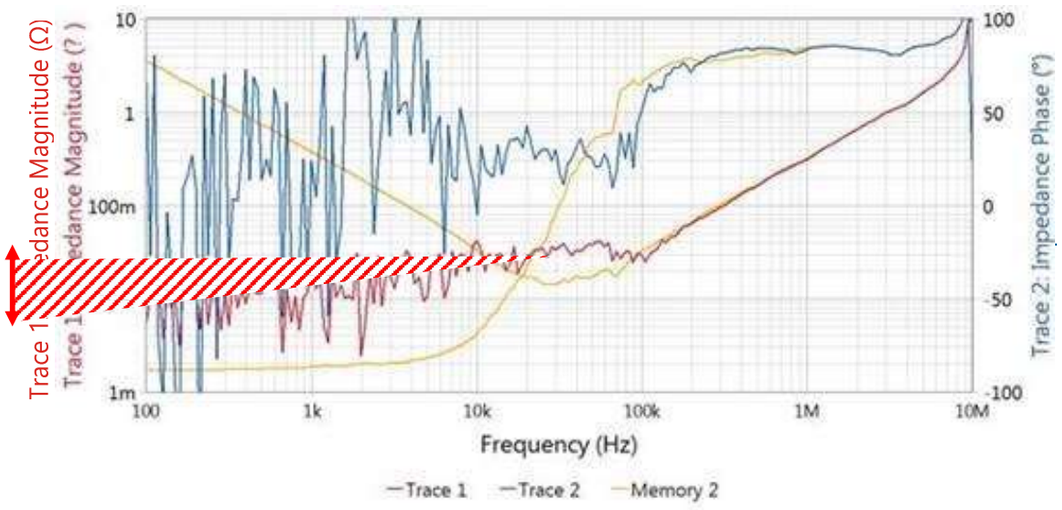
Impedance Matching Target

Location of f_{P0}

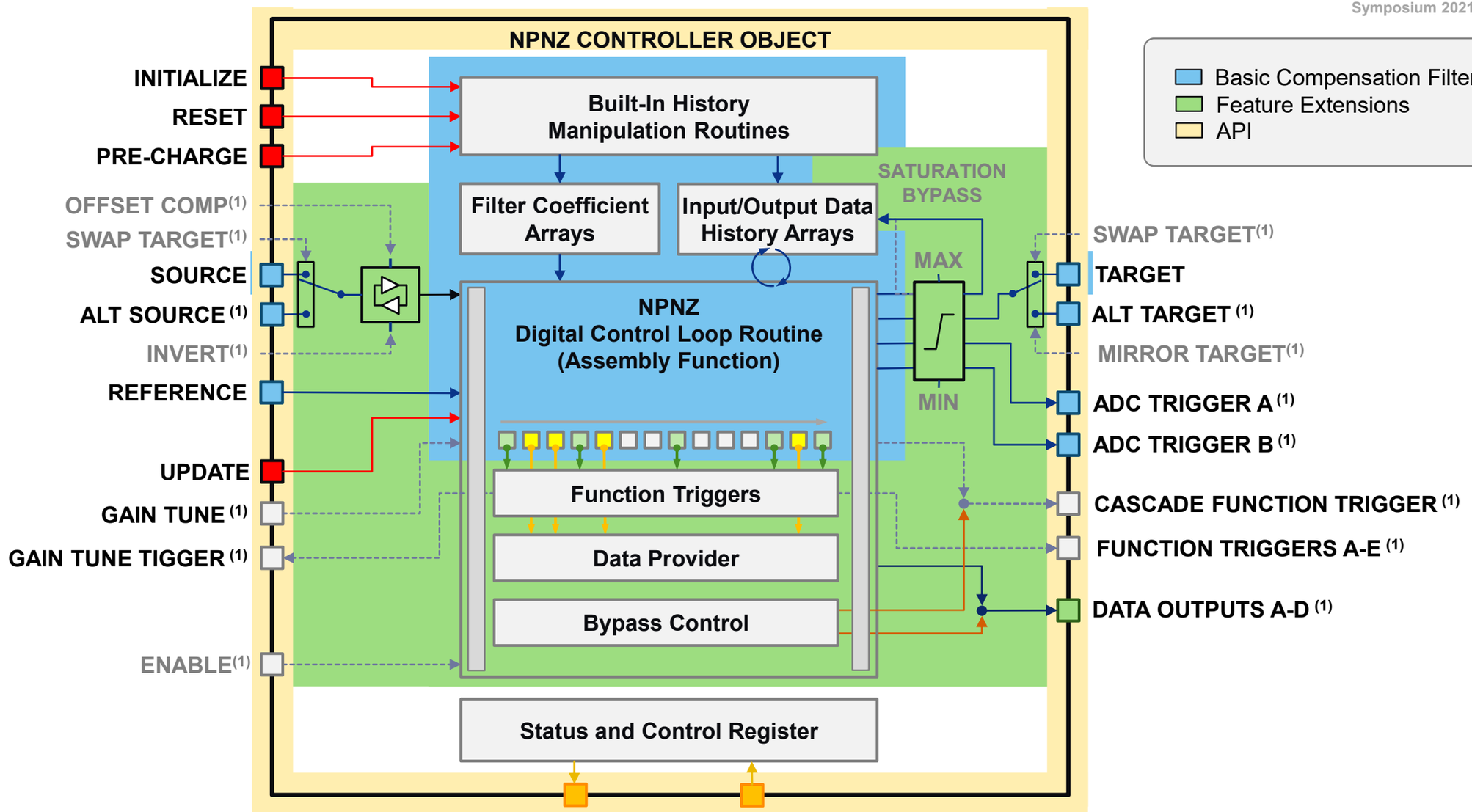


Integrator Gain

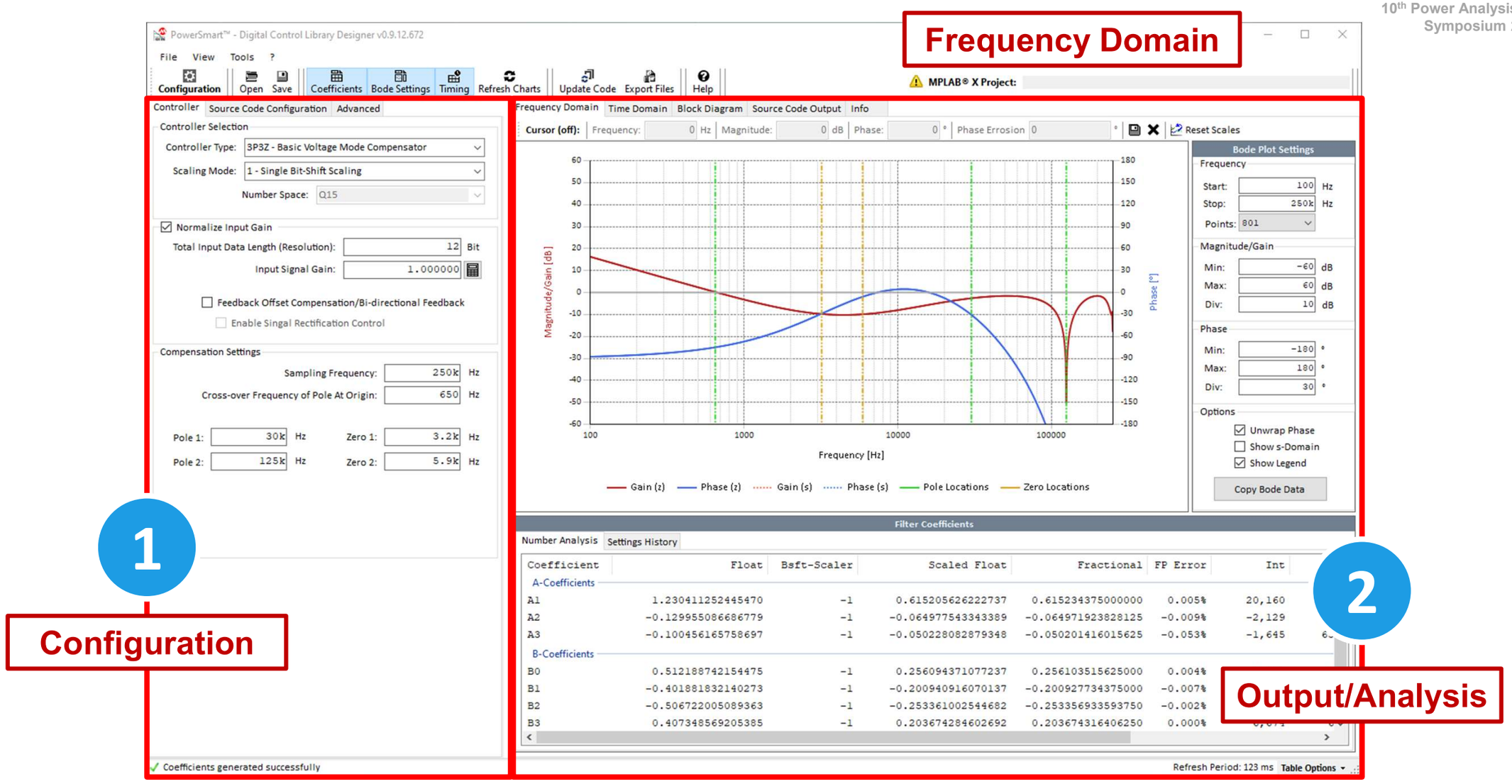
Powered



Controller Block Diagram



PowerSmart™ Digital Control Library Designer



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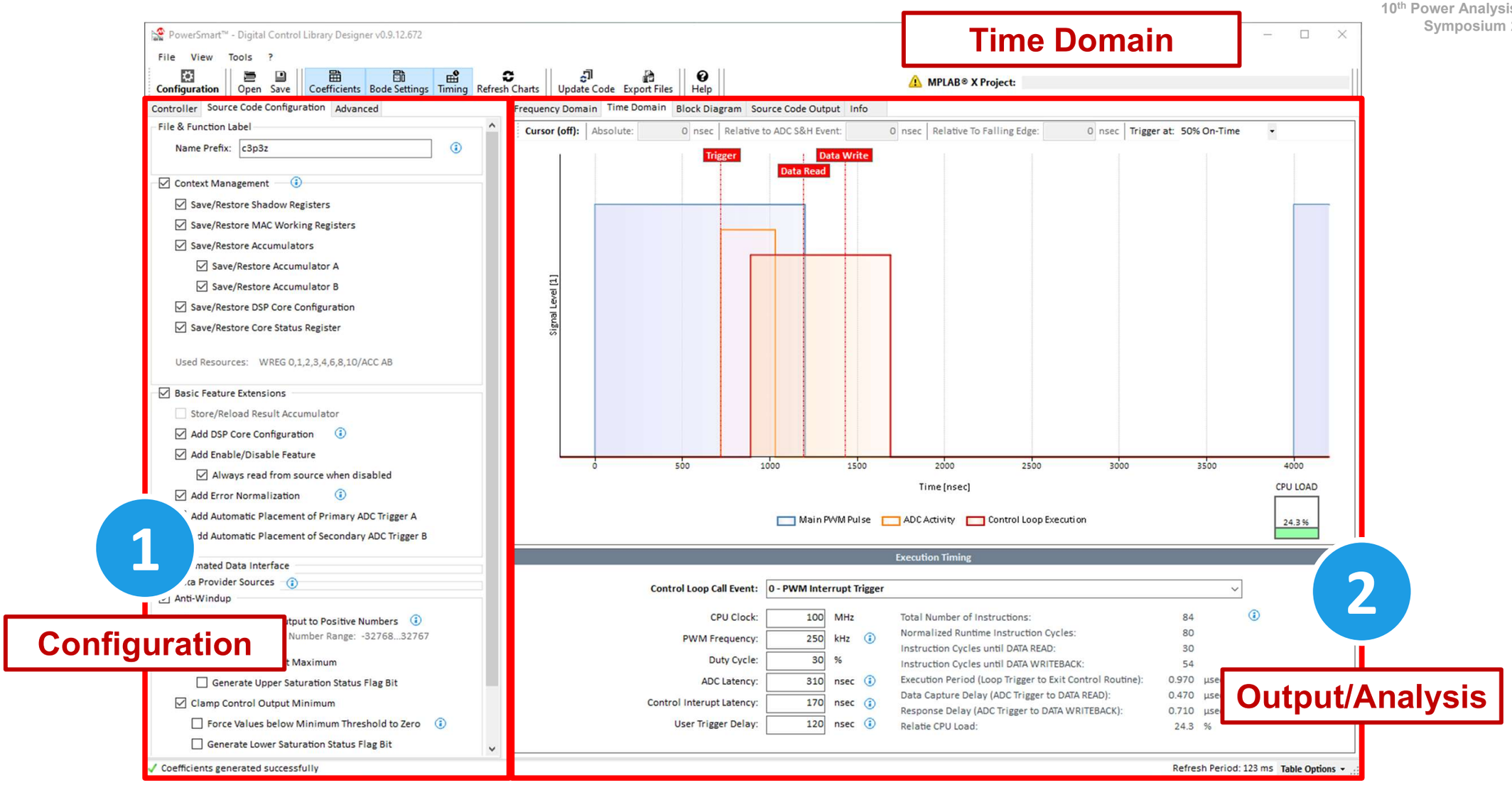

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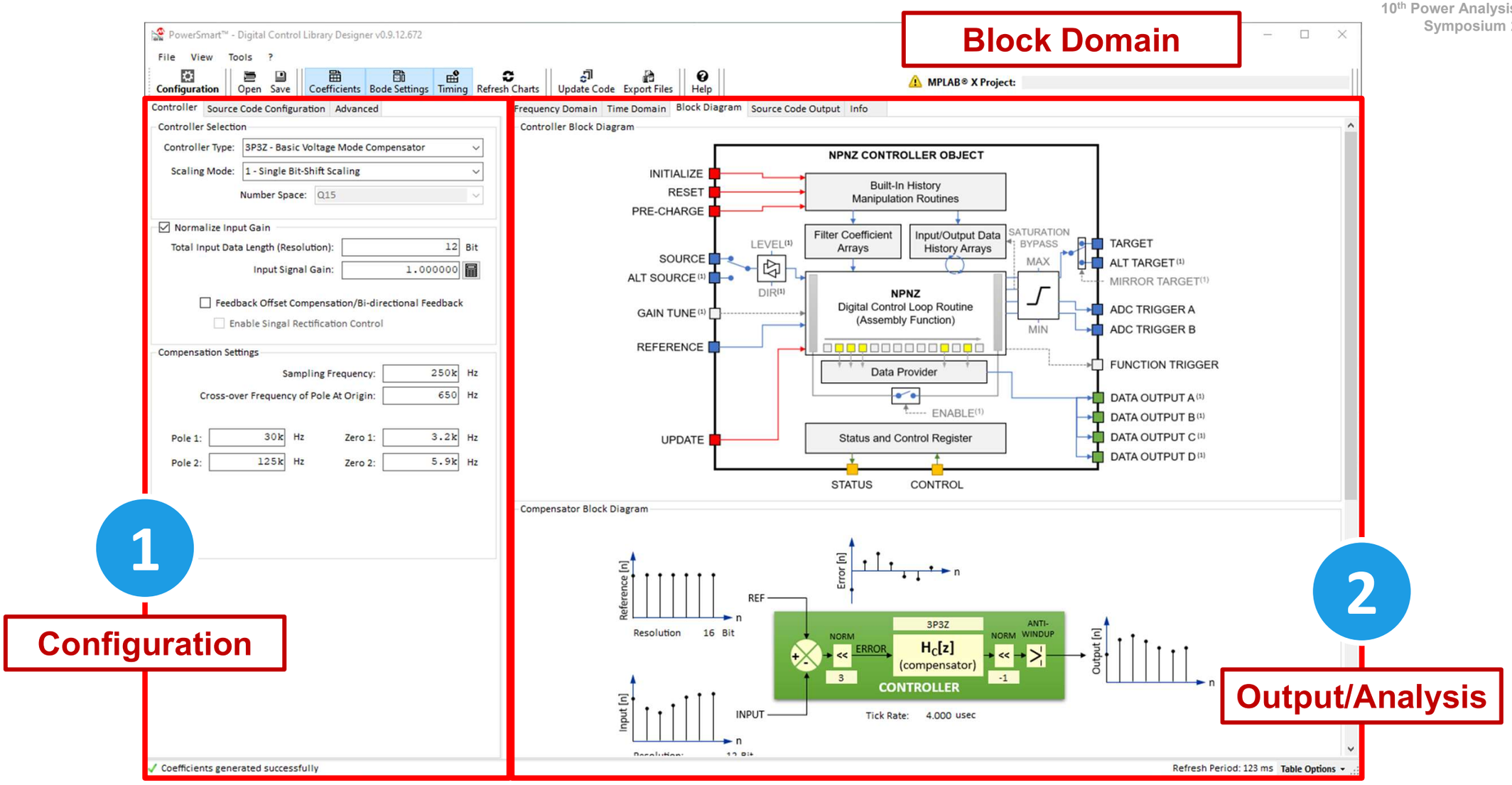

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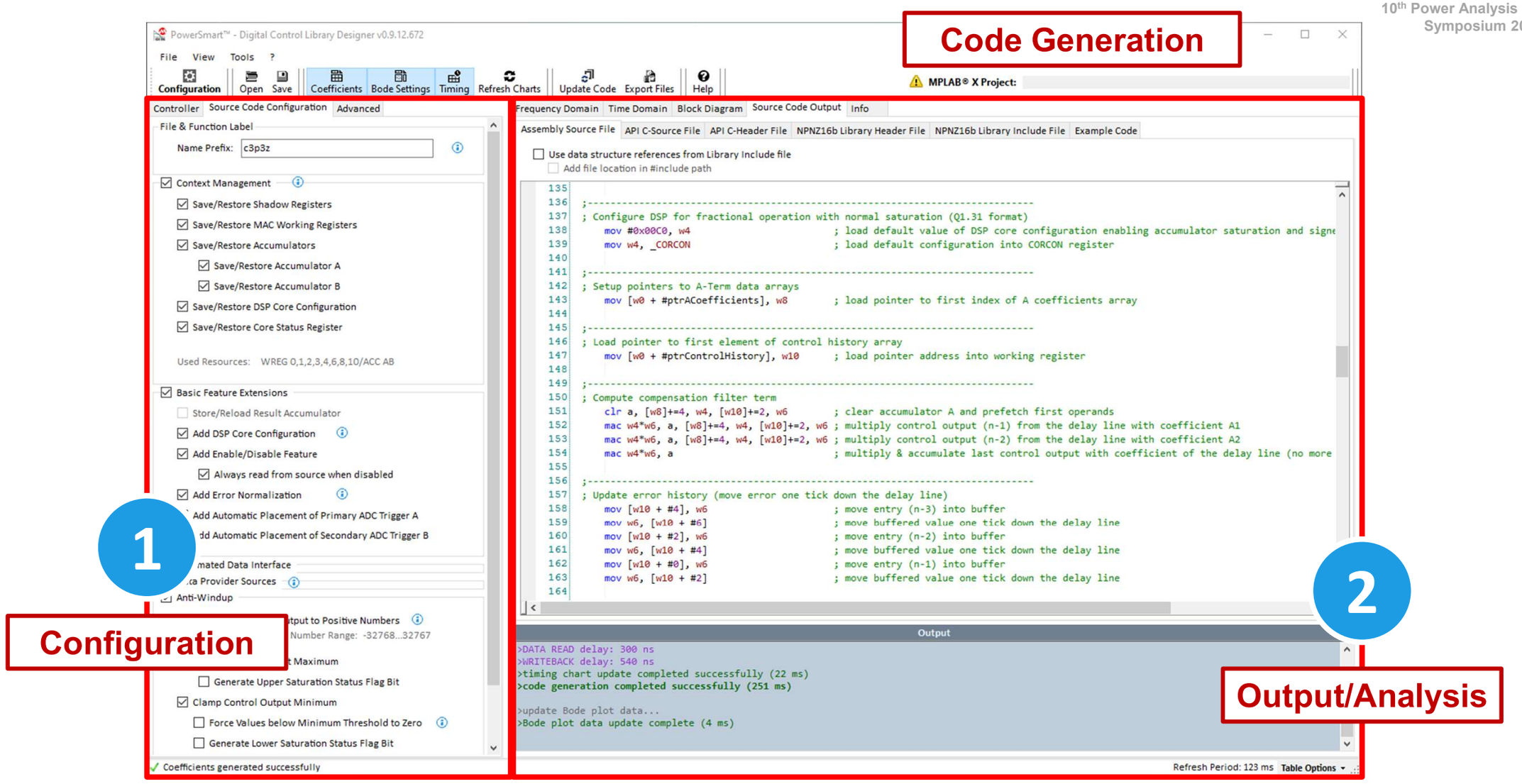
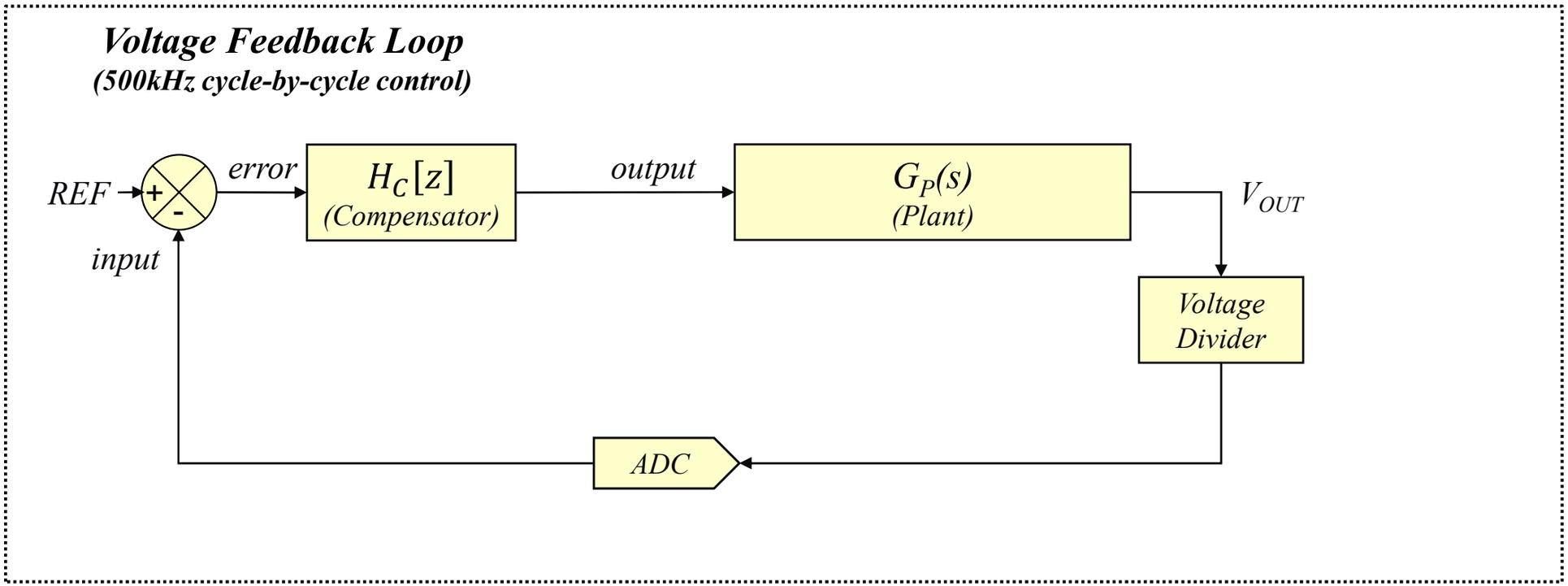


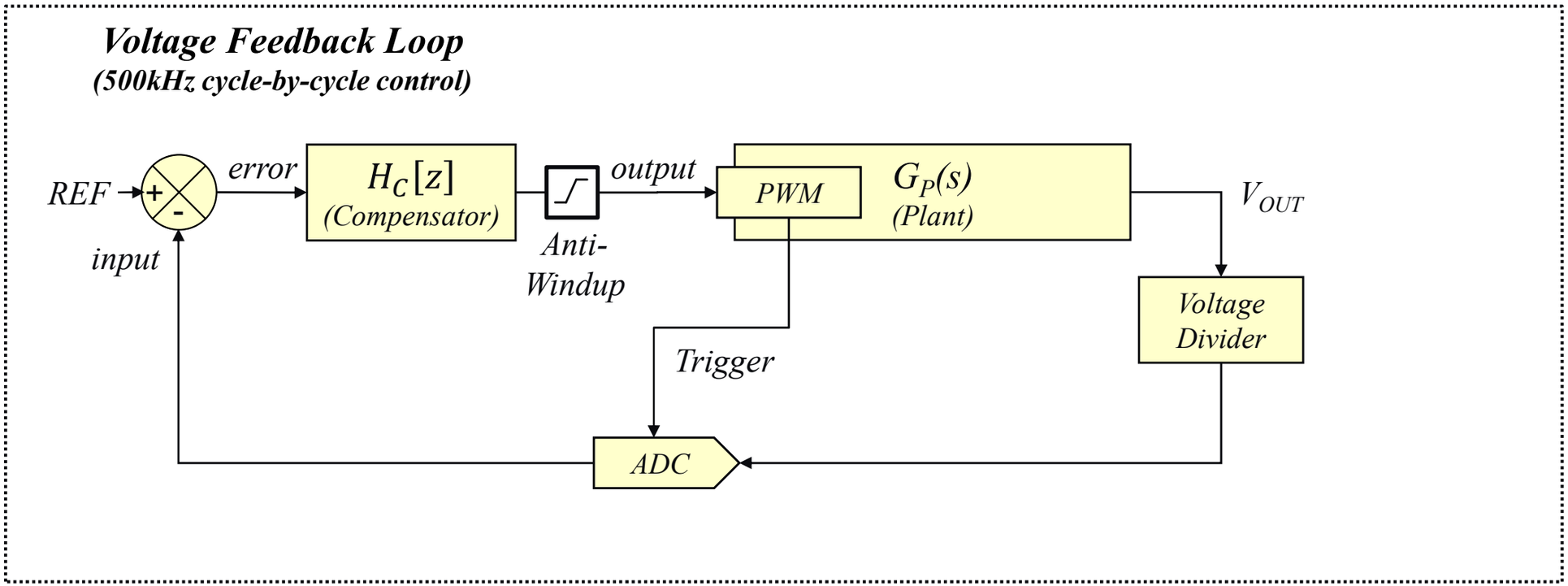
Building the Control System

Basic Voltage Mode Control Implementation



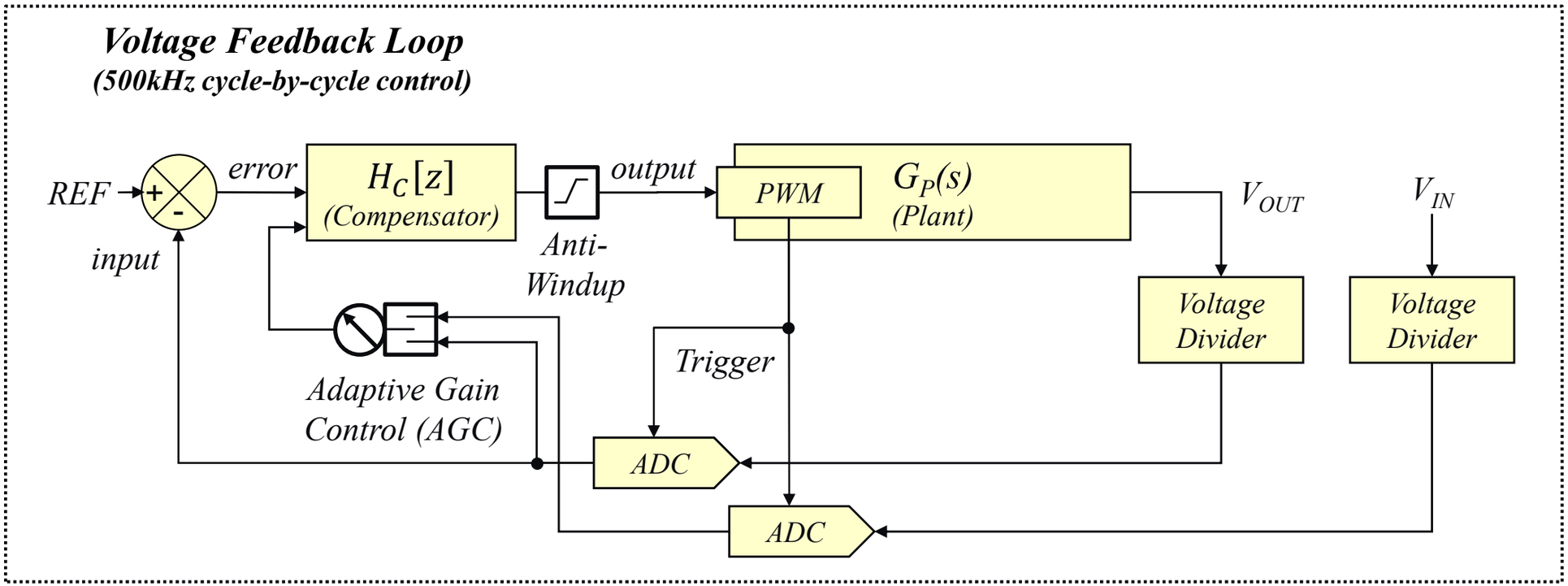
Building the Control System

Peripheral Interconnections



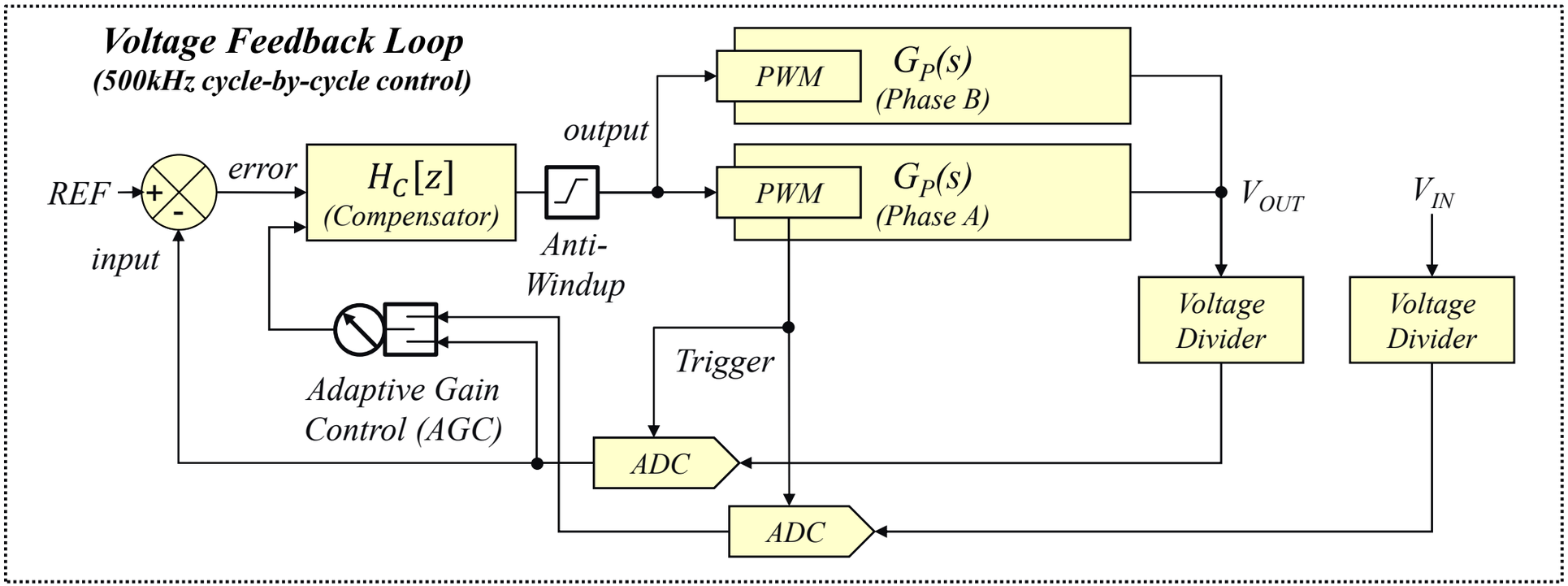
Building the Control System

Adaptive Gain Control Implementation



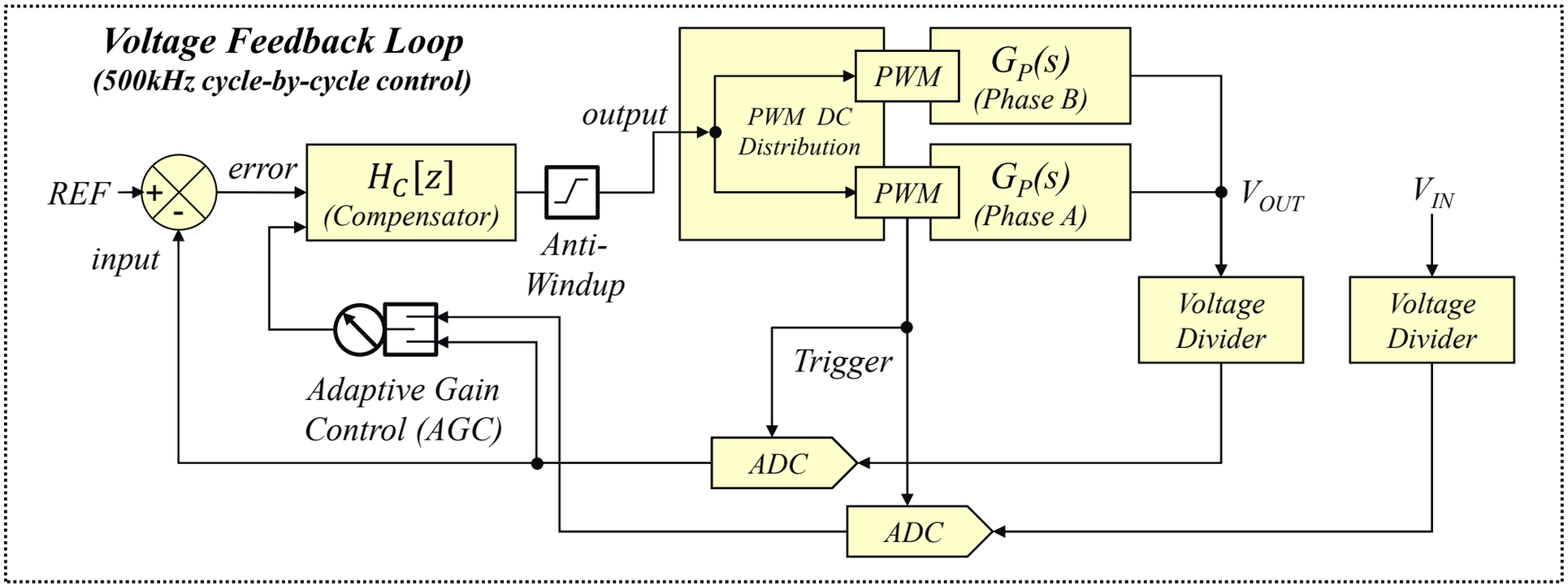
Building the Control System

PWM Mirroring with Phase Shift



Building the Control System

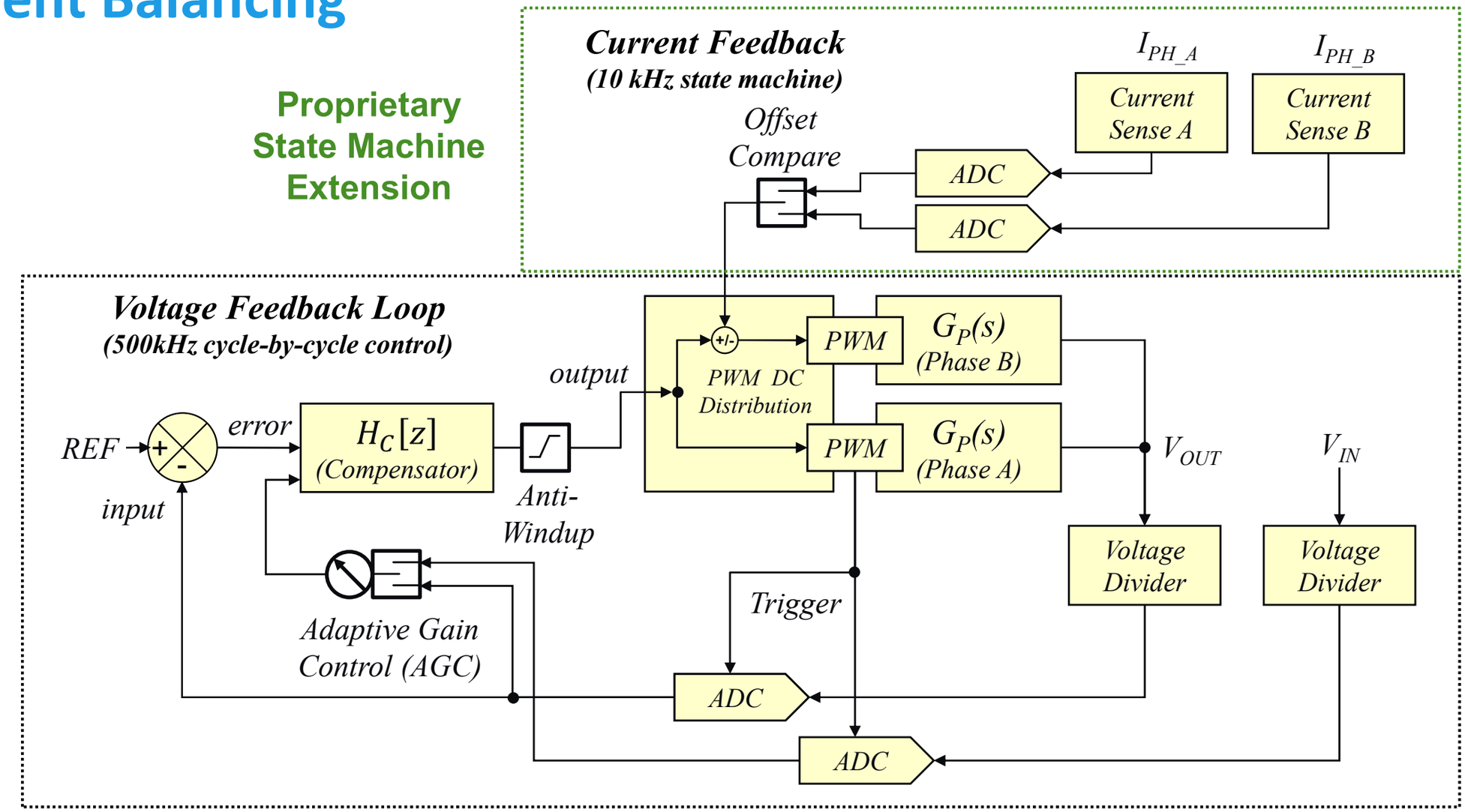
PWM Duty Cycle Distribution



Building the Control System

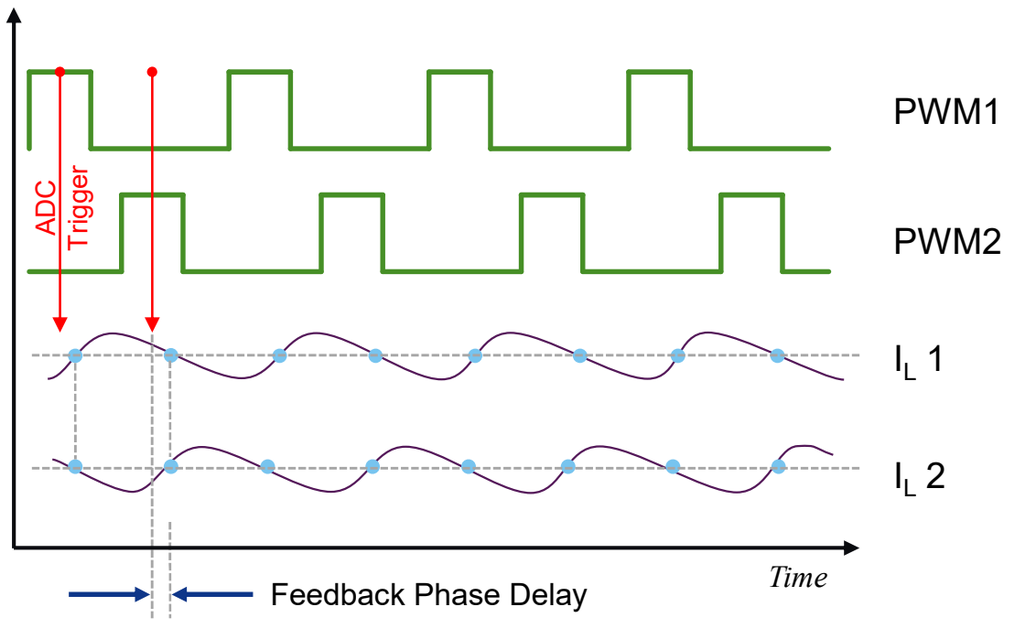
Current Balancing

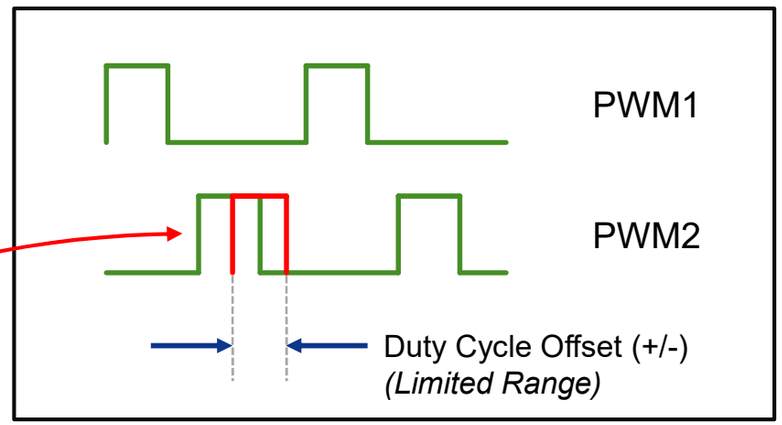
Proprietary State Machine Extension



Current Balancing Implementation

Simple Bit Tracker Implementation





$$\Delta I_L = I_{L1} - I_{L2}$$

Sign-Bit of result is OR'ed with 0x0001
and added to duty cycle of PWM2
every 100 us (=10 kHz)
resulting in adjustment in 250 ps
increments/decrements

Agenda

- 48V Rack Power Distribution Networks and Conversion Points
- 300W 48V 1/16th Brick DC/DC Converter Power Module
  - EPC9143: Unidirectional Power Module
  - EPC9151: Bi-Directional Power Module
- High-Speed Multiphase Controller Design
  - Type IV Adaptive Voltage Mode Control
  - PWM Steering and High-Speed Current Balancing
- **Summary**

Summary

- **Digital control loops allows**
  - Using real and complex poles and zeros to overcome complex frequency domain limitations
  - Independent pole and zero locations allow runtime tuning
  - Runtime tuning allows adaptation of loop gain to operating conditions
  - Higher order control systems allow independent tuning of output impedance and bandwidth
- **Impedance and Bandwidth Tuning**
  - simplifies system integration
  - Improves overall system stability
  - Minimizes cost and size

Thank You!

May the Power be with you!

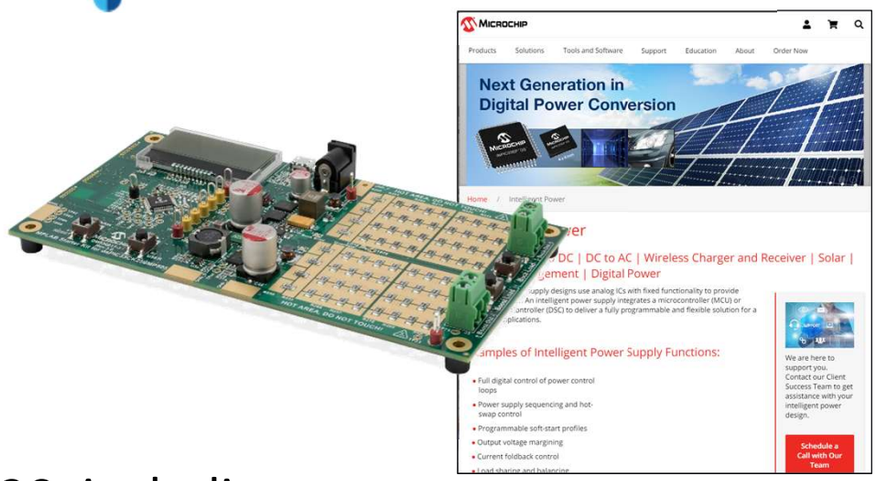
POWER
YOUR IDEAS!

Appendix

Digital Power

- **Getting Started in Digital Power**
  - Intelligent Power Design Center:
    https://www.microchip.com/power
- **How-2 Starter Kits**
  - Digital Power Starter Kit 3 (Part-No. DM330017-3):
    https://www.microchip.com/dm330017-3
- **Training:**
  - Microchip University (Virtual Training Platform):
    https://secure.microchip.com/mu

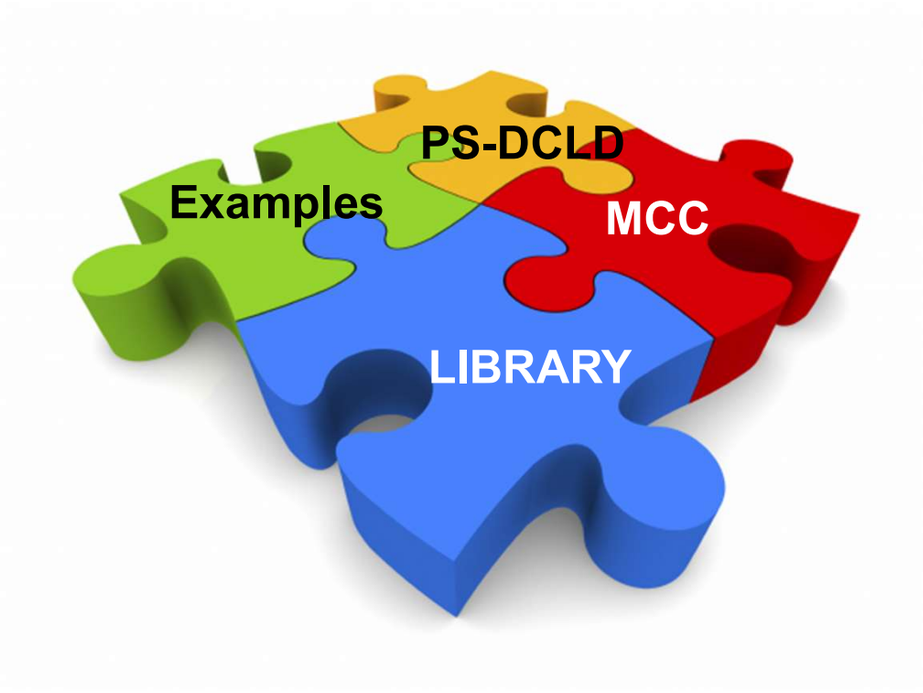
MICROCHIP UNIVERSITY

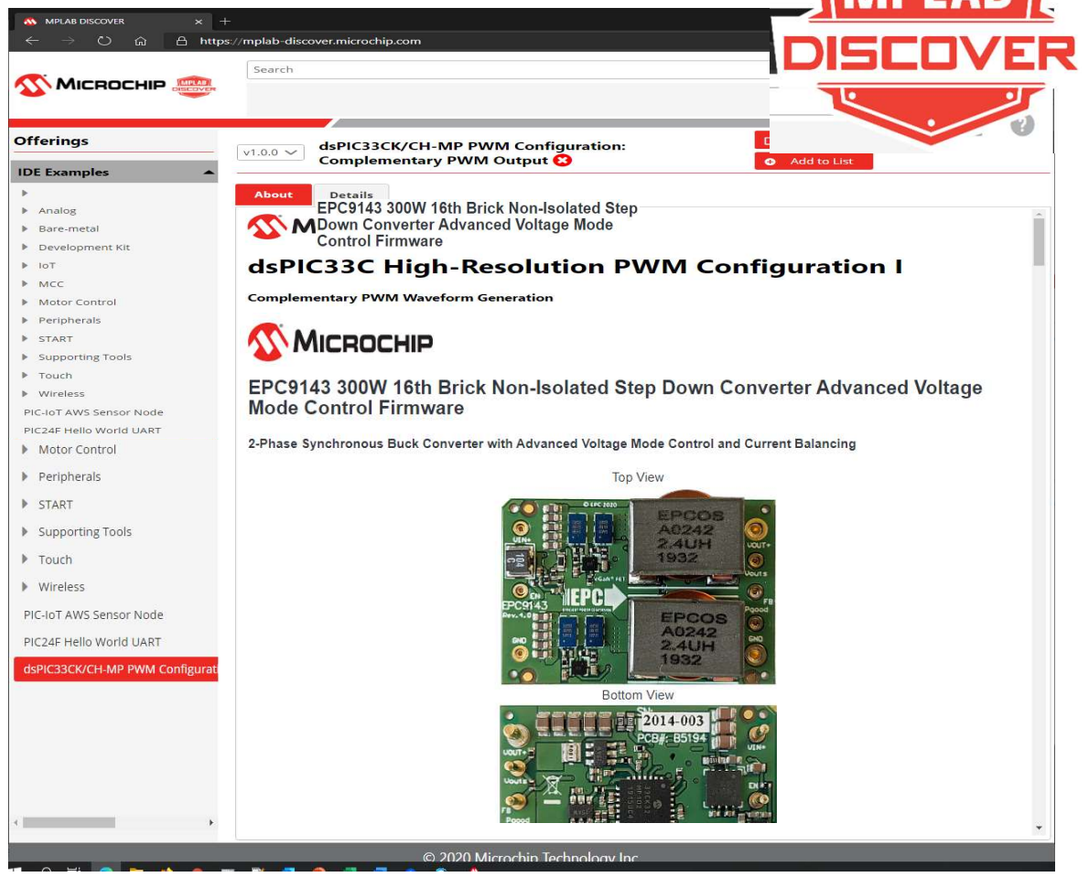


Please note:
All Face-2-Face workshops have been suspended in early 2020, including the well-known MASTERs conferences usually conducted in 9 nations around the globe. For the time being all available trainings have been moved to our new virtual training platform ***Microchip University***.

Digital Power Design Resources

- **Find hundreds of code examples and design tools on https://discover.microchip.com**





Product Websites

- **dsPIC33CK32MP102: Digital Signal Controller for SMPS Applications**
  https://www.microchip.com/dsPIC33CK32MP102

- **MCP6C02: 65 V Shunt Current Sense Amplifier**
  https://www.microchip.com/mcp6c02

- **EPC9143: 300 W 48 V Unidirectional 16th Brick Reference Design**
  https://www.microchip.com/EPC9143

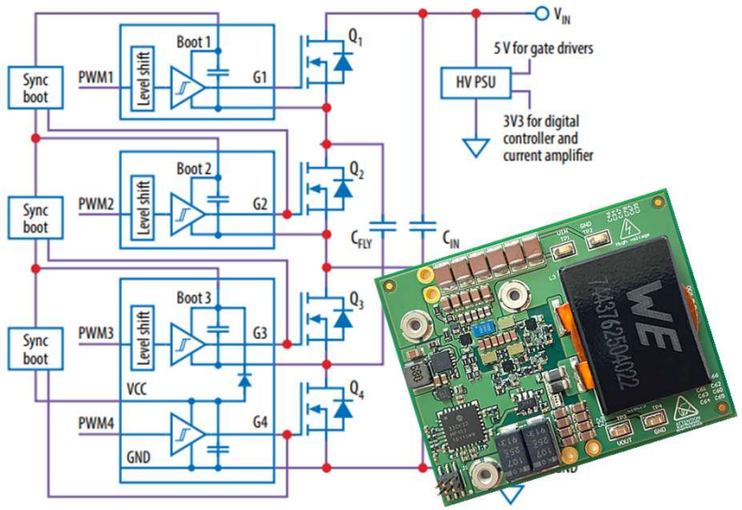
- **EPC9151: 300 W 48 V Bidirectional 16th Brick Reference Design**
  https://www.microchip.com/EPC9151

Related Product Websites

- **EPC9148: 250 W 48 V Three-level Synchronous Buck Converter**

  Ultra-Thin, multi-level converter for high performance computing systems

  https://www.microchip.com/EPC9148



- **EPC9153: 250 W 48 V High Efficiency, Thin Power Module**

  Thin Power Module for high performance computing systems with 200% over-power capability

  https://www.microchip.com/EPC9153