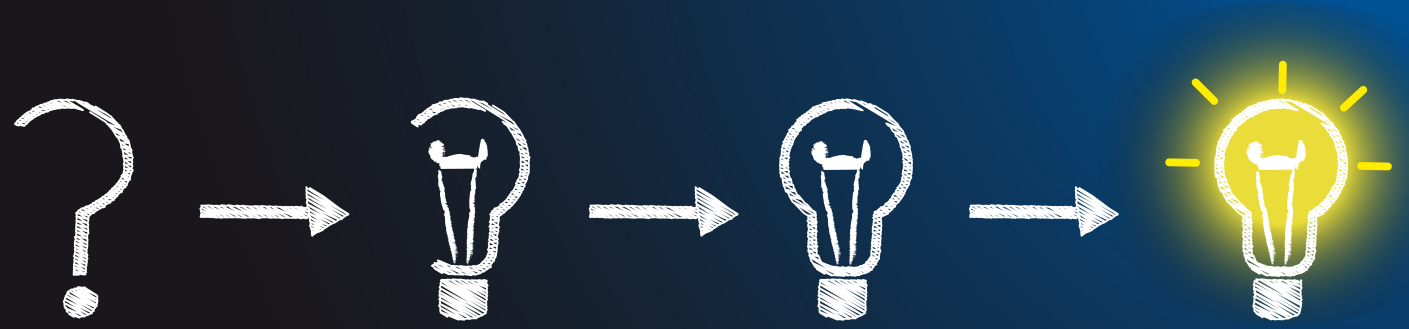


10th Power Analysis & Design Symposium

March 10th, 2021 - Worldwide (Virtual)

The Interactions Between Power Electronics, Power Integrity, Signal Integrity and EMI

by Steve Sandler - Picotest

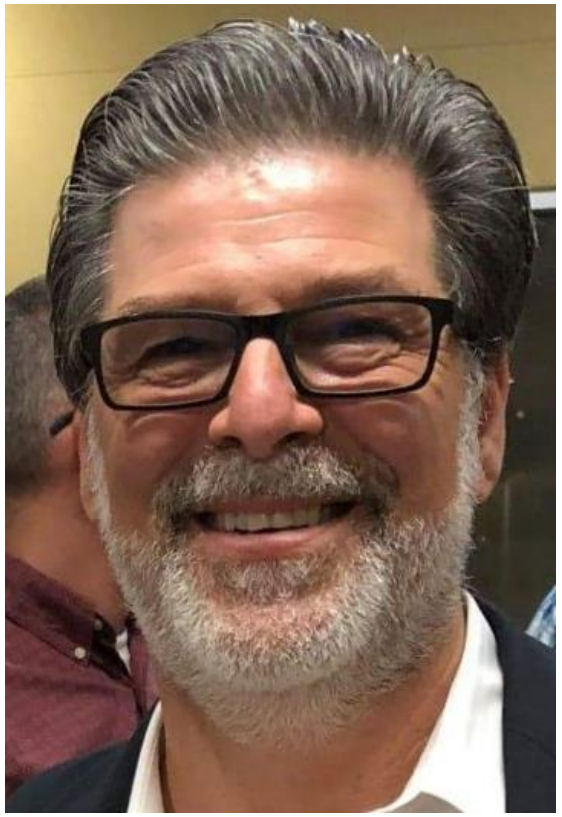
OMICRON LAB

The Interactions Between Power Electronics, Power Integrity, Signal Integrity, and EMI

Steven M. Sandler - Picotest

10th Power Analysis & Design Symposium 2021 (VIRTUAL)
March 10, 2021

Bio



- **Steve Sandler** has been involved with power system engineering for more than 40 years. Steve is the founder of PICOTEST.com, a company specializing in power integrity solutions including measurement products, services and training. He frequently lectures and leads workshops internationally on the topics of power, PDN and distributed systems and is a Keysight certified expert for EDA software.
- Steve frequently writes articles and books related to power supply and PDN performance and his latest book, Power Integrity Using ADS was published by Faraday Press in 2019. Steve founded AEi Systems, a well-established leader in worst case circuit analysis and troubleshooting of high reliability systems.

A Multitude of Disciplines

- Power Electronics (PE)
- Power Integrity (PI)
- Signal Integrity (SI)
- Electromagnetic Interference (EMI)

There are many others, which I wont talk about in this session, but there are also specializations in:

- RF and Microwave
- Millimeter Wave
- Analog and Sensors
- Thermal
- Structural Reliability

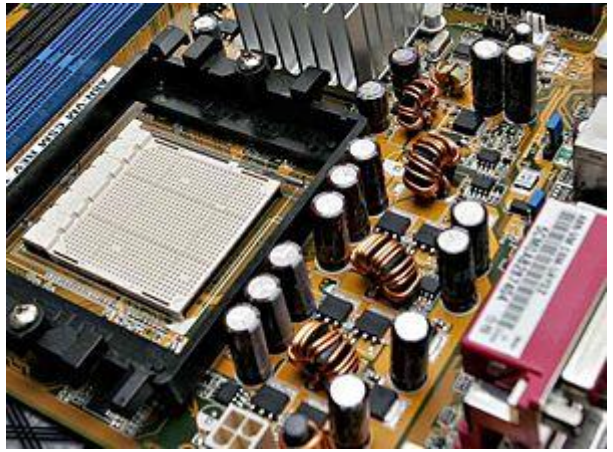
Power Electronics (PE)

Power Electronics is focused on the performance of the Power supply, POL switching regulator, or linear regulators. A typical modern system may have dozens of power electronics circuits, either individually or within integrated PMICs.

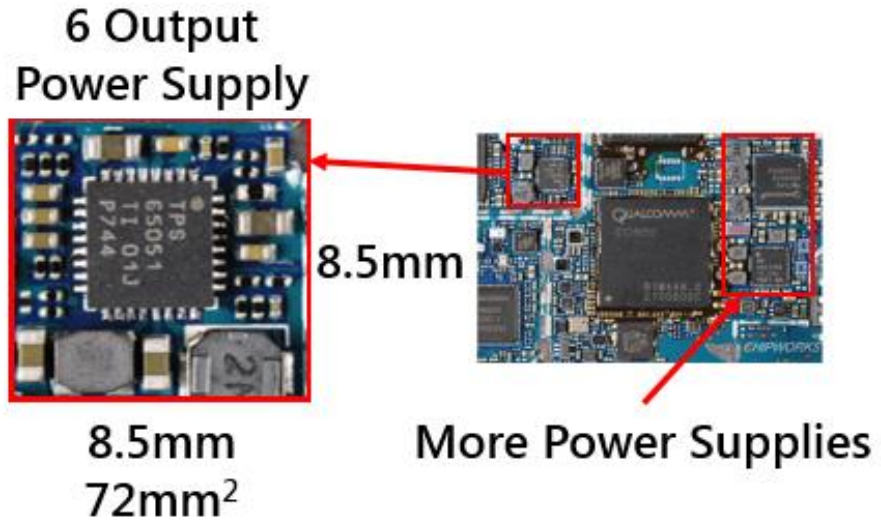
The Power Electronics Engineer has specific Figures of Merit (FOM) and this (non-exhaustive) list identifies some of the most common:

- Efficiency
- Size/Weight
- EMI
- Output **Impedance**
- Regulation
- Transient Response
- Ripple
- Cost

Multi-Phase VRM



High Density PMICs

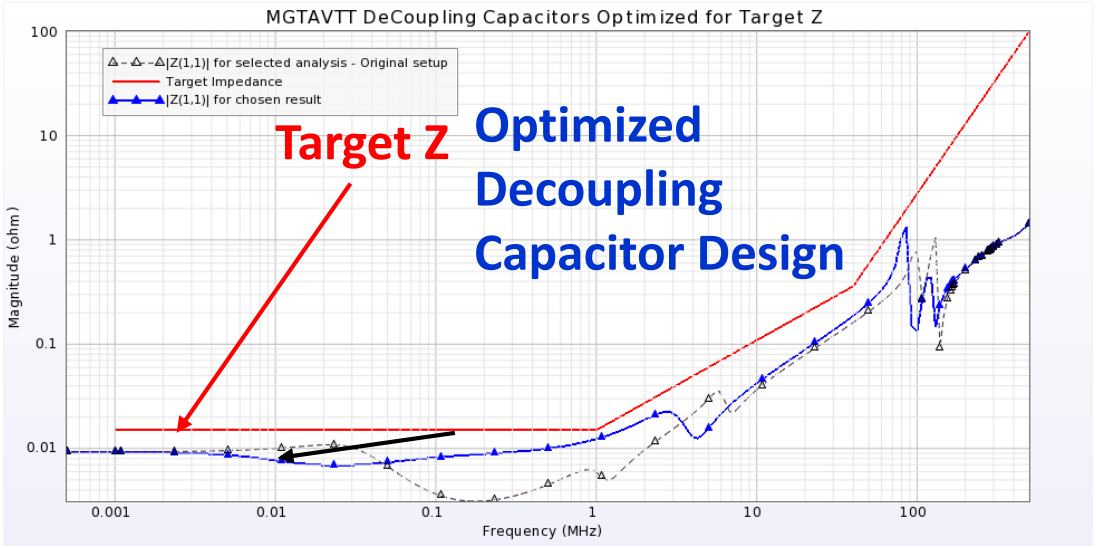


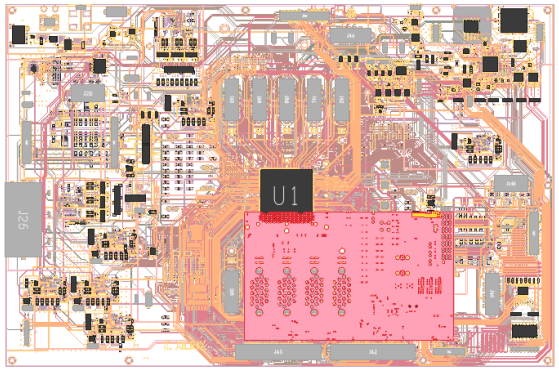
Power Integrity (PI)

Power Integrity is focused on receiving the low frequency power electronics output and distributing it to the high-speed and sensitive circuits. This includes the filtering and decoupling to support the load current demands that are much higher in frequency than the power electronics circuitry.

The Power Integrity Engineer also has specific goals, and this (non-exhaustive) list identifies some of the most common:

- Target **Impedance**
- Ripple Noise
- Excess Inductance





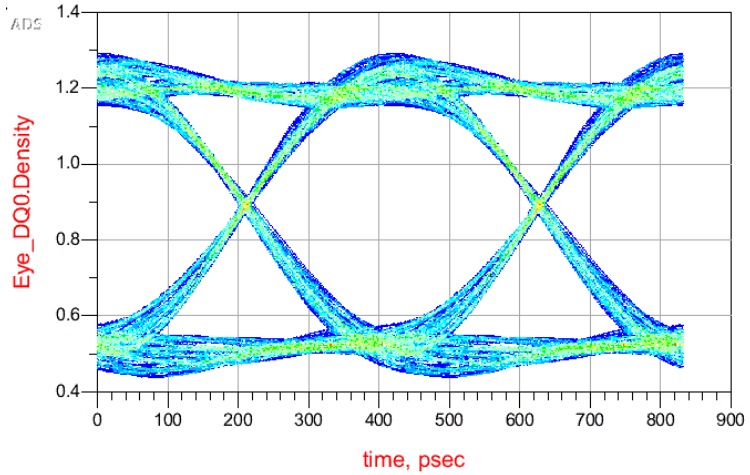
Images Copyright Keysight – Courtesy Heidi Barnes

Signal Integrity (SI)

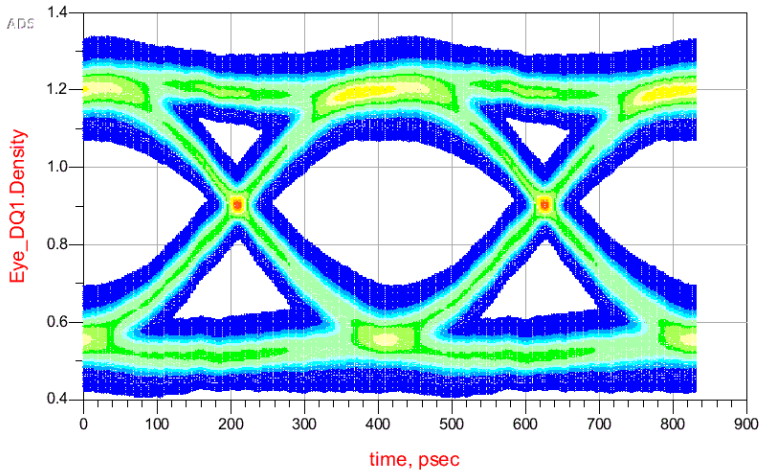
Signal Integrity is focused on transmitting and receiving high-speed data from one location to another. This includes mostly the degradation of the signal quality from the origin to its arrival at the destination. The majority of signal integrity analysis today is “Power-Aware,” meaning that it recognizes the contribution of the power supply and power integrity impacts on the transceiver performance

The Signal Integrity Engineer also has specific goals, and this (non-exhaustive) list identifies some of the most common:

- Jitter
- Crosstalk
- PSNR
- Channel **Impedance**



Eye Diagram without the effect of the PDN



Eye Diagram with PDN (Power-Aware SI)

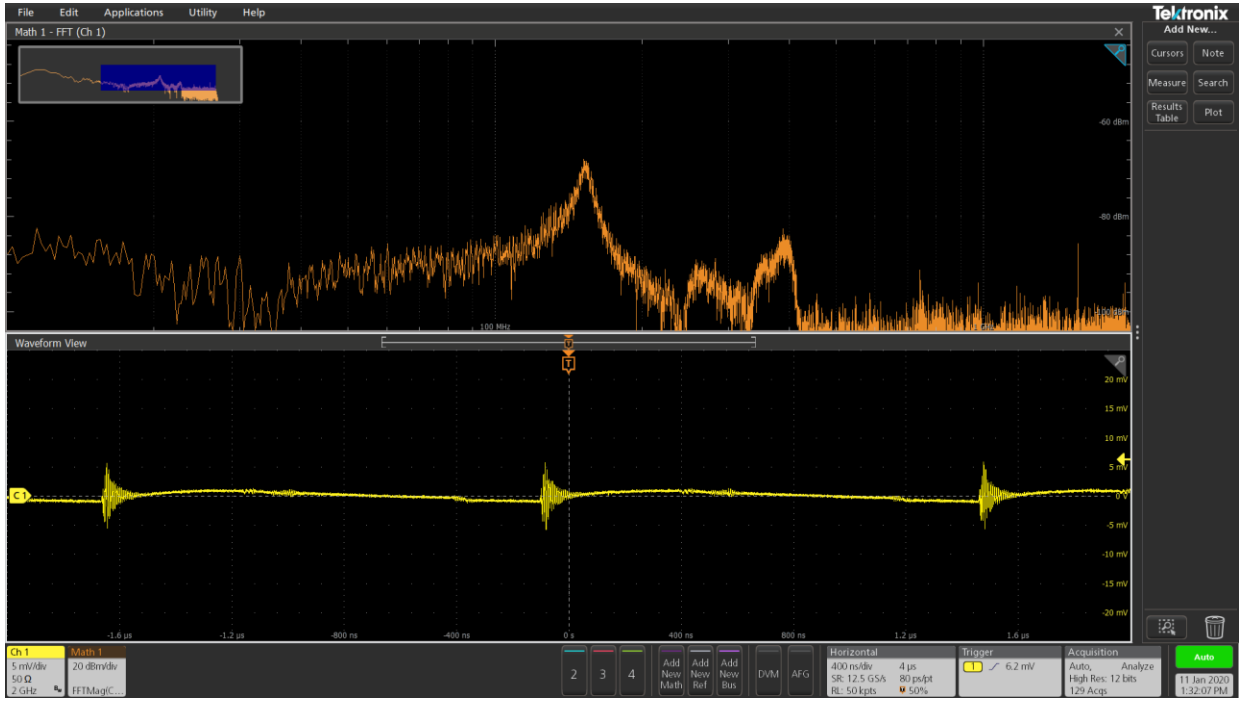
Images Copyright Keysight – Courtesy Heidi Barnes

Electromagnetic Interference (EMI)

EMI is focused on conducted and radiated signals that escape from the electronics circuitry where they can interfere with other circuits. For example, EMI in the 100MHz range might create noise in an FM radio, while 2.4GHz EMI might interfere with cell phone or Wi-Fi performance.

The EMI Engineer also has specific goals, and this (non-exhaustive) list identifies some of the most common:

- Unbroken Return Paths
- Tightly Sealed Enclosure
- Minimum Coupling
- No High Q **Impedance** Peaks



PICOTEST

The Common Denominator

They interact, whether we like it or not

There is a common thread connecting them…

Impedance

Courtesy, Eric Bogatin, Signal Integrity Journal
http://www.signalintegrityjournal.com

PICOTEST

Contrary to Popular Belief

- These interactions are NOT limited to high frequency or high power
- Impedance isn't the ONLY issue

Let's look at just a few examples…

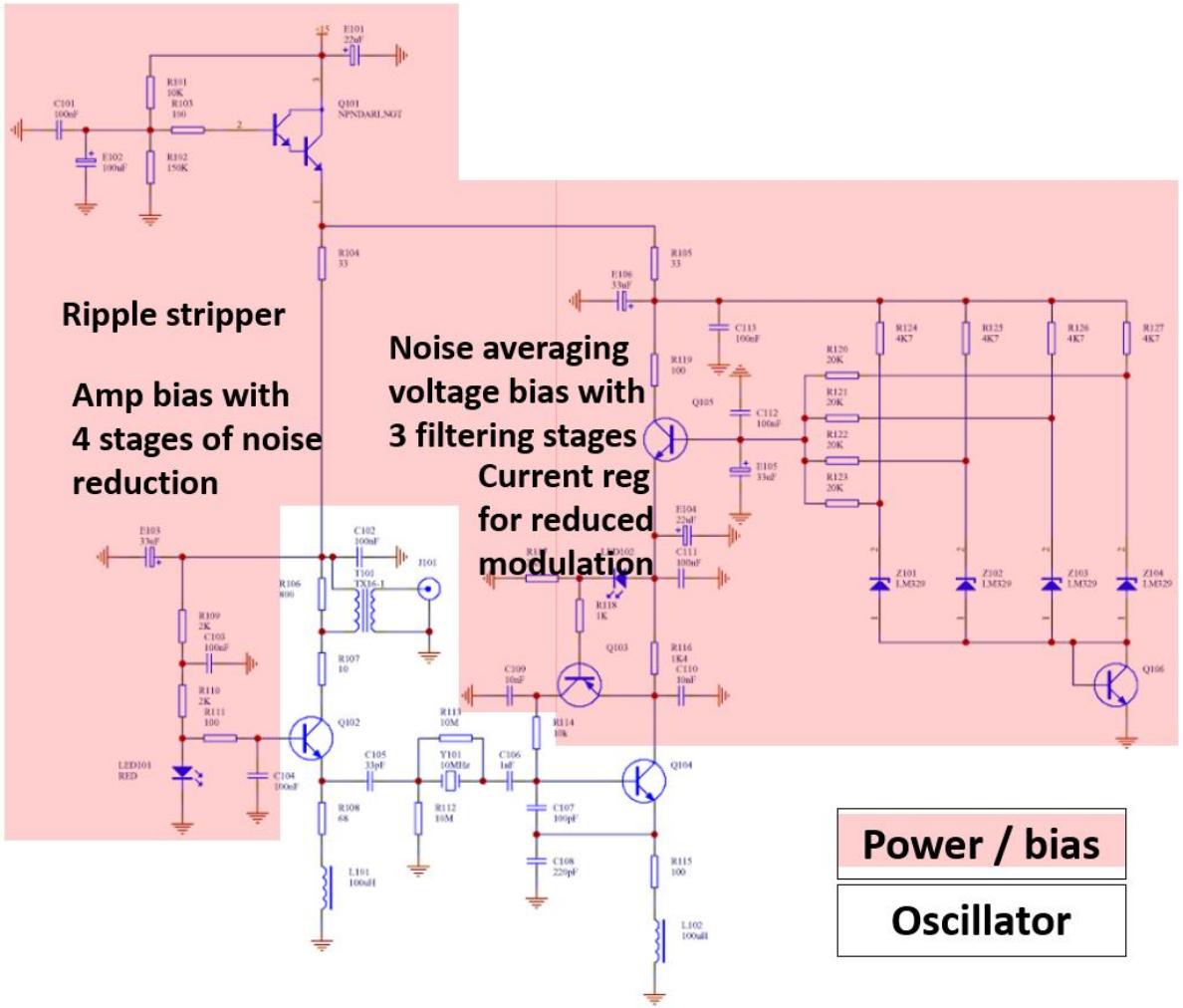
PE -> SI

It seems oscillator designers have known about the interaction between the power supply and the oscillator for ages

As this example shows, there is a lot more power supply circuitry in the oscillator than oscillator circuitry

Master oscillator designer, Charles Wenzel, knew this well and was constantly looking for better methods of reducing power supply noise

Power supply noise is one of the dominant sources of jitter in SI systems and generally this is included in power-aware SI simulation

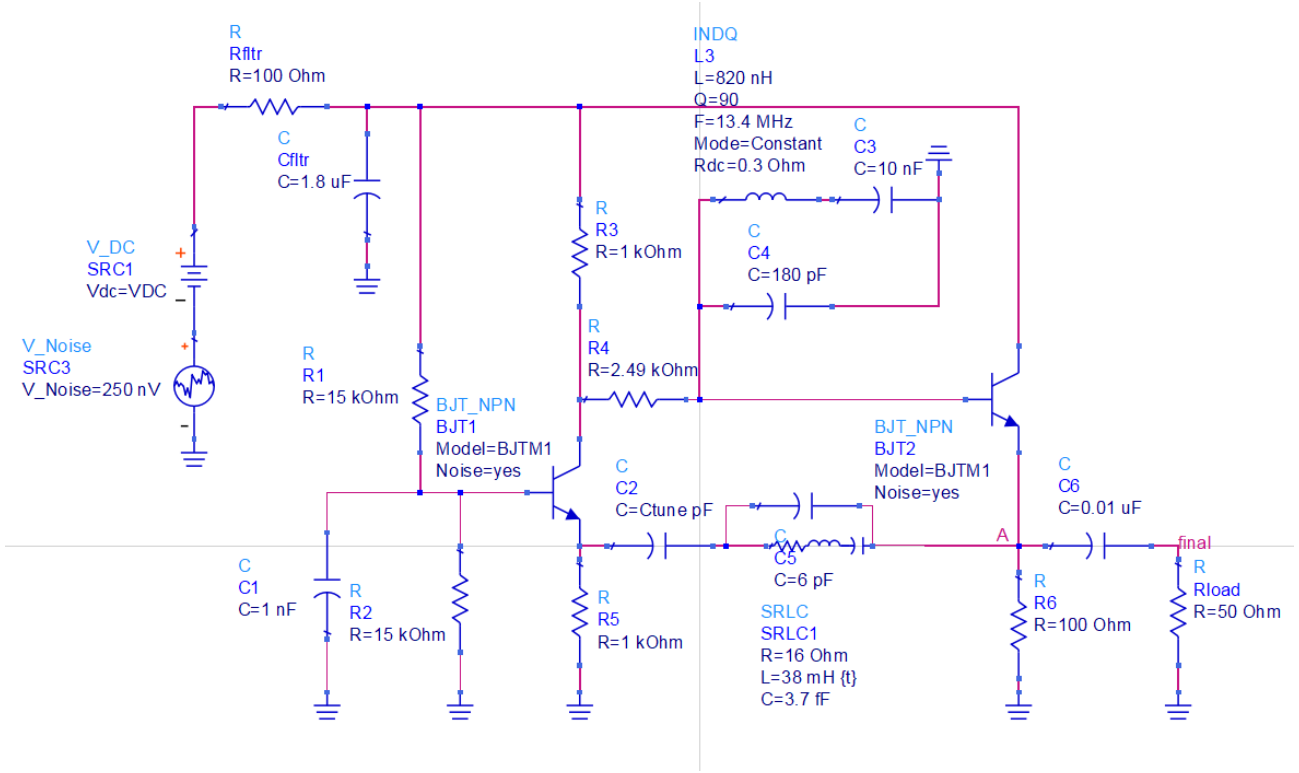


Courtesy http://www.ko4bb.com/~bruce/CrystalOscillators.html

PICOTEST

Power-Aware Simulation / Filter Design

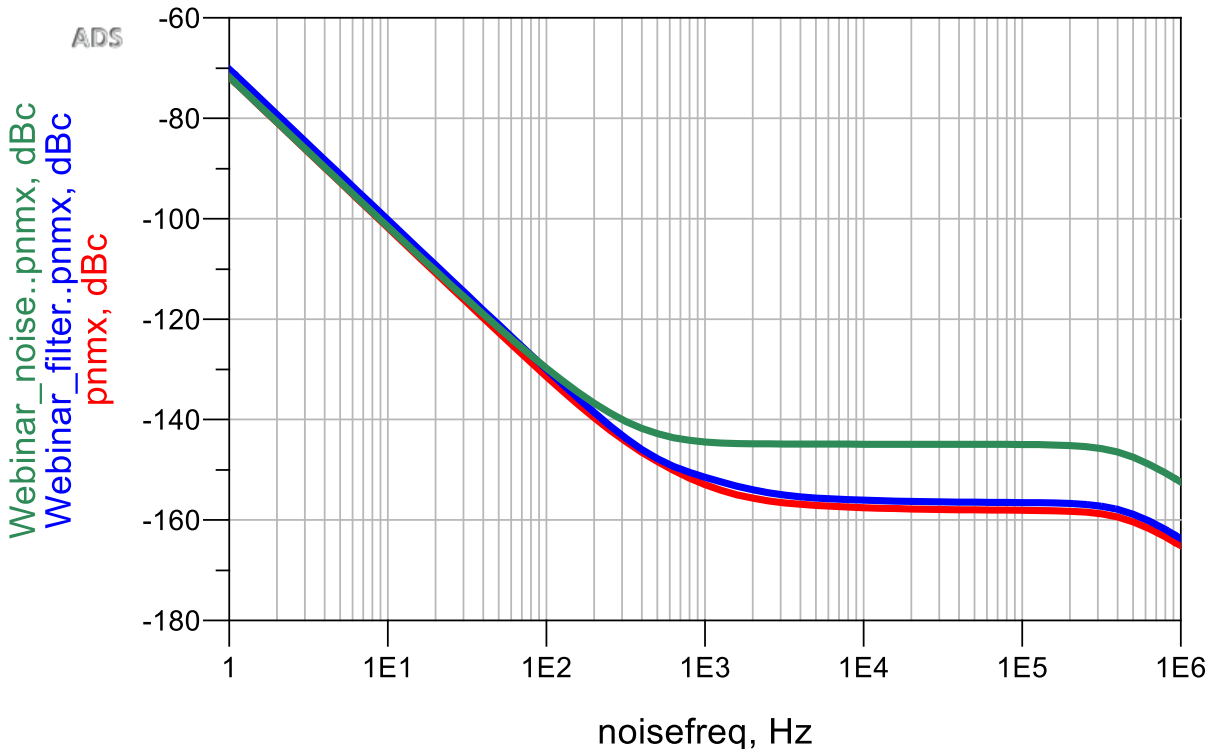
Phase noise is somewhat dependent on the **impedance** of the loaded crystal resonant Q



Phase noise without power supply noise

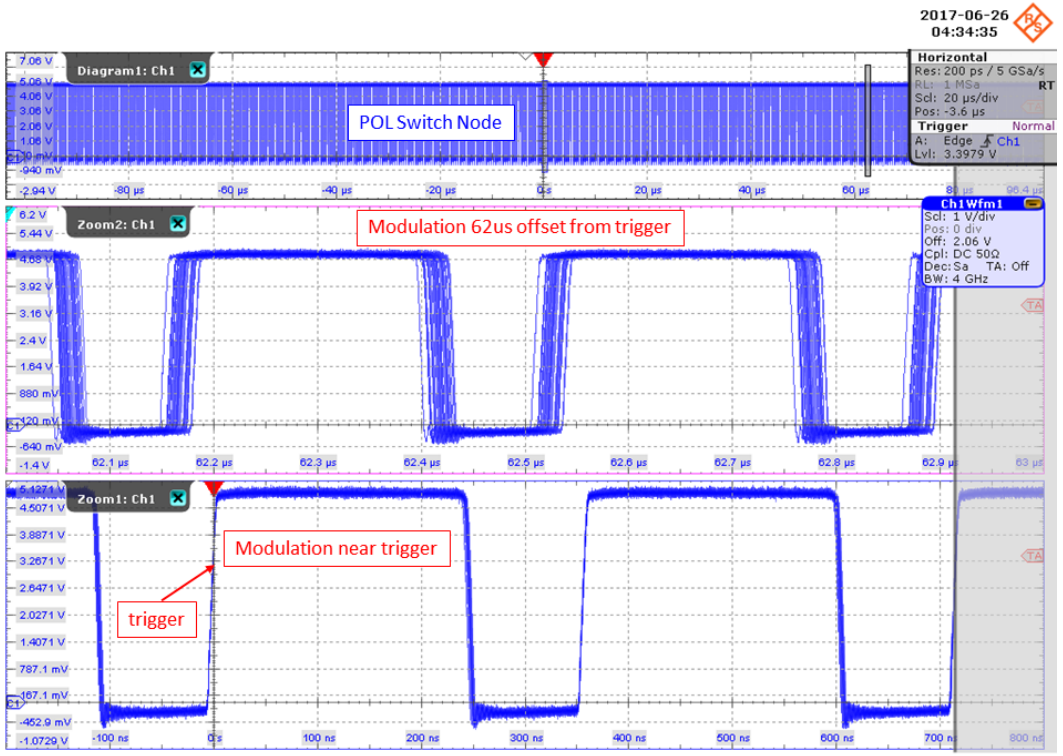
Phase noise with power supply noise

Phase noise with power supply noise and filter



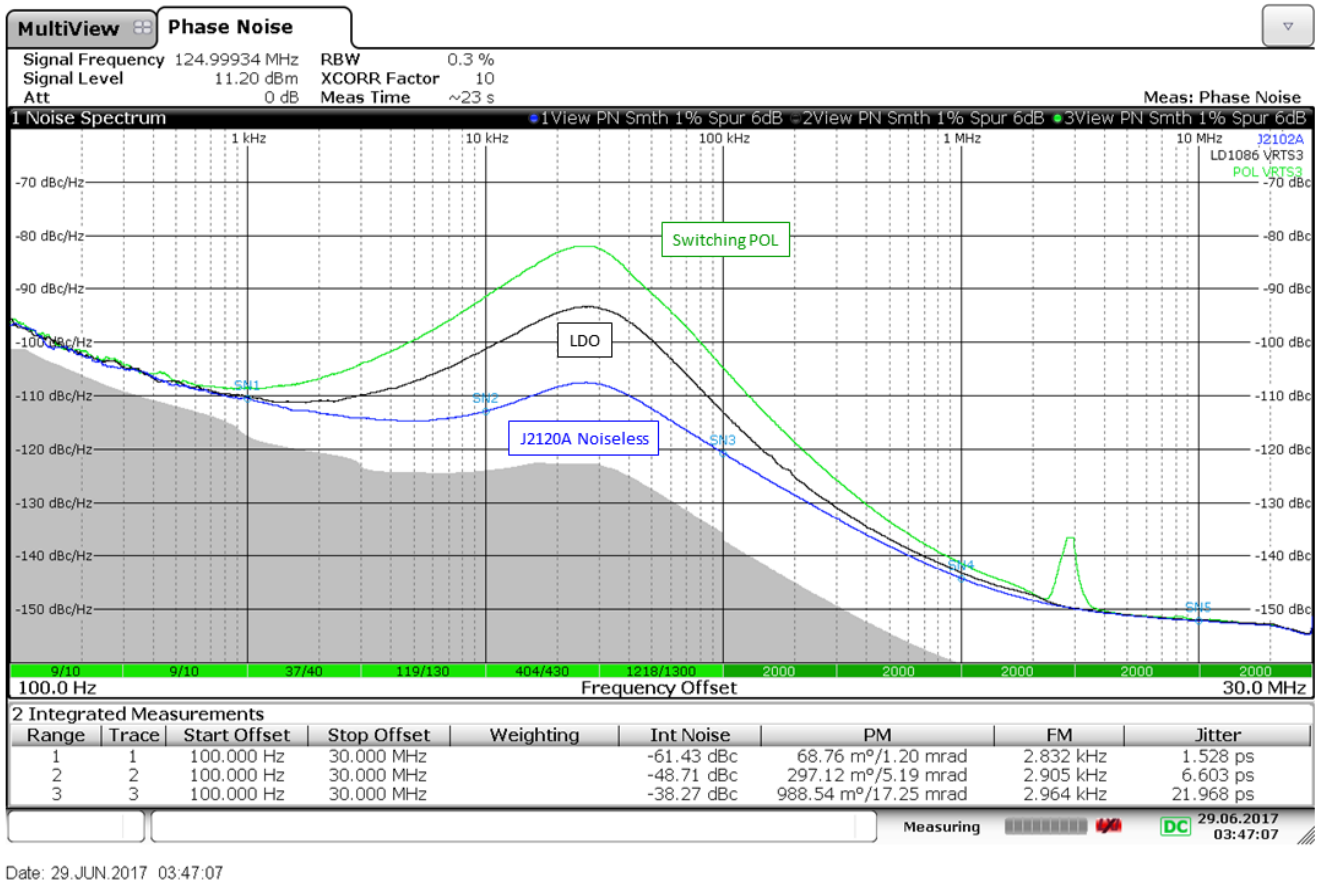
PICOTEST

PE -> SI



Many switching power supplies use less than stellar oscillator circuits, resulting in switching frequency jitter

The switching frequency jitter results in power supply noise, which in-turn results in oscillator jitter - **Jitter-Induced Jitter**



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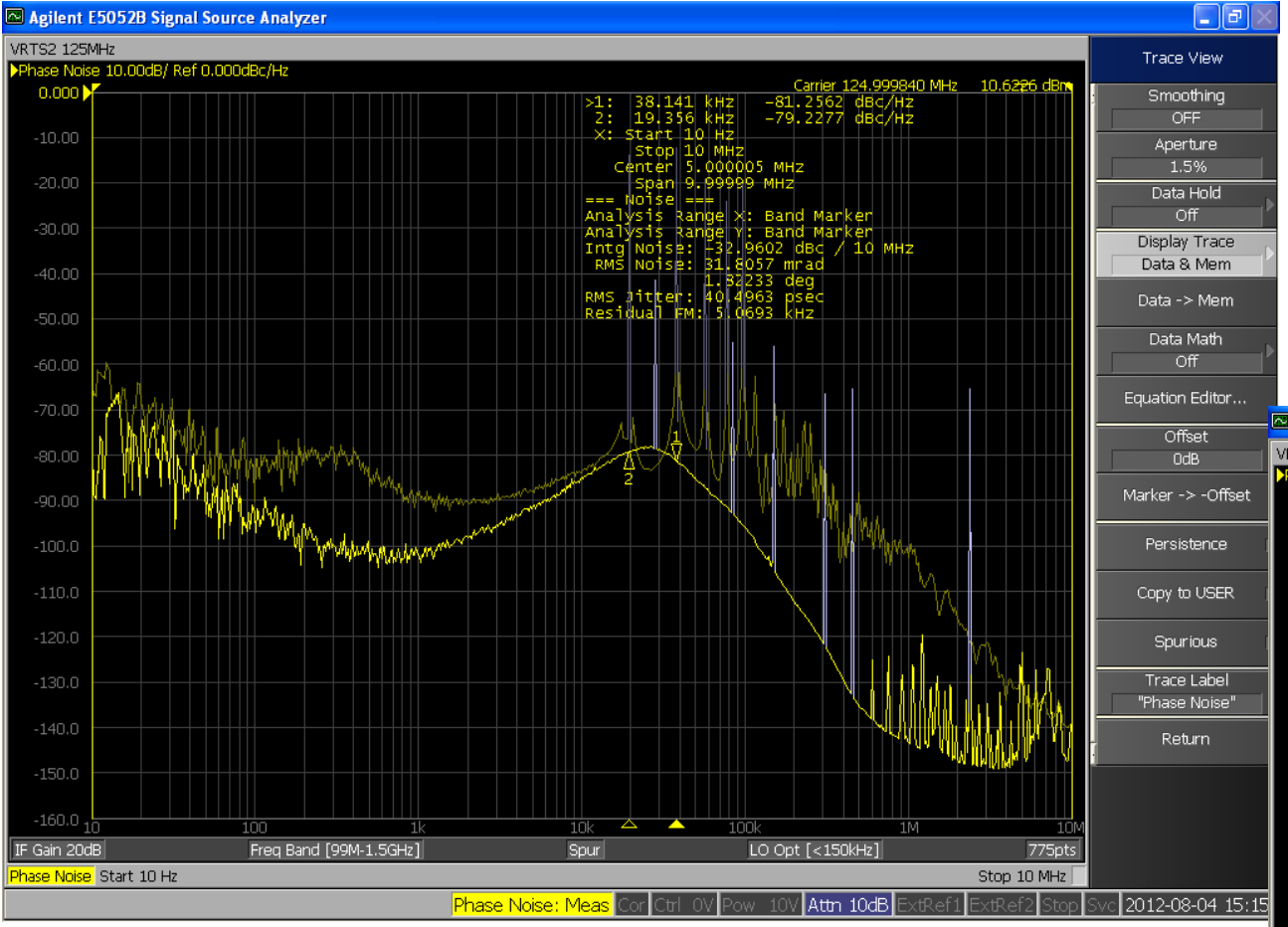
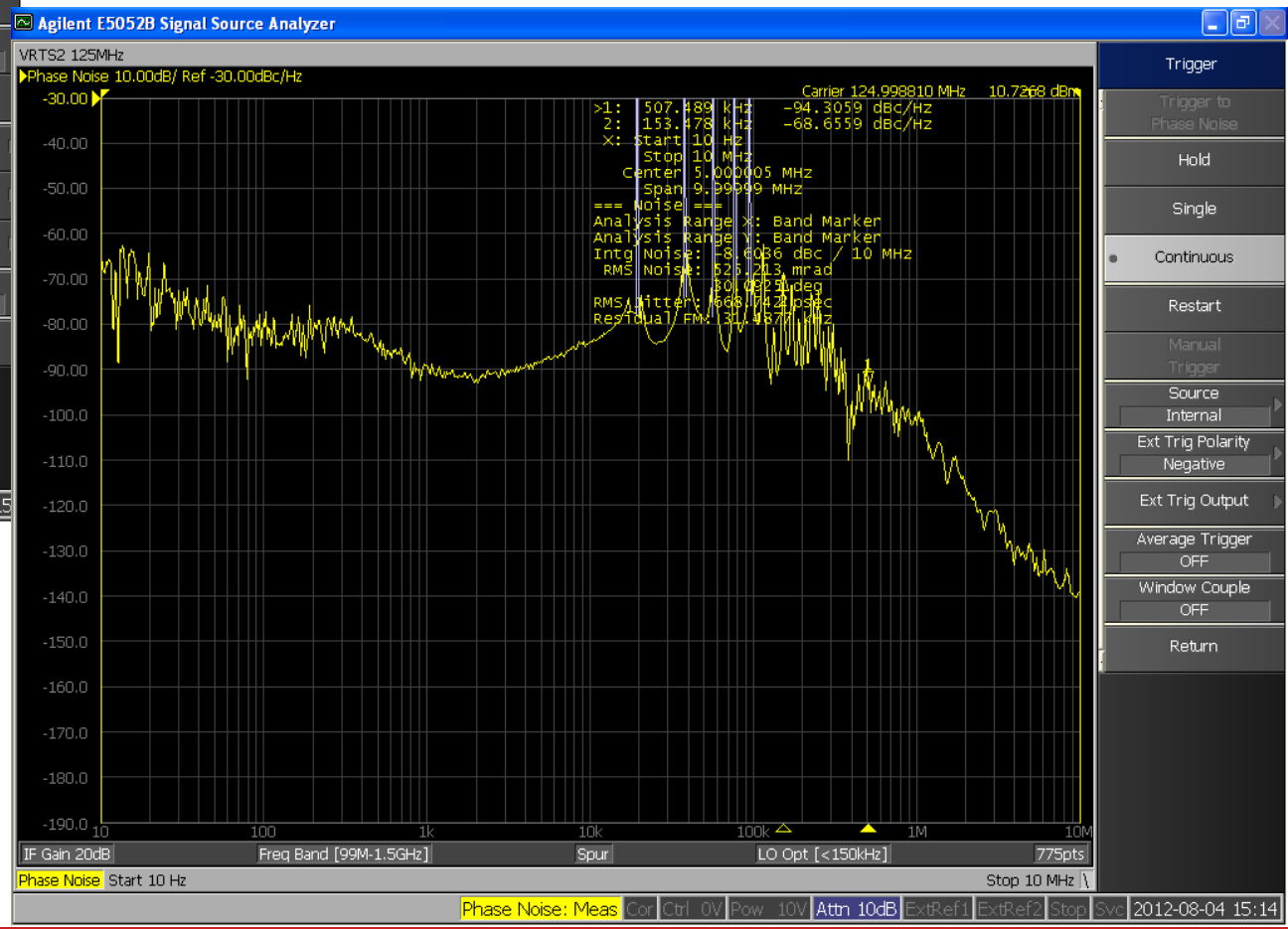


Circuits like Burst, Chirp, or PFM mode are often implemented in POL switching regulators when they operate at low power. This improves efficiency

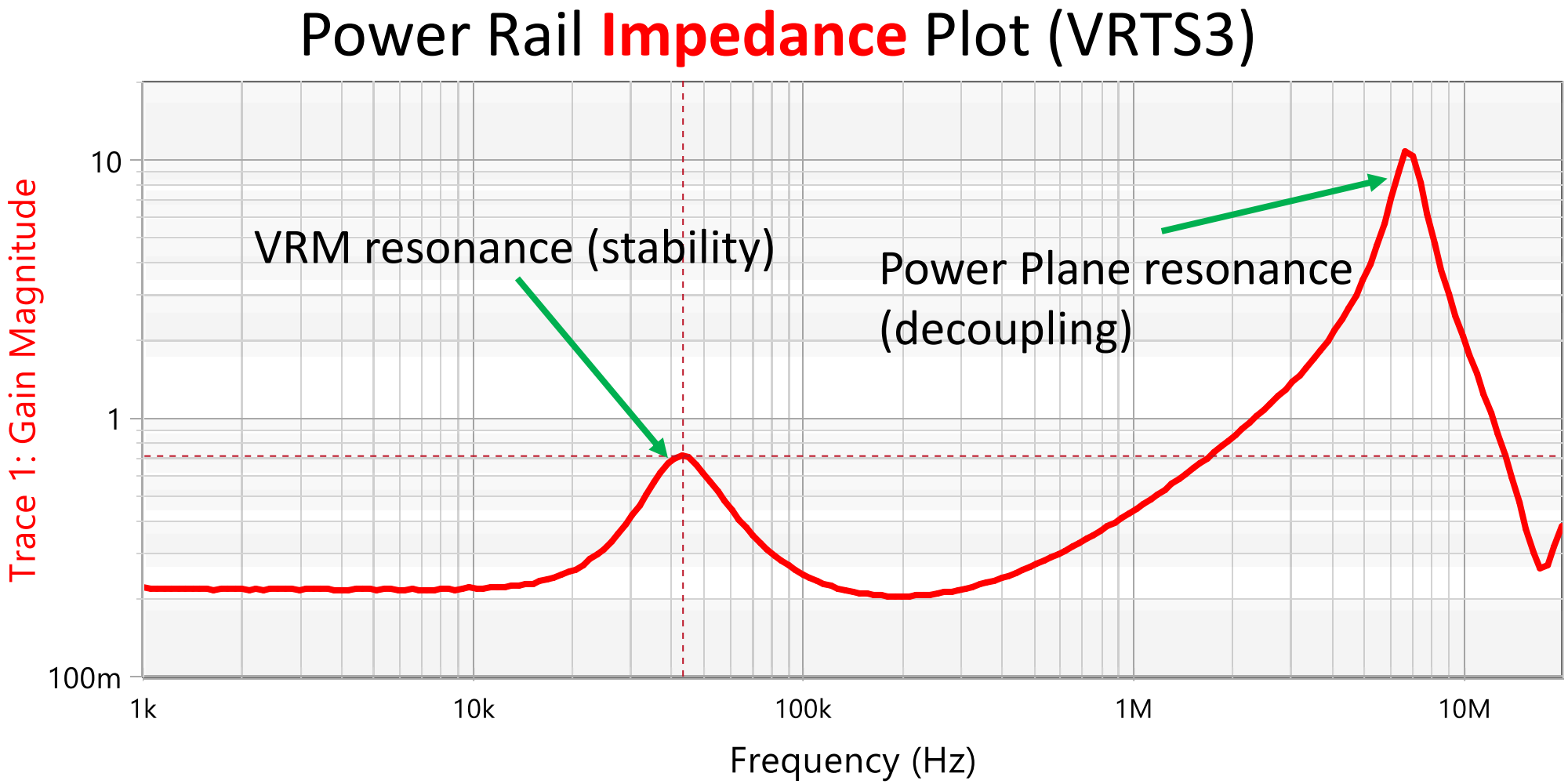


Of course, this destroys SI performance by generating noise in the reference clocks and the PLLs

But that's the SI guy's problem, right?

PICOTEST

Power Rail Resonances Result in SI Too



PICOTEST

PI -> PE -> SI

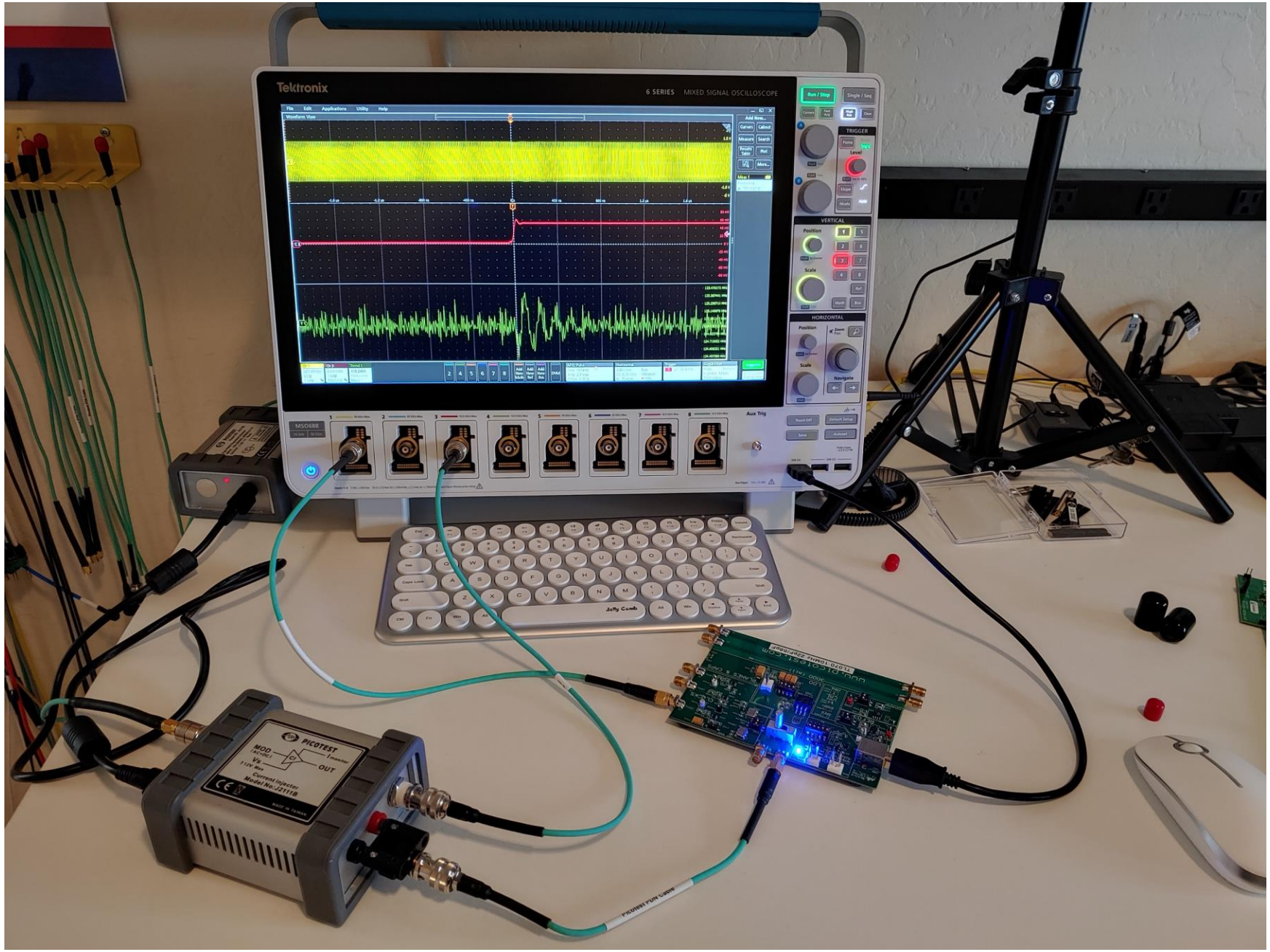
Those PE and PI resonances get excited by the dynamic operation of the system and interact (in a bad way)

In this picture, the upper YELLOW trace is a 125MHz reference clock

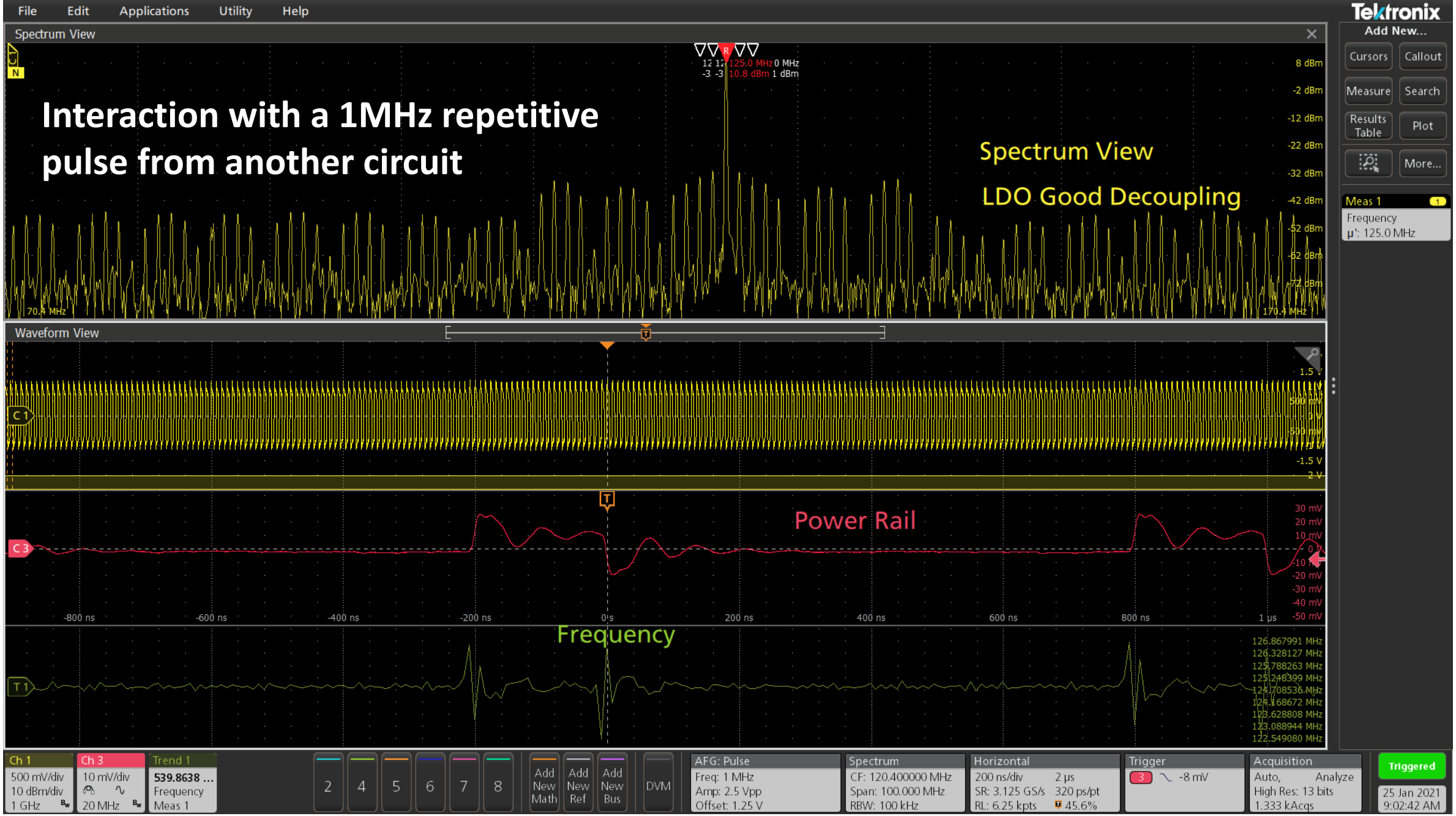
The PINK trace is a load demand, such as a transceiver being enabled

The lower GREEN trace is the frequency vs. time display of the 125MHz reference clock

The ringing is the response of the 7MHz resonant **impedance** peak



PICOTEST



PICOTEST

SI -> PI

Interactions occur in the opposite direction just as easily

The same power plane can be excited to create a Rogue Wave, or an extreme voltage variation, typically at a high-speed device

Here the digital signal pattern is created in a unique way, to excite both the VRM **impedance** resonance and the 7MHz power plane resonance

The combination results in a 70mVpp noise signal. This noise is much larger than what would be allowed for a 1.2V power rail or a PLL

PICOTEST

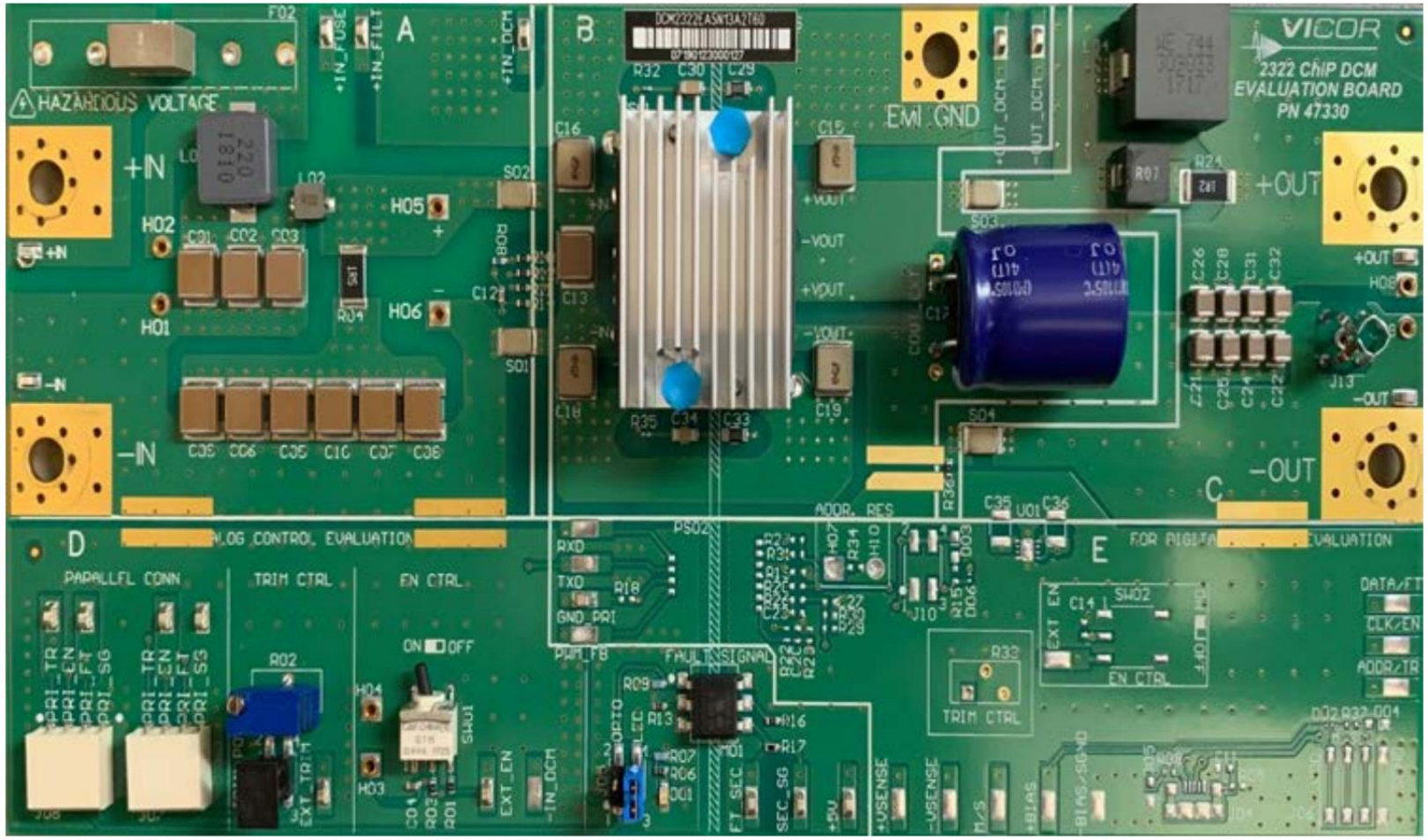
Challenge: Encapsulated Vicor Module

Determine:

- Inductance and turns ratio of the power transformer
- Mode of Operation

Rules:

- No probe can contact the module or copper on the printed circuit board
- Cannot x-ray the module



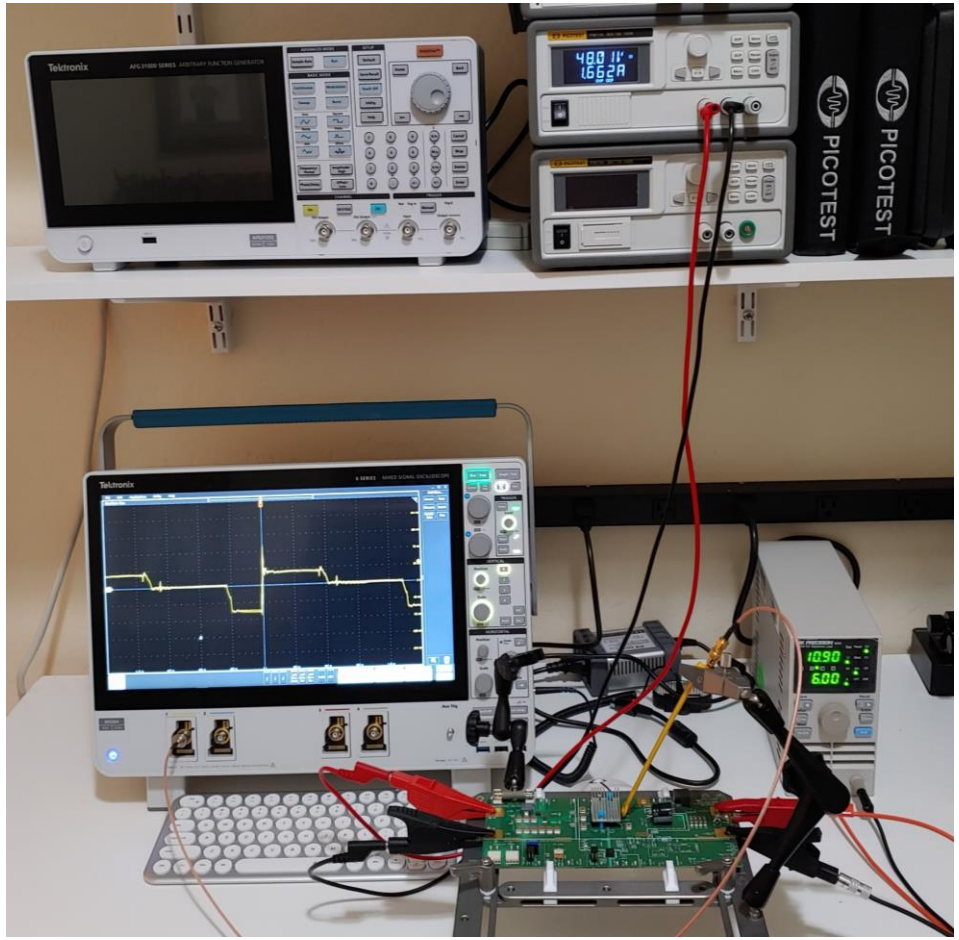
PICOTEST

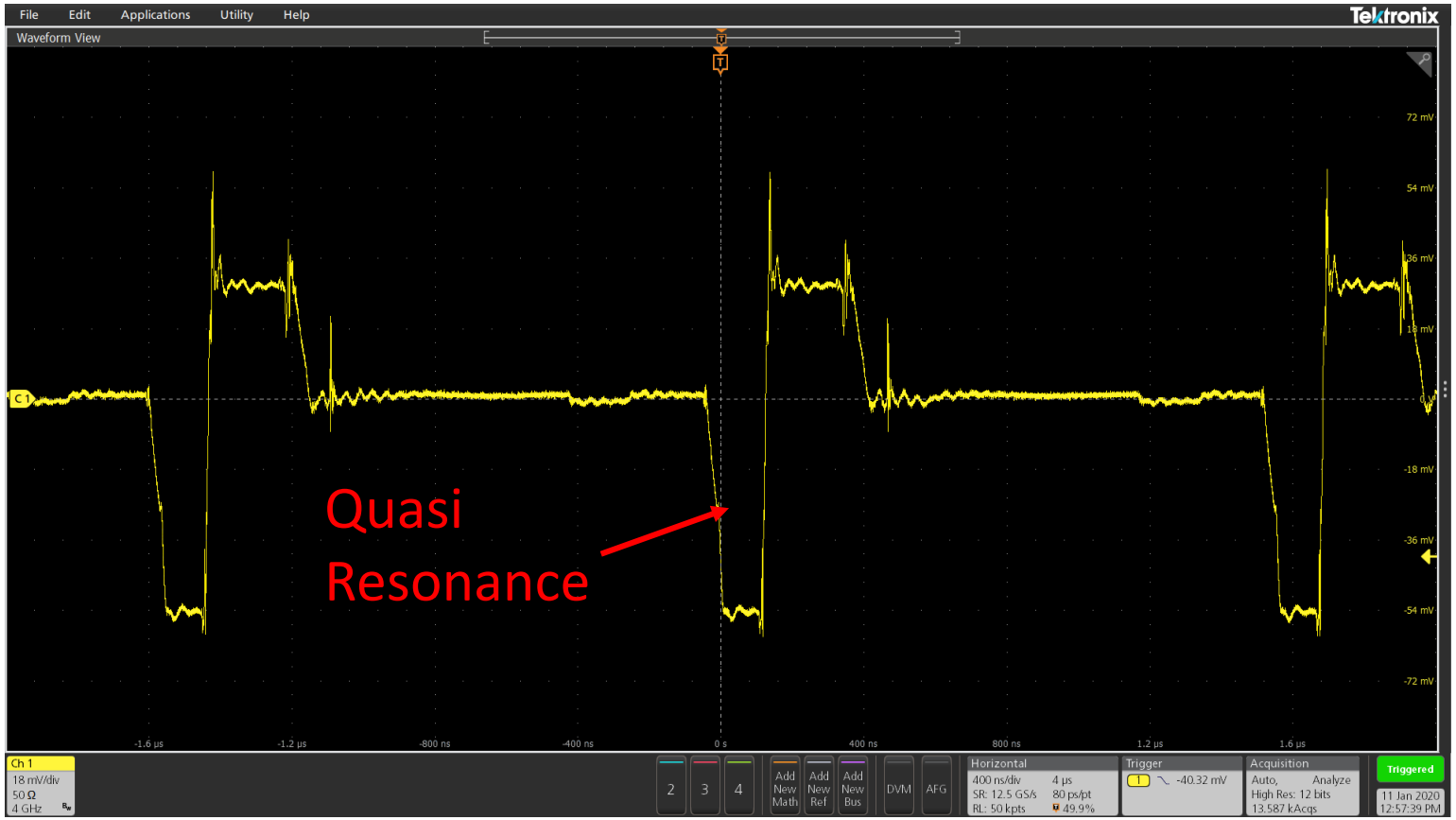
PE -> EMI

η_0 = **Impedance** of Free Space (377Ω)

$$|\mathbf{E}|_{max} \approx \begin{cases} \frac{V\Delta s\beta^2}{4\pi r} & Z_{LOOP} > \eta_0 \\ \frac{V\Delta s\beta^2}{4\pi r}\left(\frac{\eta_0}{Z_{LOOP}}\right) & Z_{LOOP} < \eta_0 \end{cases}$$

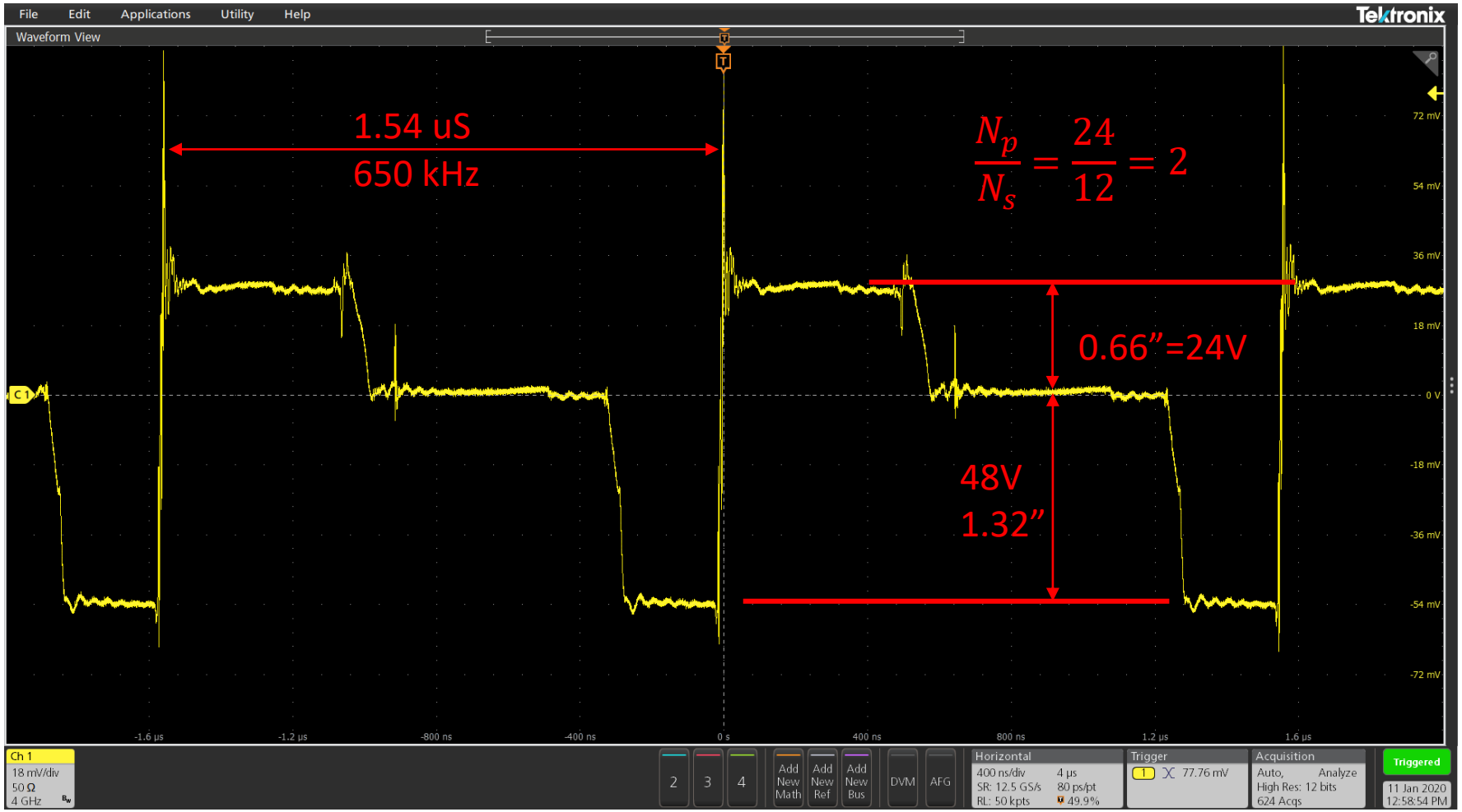
https://learnemc.com/electromagnetic-radiation





PICOTEST

Transformer Turns Ratio



$$Pin = \frac{1}{2} \cdot Lpri \cdot Ipk^2 \cdot Fsw$$

$$Ipk = \frac{Vin}{Lpri} \cdot Ton$$

Substituting

$$Pin = \frac{Fsw \cdot Ton^2 \cdot Vin^2}{2 \cdot Lpri}$$

And solving for Lpri

$$Lpri = \frac{Fsw \cdot Ton^2 \cdot Vin^2}{2 \cdot Pin}$$

Plugging in values

$$Fsw := 640 \cdot 10^3$$

$$Ton := 200 \cdot 10^{-9}$$

$$Vin := 48$$

$$Pin := 12$$

$$Lpri := \frac{Fsw \cdot Ton^2 \cdot Vin^2}{2 \cdot Pin} = 2.458 \times 10^{-6}$$

$$Ipk := \frac{Vin}{Lpri} \cdot Ton = 3.906$$

$$Pin := \frac{1}{2} \cdot Lpri \cdot Ipk^2 \cdot Fsw = 12$$

TEMPEST

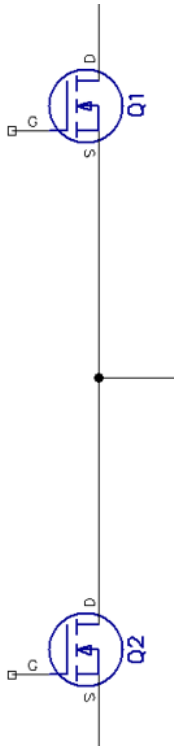
In the 1950's it was observed that the emanation of EMI allowed signals to be captured and decoded

TEMPEST (Telecommunications Electronics Materials Protected from Emanating Spurious Transmissions) rules were developed and implemented to minimize the ability to decode signals, which were transmitted through many mediums. For example, audio signals, ocean waves, and RF currents in the skins of aircraft and submarines all transmitted data, which could be decoded

https://en.wikipedia.org/wiki/Tempest_(codename)

Simplified Step-Down

Totem-Pole Half Bridge

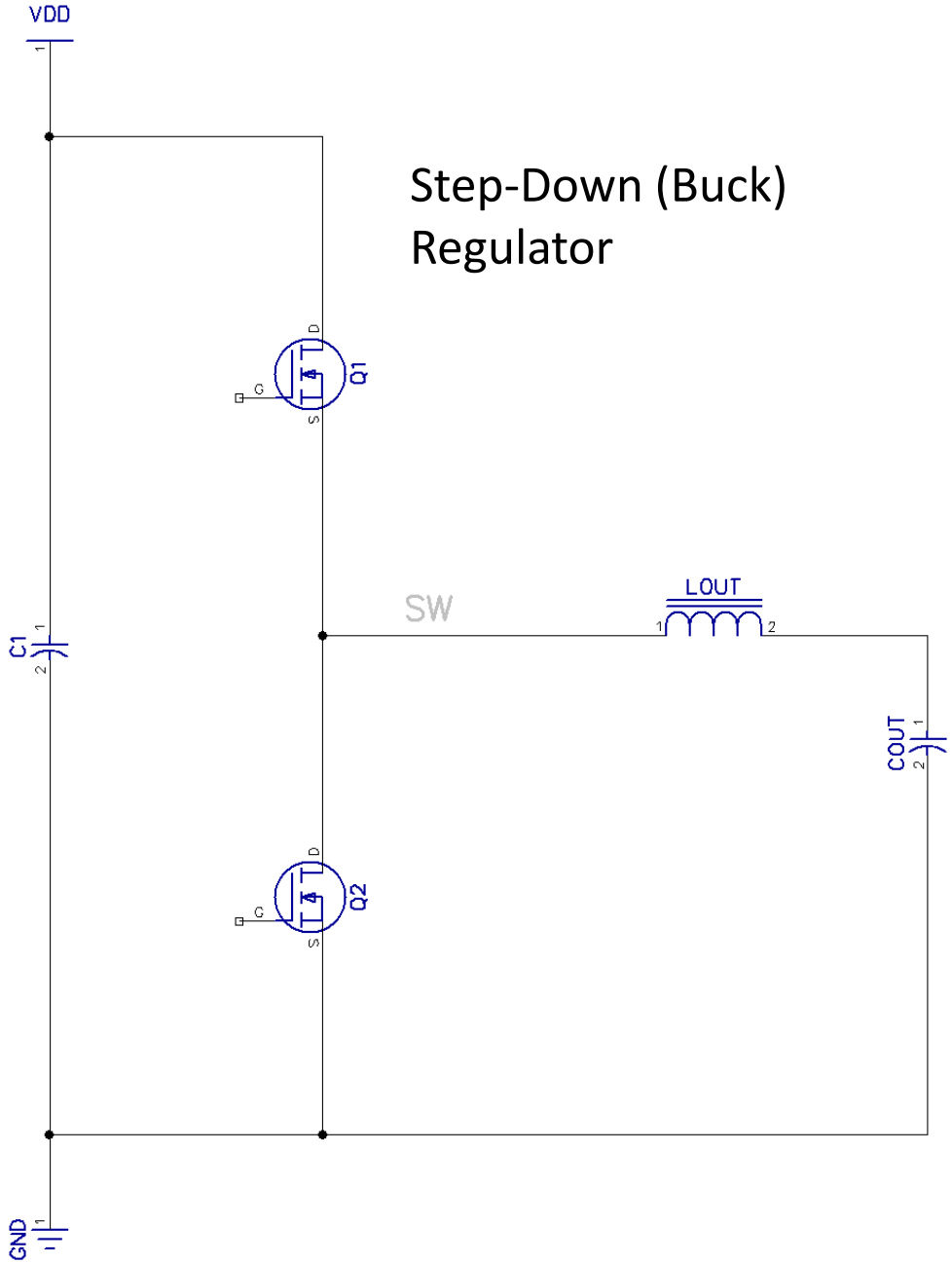


The half bridge (or totem pole) is a very common circuit. It's the output stage of logic gates

This is also the power circuit for the common step-down converter and also for the half-bridge and full bridge power converter

There are other topologies for sure, but this one is simple to understand and once you understand it, you can easily understand the others

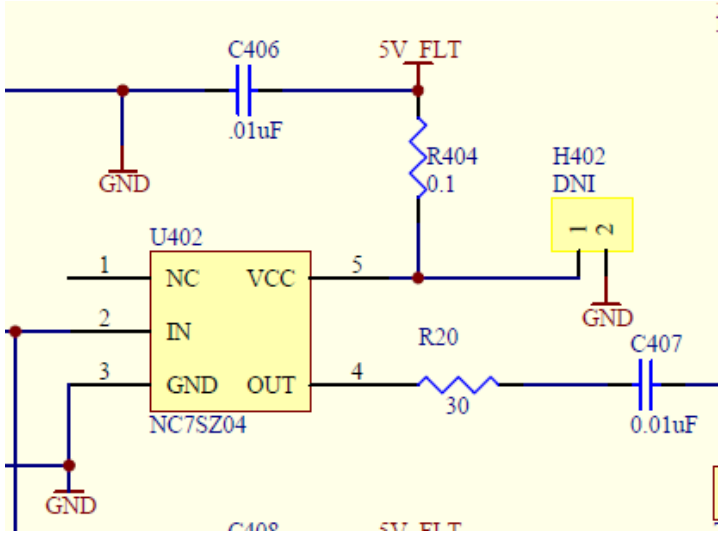
Step-Down (Buck) Regulator

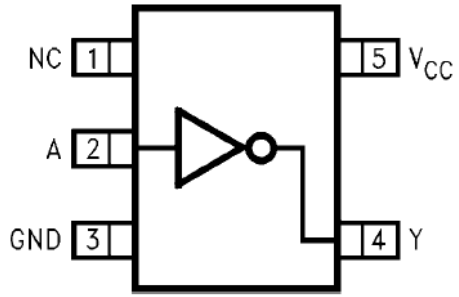


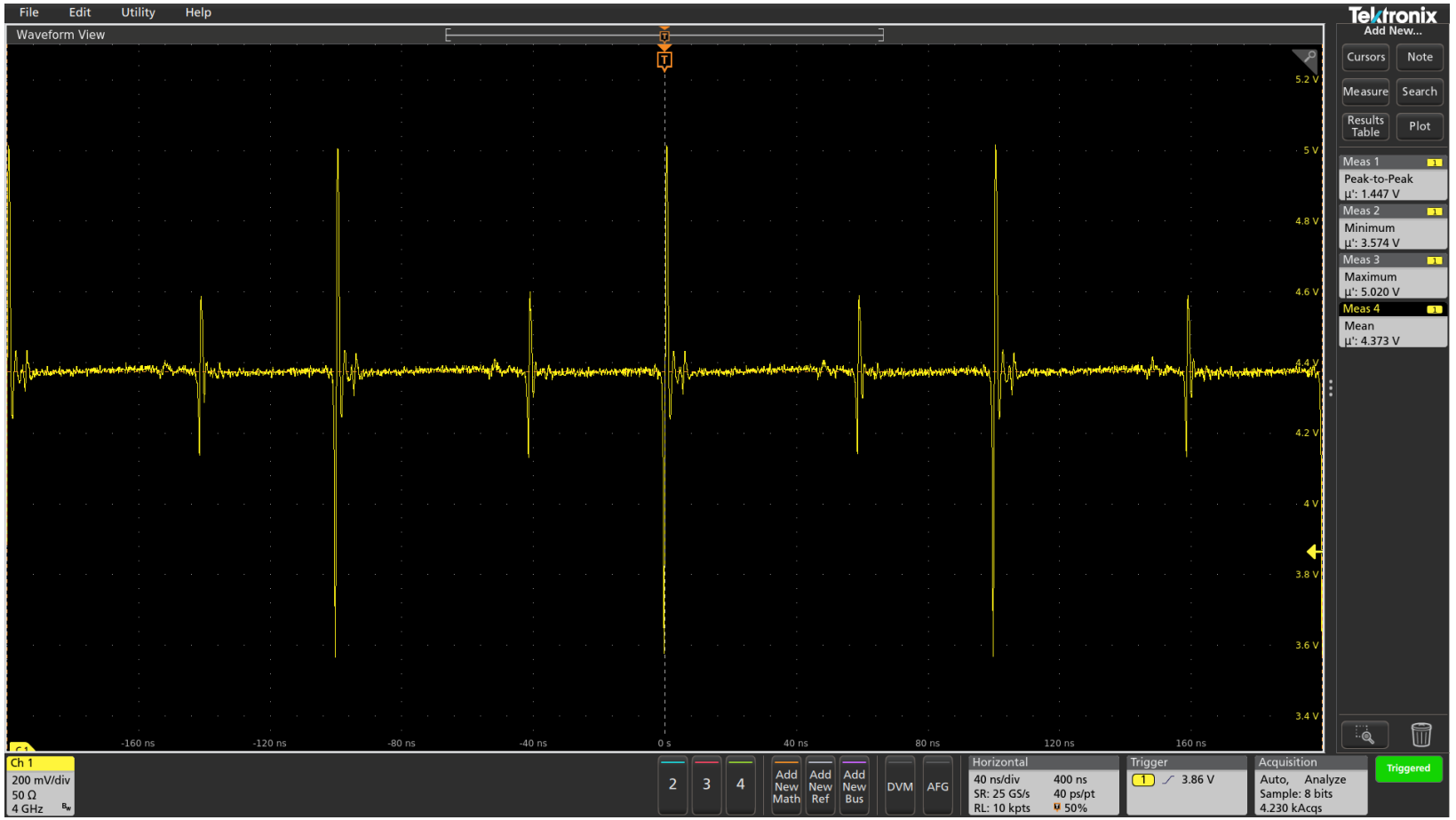
PICOTEST

SI -> PI

CMOS Logic Gate – NO LOADING AT ALL, yet generates almost 1.5Vpp transient. Due to the interaction between the source **impedance** and the MOSFET Coss **impedance**

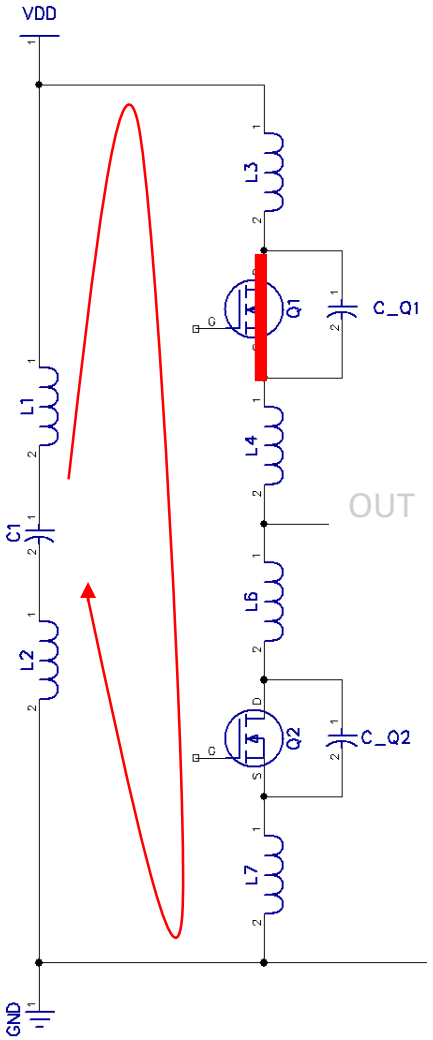






PICOTEST

Simplified Circuit – Parasitic Impedance Added



The input Vcc decoupling capacitor, C1, is shown along with the interconnect inductance between the chip and the cap (not the placement of the pins)

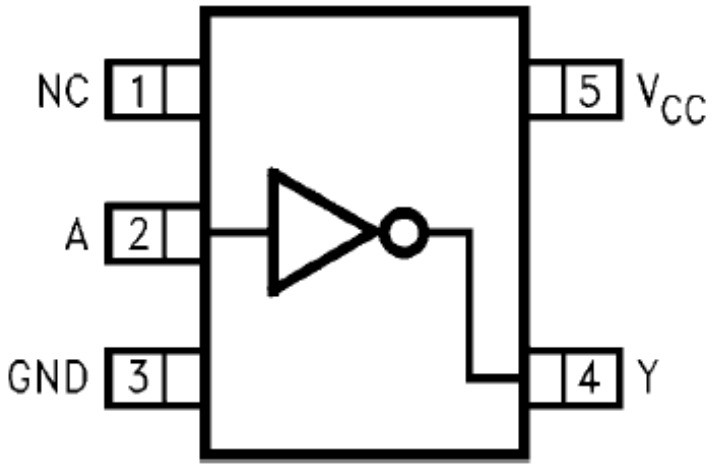
L3, L4, L6, and L7 are the PCB and the bond wires, while C_Q1 and C_Q2 are the internal MOSFET COSS terms. There is an additional capacitor that is the output trace or plane connected to the OUT pin

When the top MOSFET, Q1, turns on, the inductive parasitic elements resonate with the Coss of the lower MOSFET (C_Q2)

This results in a resonant current (ringing) or a SINC waveform, depending on the damping provided by the MOSFET resistance and the PCB losses

A Better Model

How to decouple??



There are 3 types of responses from this circuit

$$I_{instantaneous} = C \cdot \frac{dV}{dt}$$ **This is an impulse with finite dV/dt**

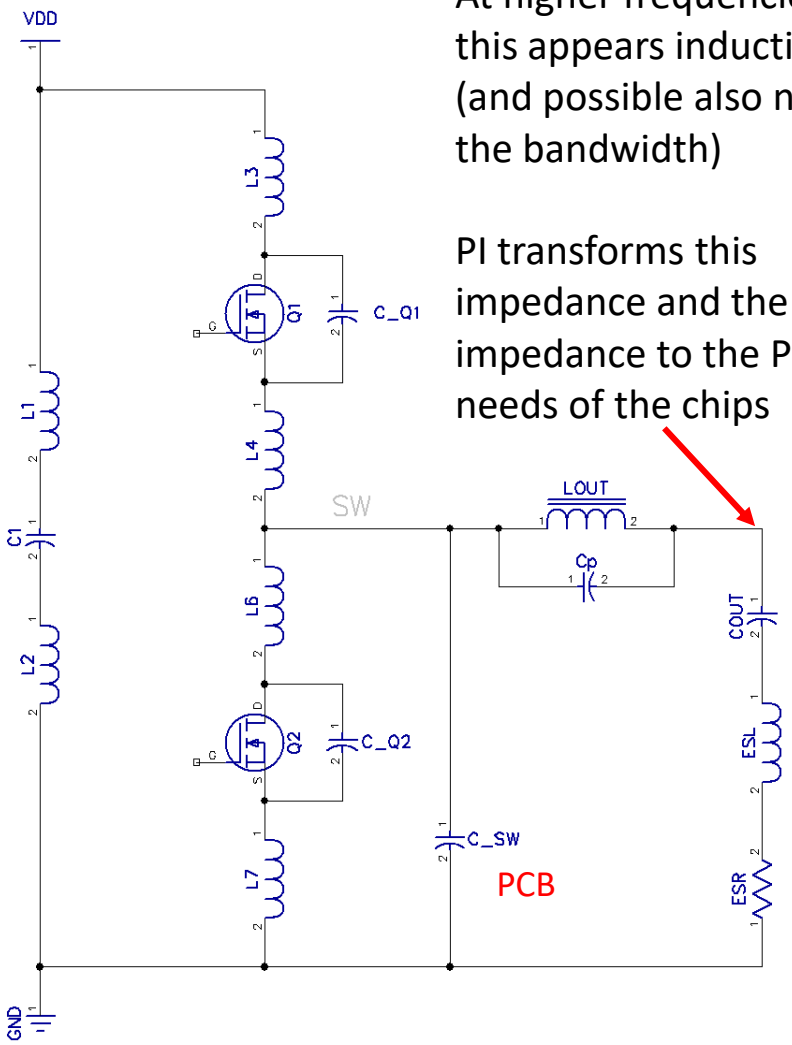
$$I_{average} = C \cdot V \cdot Fsw$$ **This is the average over the repetition**

$$I_{resonant} \cong \frac{V}{Z_o} = V \cdot \sqrt{\frac{C}{L}}$$ **This causes the ringing**

Our logic gate example had a very fast dV/dt (5V/300ps) and low repetition rate. The instantaneous impulse current is very high, while the average current is near zero

The poor placement of the Vcc and GND pins results in high inductance for L1 and L2

Extending it to a VRM

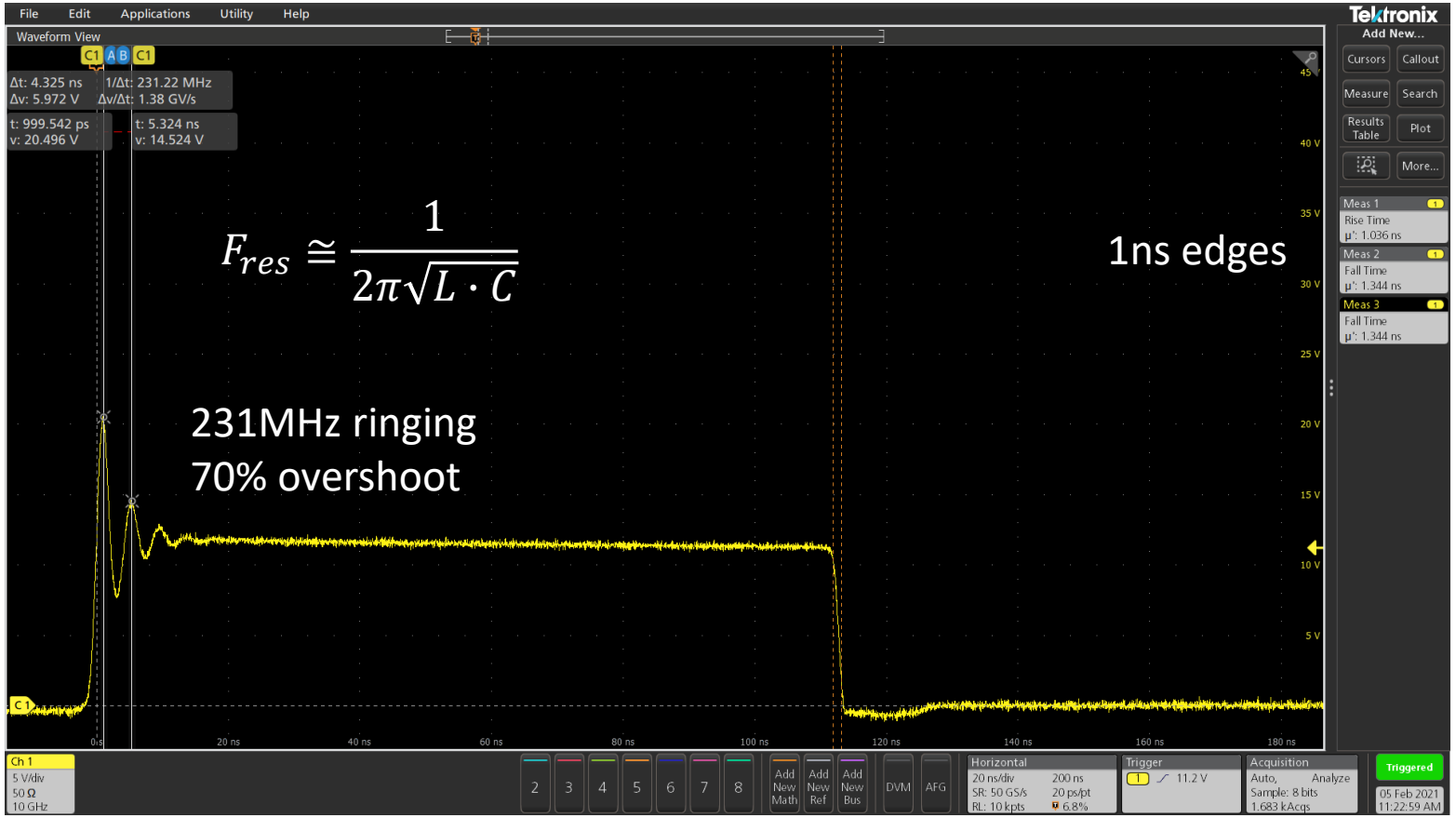


At higher frequencies this appears inductive (and possible also near the bandwidth)

PI transforms this impedance and the PCB impedance to the PI needs of the chips

Note there are THREE capacitance contributors: MOSFET, PCB and Inductor

230MHz will appear in the EMI



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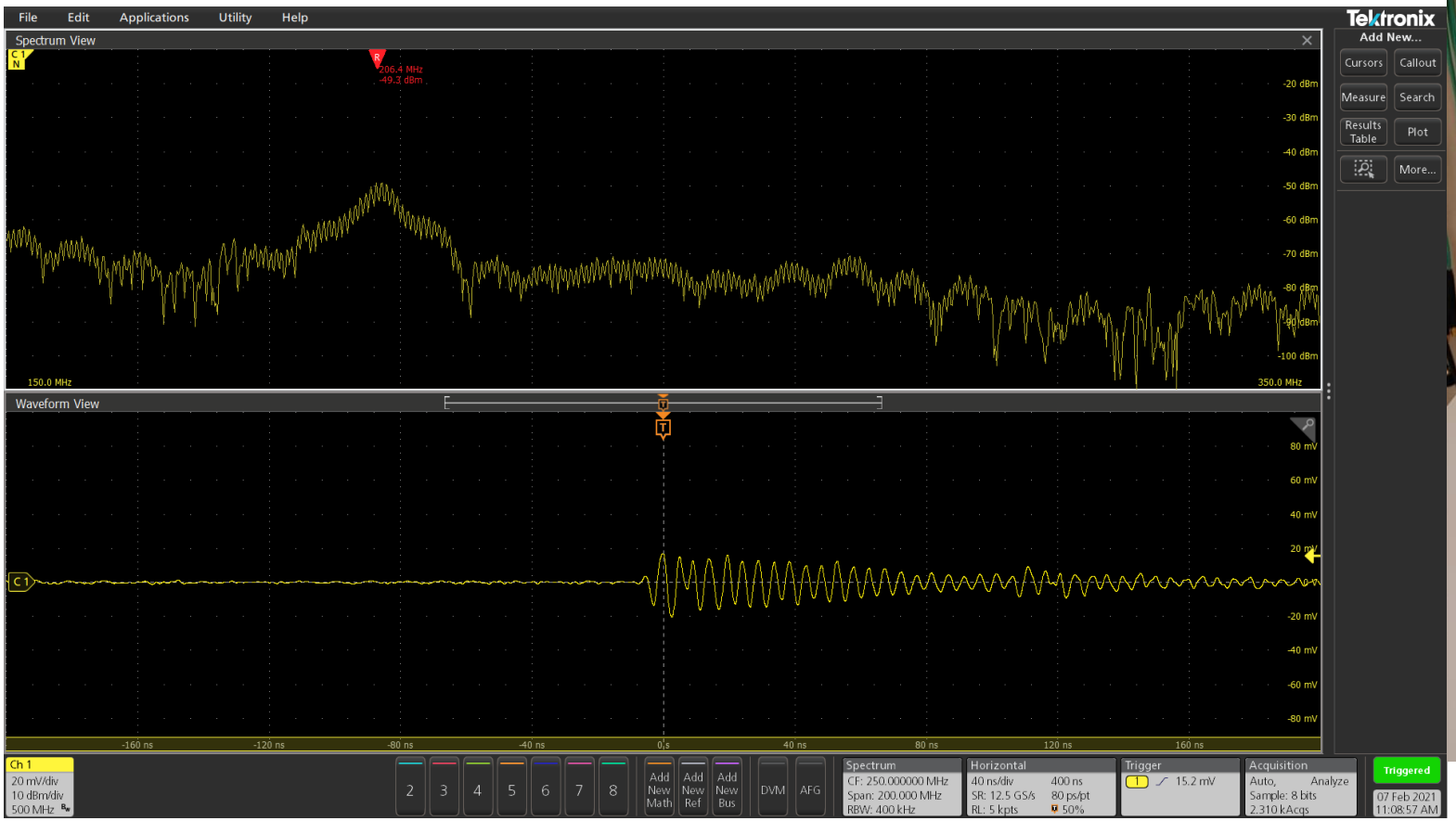
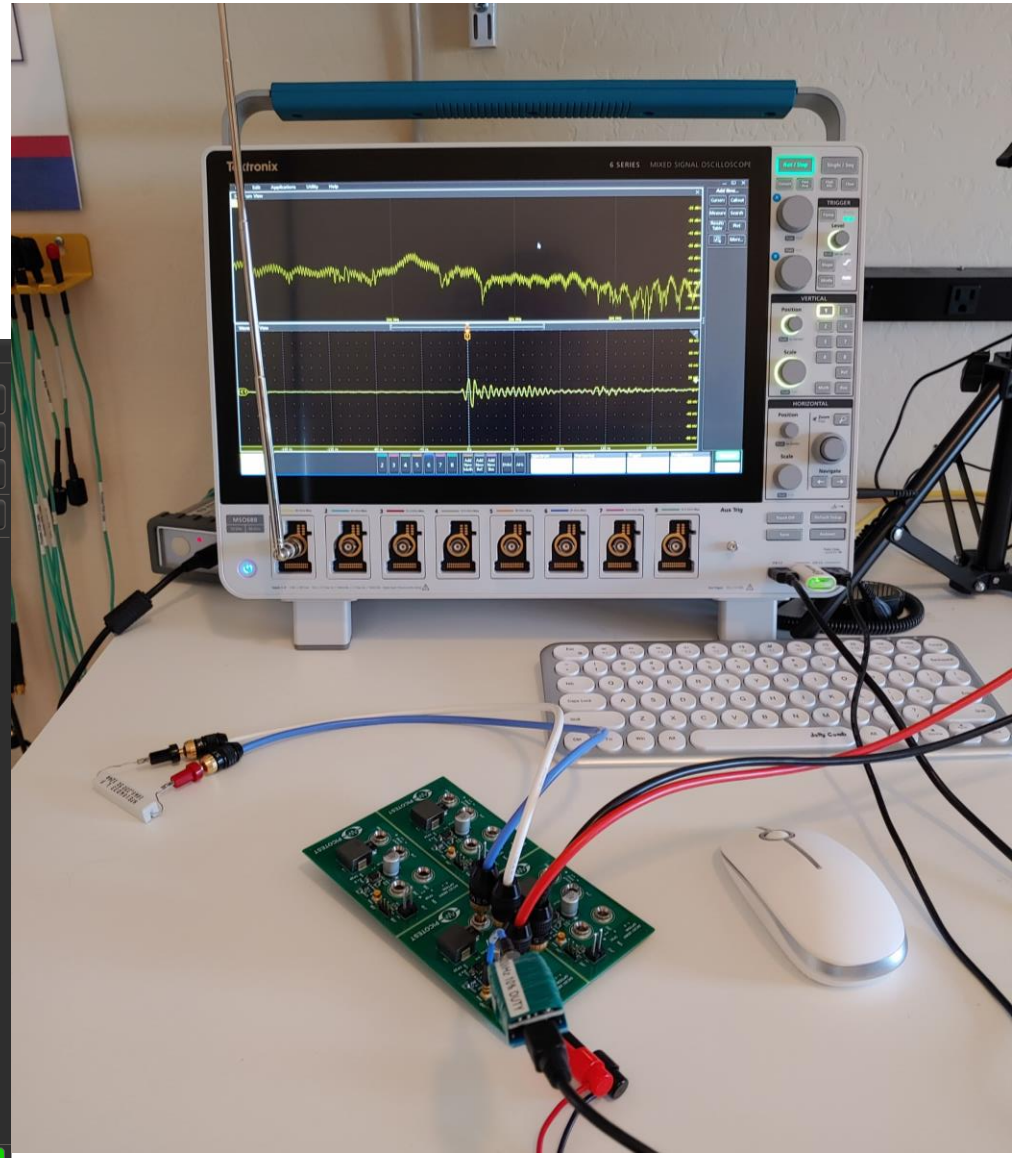
YEP, EMI

Impedance -> Ringing -> EMI





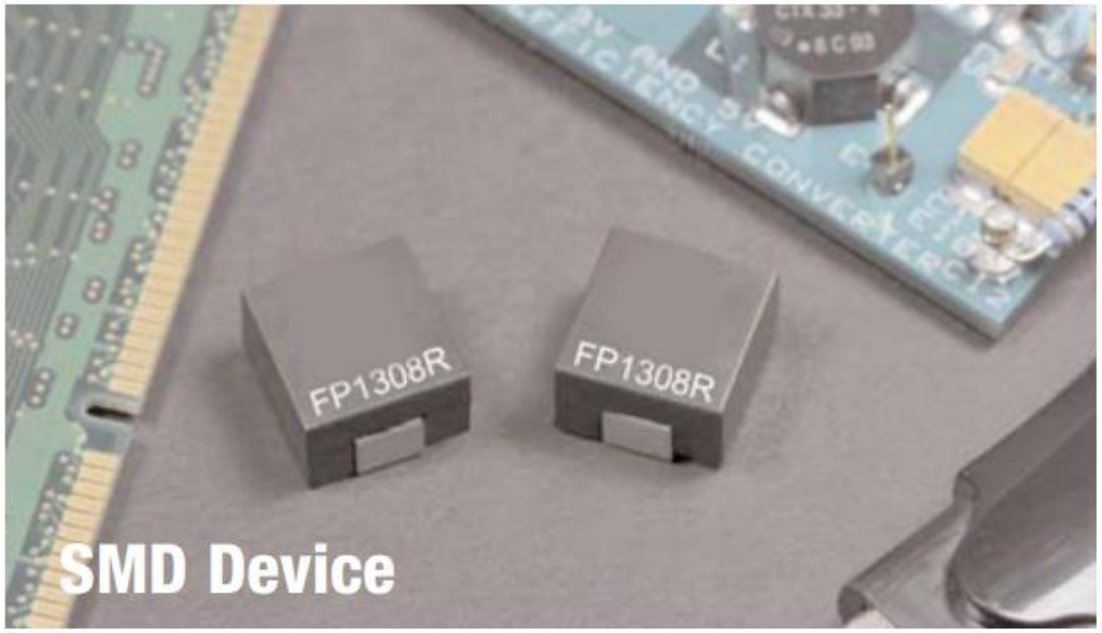
PICOTEST

Inductor

Inductors are often poorly specified. Neither SRF or parallel parasitic capacitance are specified

Inductive **Impedance**

Product Specifications							
Part Number[7]	OCL[1] ± 10% (nH)	FLL[2] (nH)	I_{rms}[3] (Amps)	I_{sat}1[4] @ 25°C (Amps)	I_{sat}2[5] @ 125°C (Amps)	DCR (mΩ) @ 20°C	K-factor[6]
R1 Version							
FP1308R1-R11-R	110	79	57	120	105	0.32 ± 9.4%	233
FP1308R1-R21-R	210	152		80	68		233
FP1308R1-R26-R	260	187		64	52		233
FP1308R1-R32-R	320	230		52	40		233
FP1308R1-R44-R	440	317		37	28		233
R2 Version							
FP1308R2-R11-R	110	79	45	120	105	0.53 ± 10%	233
FP1308R2-R21-R	210	152		80	68		233
FP1308R2-R26-R	260	187		64	52		233
FP1308R2-R32-R	320	230		52	40		233
FP1308R2-R44-R	440	317		37	28		233
R3 Version							
FP1308R3-R11-R	110	79	68	120	105	0.18 ± 20%	233
FP1308R3-R21-R	210	152		80	68		233
FP1308R3-R26-R	260	187		64	52		233
FP1308R3-R32-R	320	230		52	40		233
FP1308R3-R44-R	440	317		37	28		233

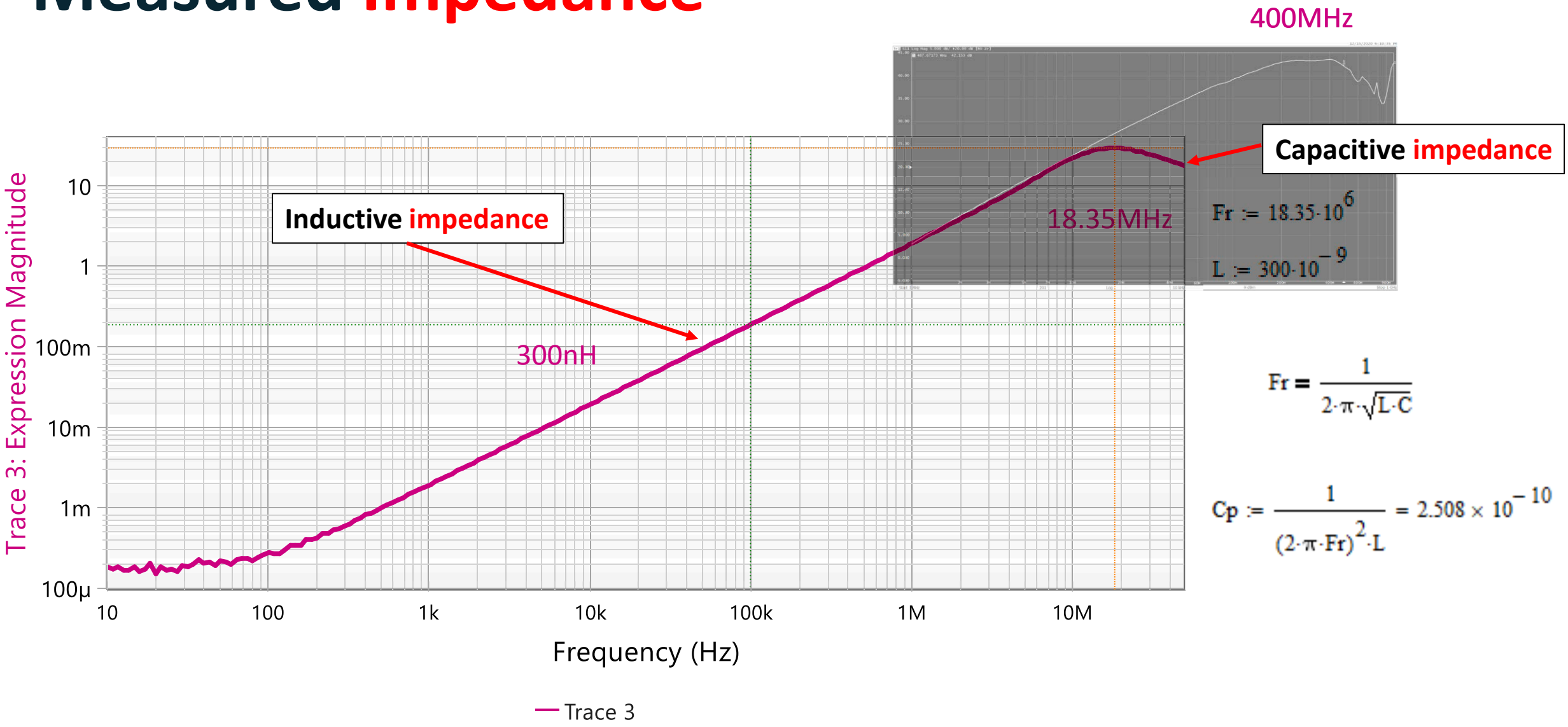


Product features

- 13.4 x 12.7 x 8.0mm surface mount package
- Ferrite core material
- High current carrying capacity, Low core losses
- Controlled DCR tolerance for sensing circuits
- Inductance range from 110nH to 440nH
- Current range from 37 to 120 Amps
- Frequency range up to 2MHz

PICOTEST

Measured Impedance

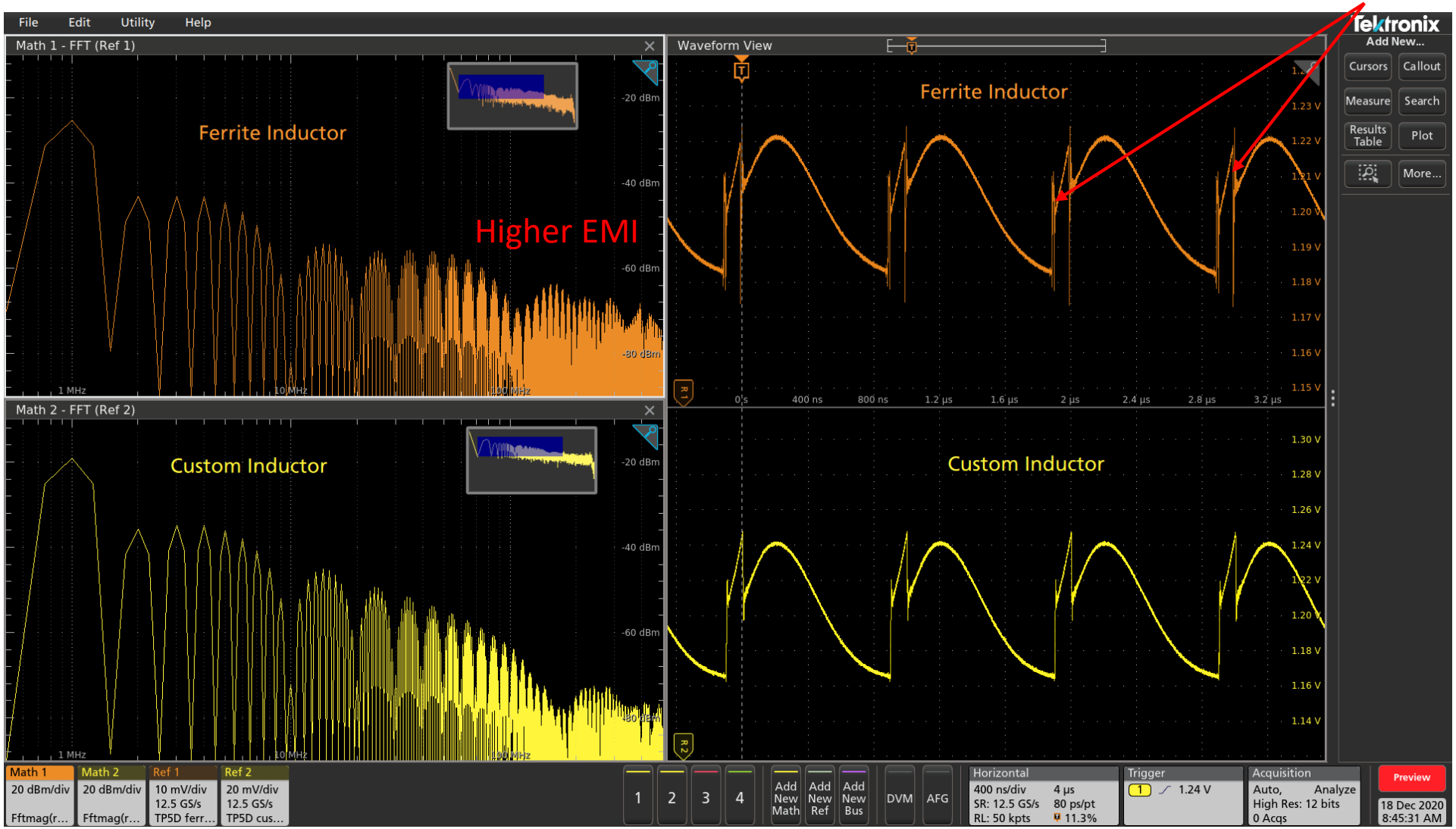


$$Fr = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$$

$$Cp := \frac{1}{(2 \cdot \pi \cdot Fr)^2 \cdot L} = 2.508 \times 10^{-10}$$

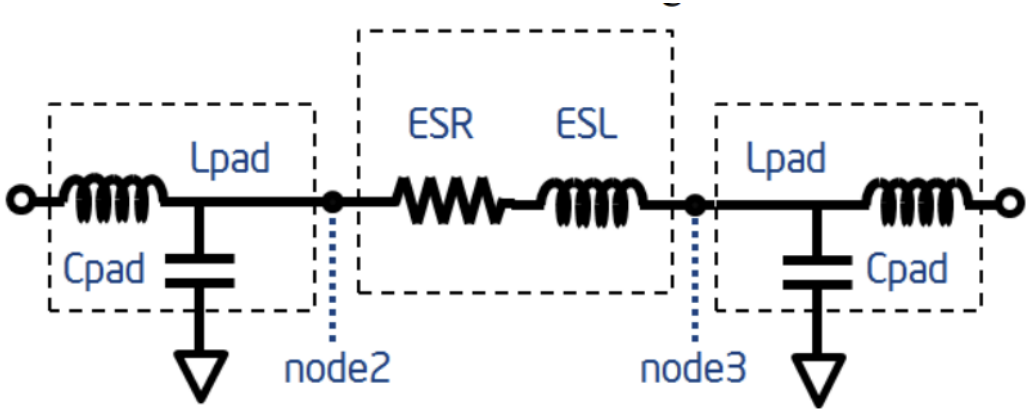
The Inductor SRF Impact

Impedance induced ringing

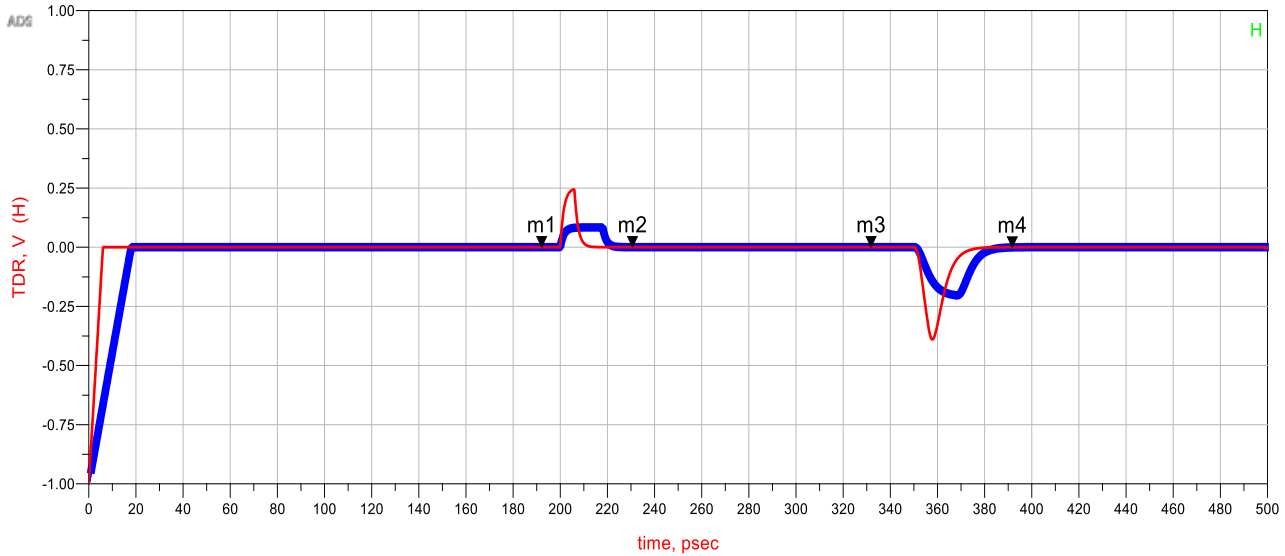


Even Higher Frequency SI Impedance Issues

High frequency capacitor model



http://b-dig.iie.org.mx/Bibdig2/P14-0270/PDF/Technical_Papers/123_3595.pdf

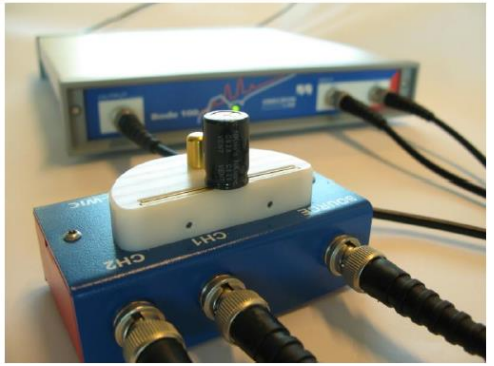


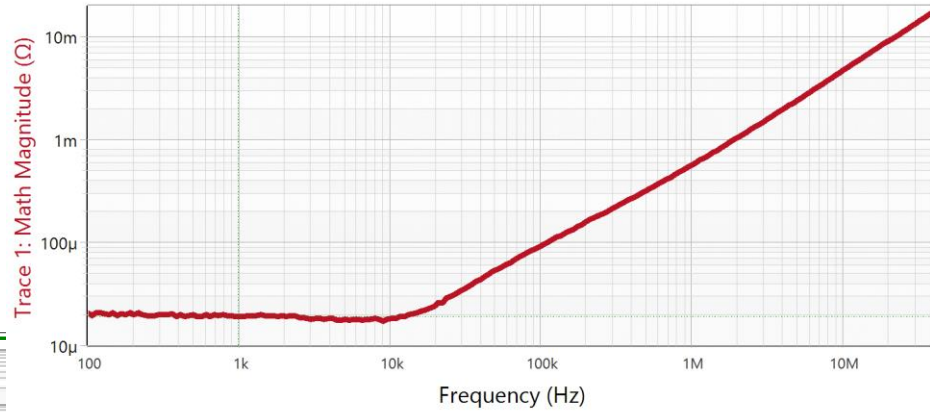
L	C
150.0 p	-149.8 f

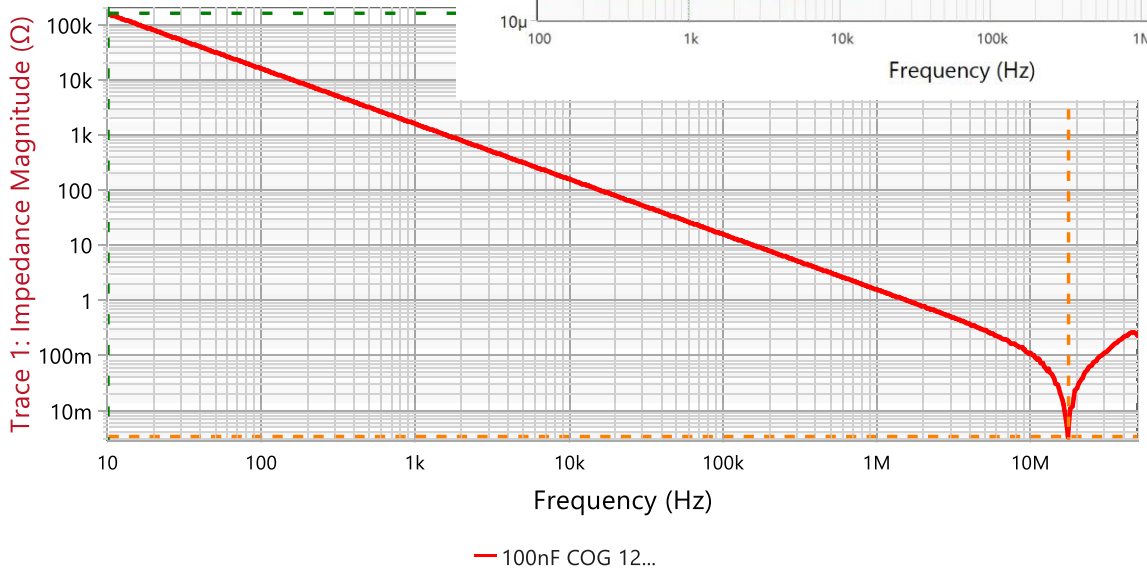
PICOTEST

How To Stay Out of Trouble??

- Choose components wisely – measure them. The manufacturer's specification will often leave out what you need to know
- The Bode 100 supports 7 impedance measurement options from uOhms to Mohms, and everything in between
- Measure your Bare boards. It isn't generally difficult to measure plane capacitance and inductance using the Bode 100
- Know how your designs impact other disciplines. Try to meet your own needs WITHOUT causing harm to others
- Everything is a compromise. Higher efficiency isn't a good thing if the result is that the system doesn't work







Key Takeaway

SI, PI, PE, and EMI don't have separate electrons, they interact with each other in a lot of different ways and through a lot of different paths. It is up to each of us to preserve SYSTEM Integrity and that means understanding the interactions and performing the fundamental measurements that are needed to preserve it.

I Don’t Expect You to Take My Word For It

Actually, I do, but in case you aren’t convinced that impedance is the common denominator…

https://www.tempoautomation.com/blog/using-impedance-control-to-manage-pcb-signal-integrity/

https://incompliancemag.com/article/emi-and-signal-integrity-how-to-address-both-in-pcb-design/

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/wp/wp_sgnlntgry.pdf

http://suddendocs.samtec.com/notesandwhitepapers/paper_track08_designing-dc-blocking-capacitor-transitions_designcon-2018.pdf

Thank You for Attending!

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