Average Current Mode Control
of Switch-Mode Power Supplies

MICROCHIP

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

Digital Control of Switch-Mode Power Supplies

Presented by Andreas Reiter

March 15th 2023

SMART | CONNECTED | SECURE

Power Conversion

Agenda

Power Supply Control Modes

Average Current Mode Control Implementation

Enforced Phase-Locking Method

Summary

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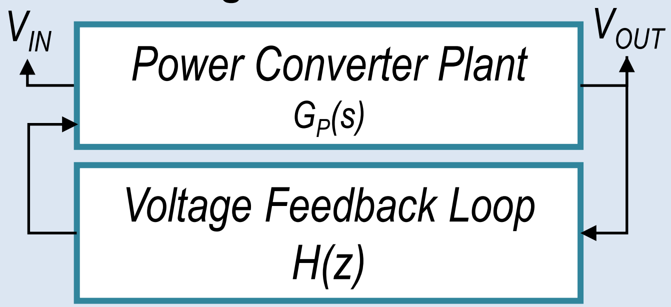
Switch-Mode Power Supply Control Modes

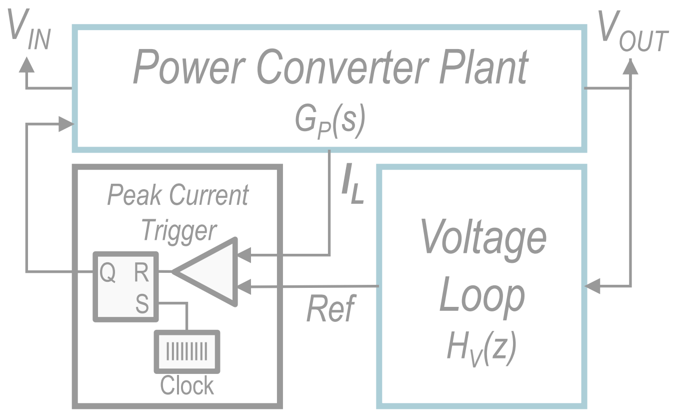
Comparison of typical, analog feedback loop implementations

Voltage Mode Control

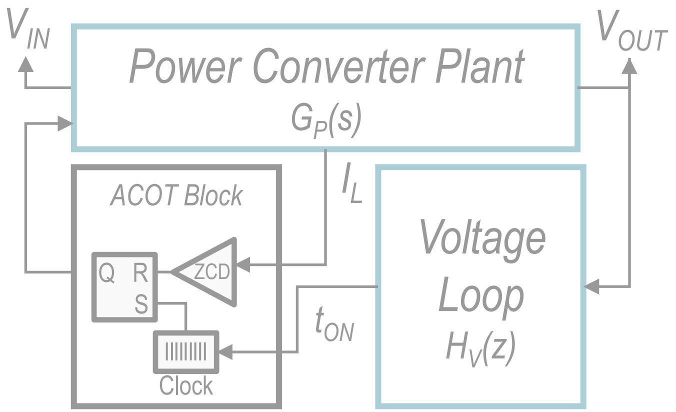


- **Indirect Control Method**
- **Universal, Topology-Agnostic***
- **Single (uncritical) Feedback Signal**
- **Applicable for**
  - Fixed Frequency
  - Variable Frequency
  - Phase Shift
- **Limitations**
  - Limited System Linearization
  - Varying Impedance
  - No Over Current Protection

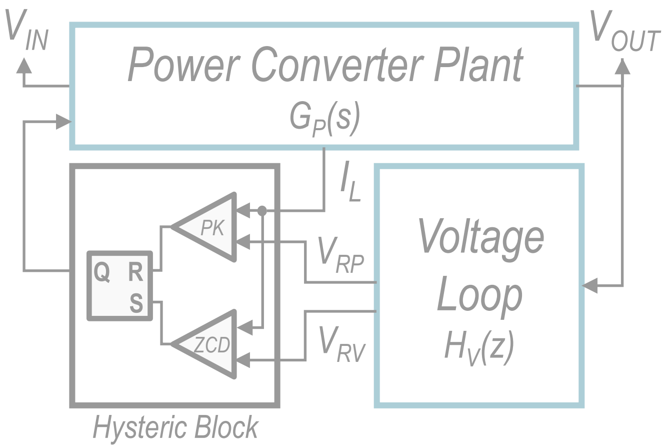
Peak Current Mode Control



Adaptive Constant On Time

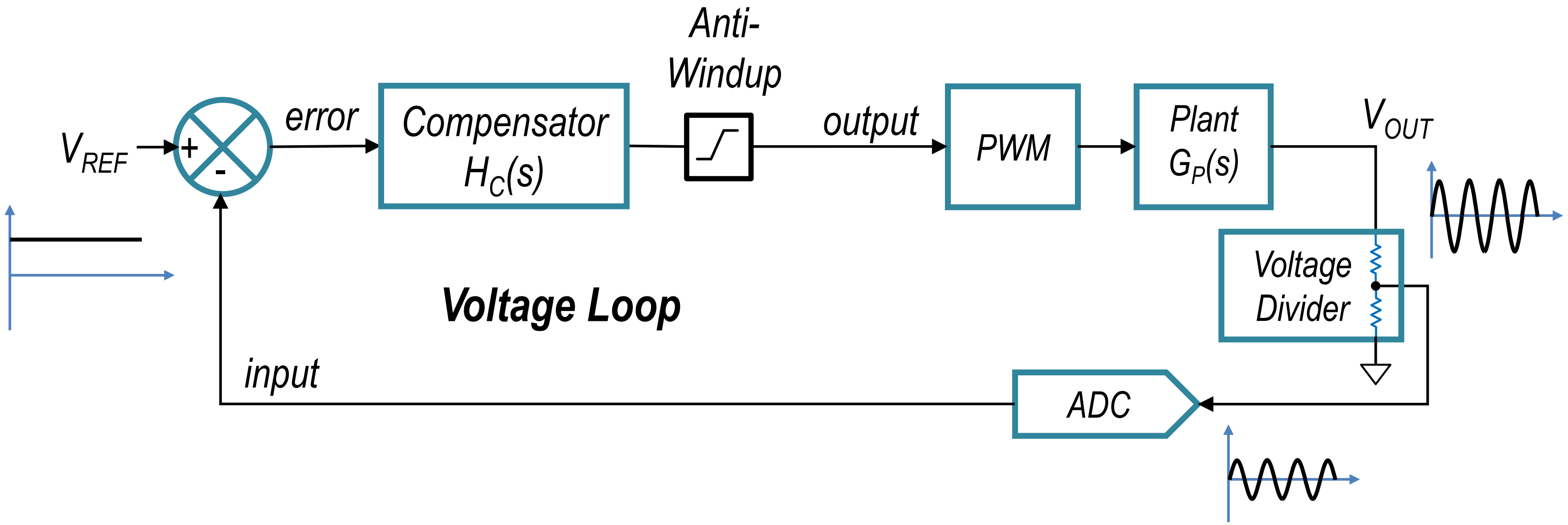


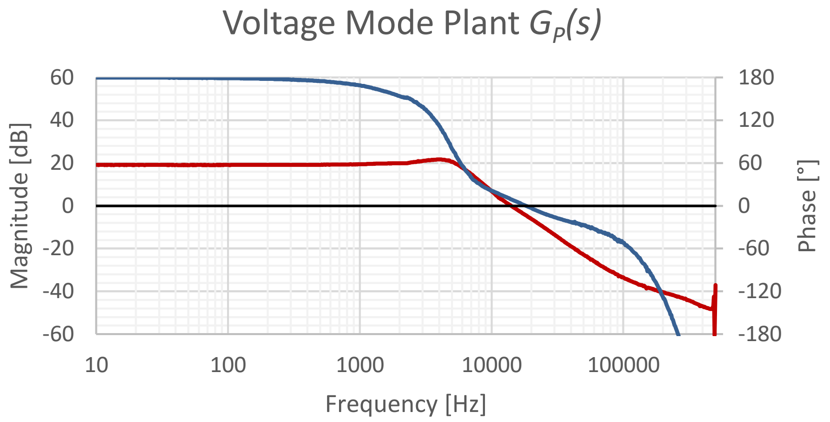
Hysteretic Mode Control

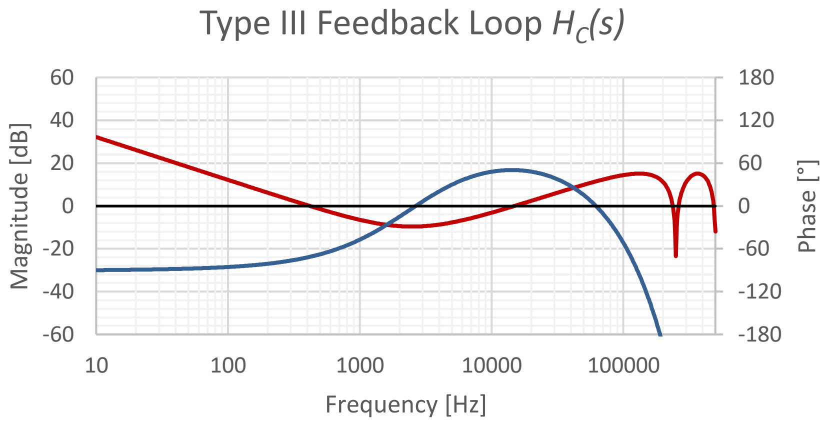


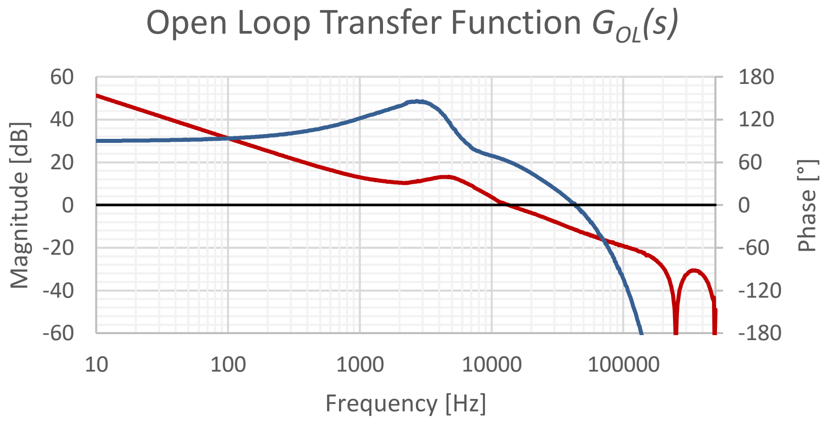
Digital Control Scheme

Single Voltage Mode Control Loop









Switch-Mode Power Supply Control Modes

Comparison of typical, analog feedback implementations

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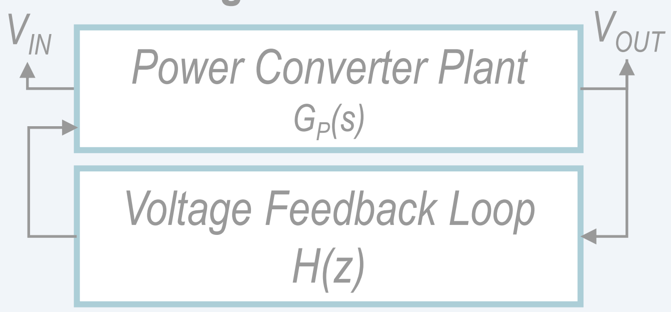

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lead to…

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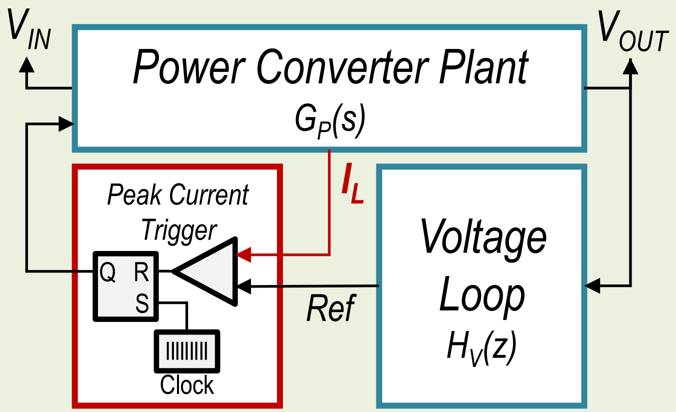

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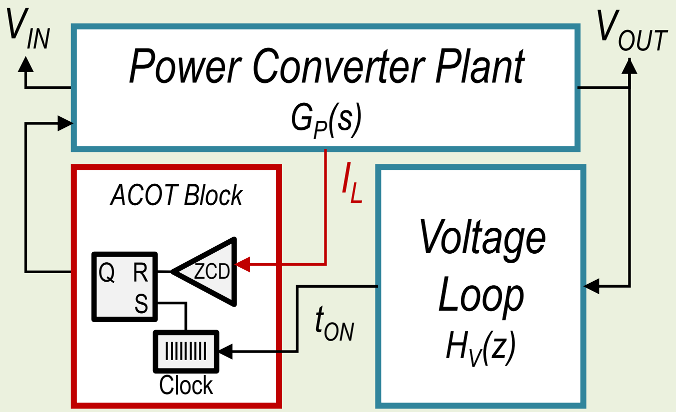

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- Modified Switch-Node Commutation
  - Inductor Current Control is Part of Switch Node (not the feedback loop)
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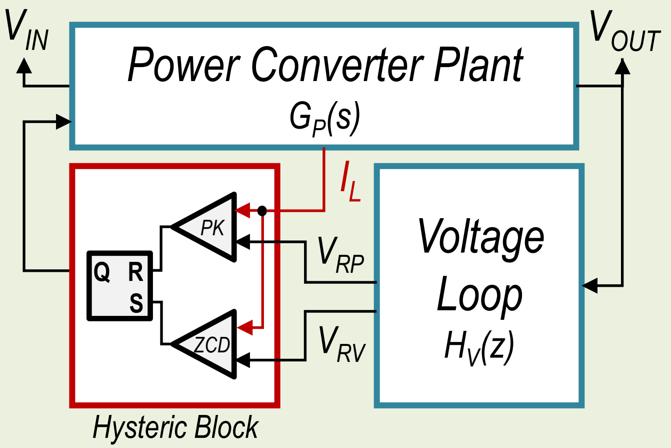
  - Phase Shift
  - COT and Hysteretic Control Applicable for Variable Frequency Only

Hysteretic Mode Control



Switch-Mode Power Supply Control Modes

Comparison of typical, analog feedback implementations

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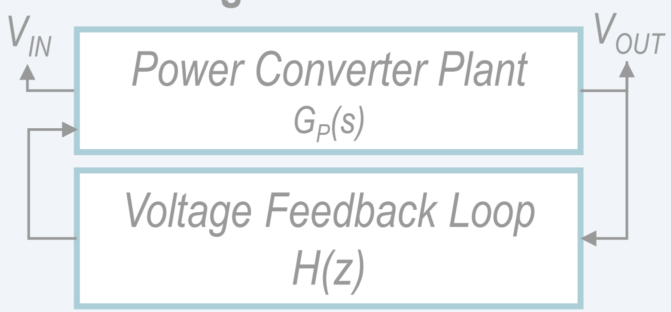

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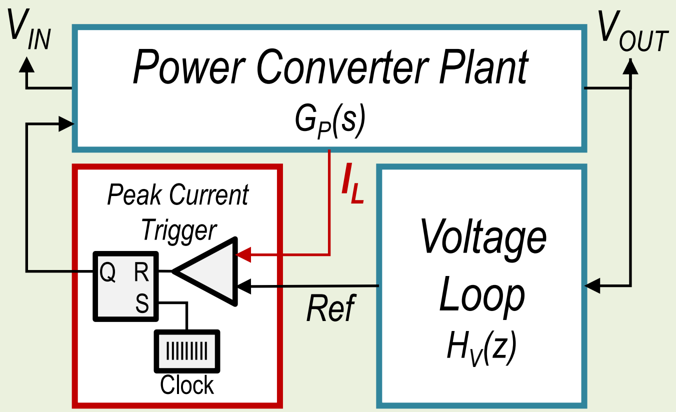

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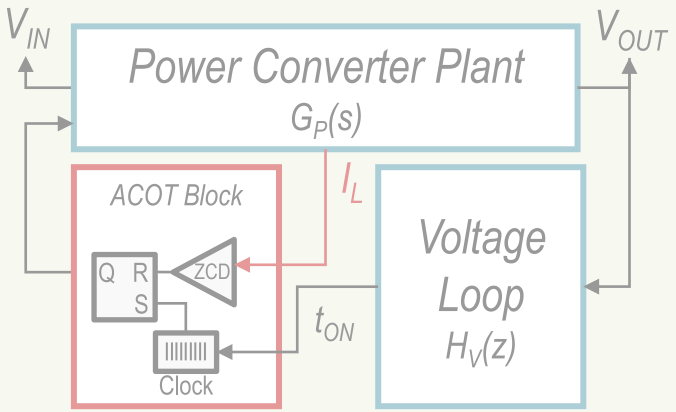
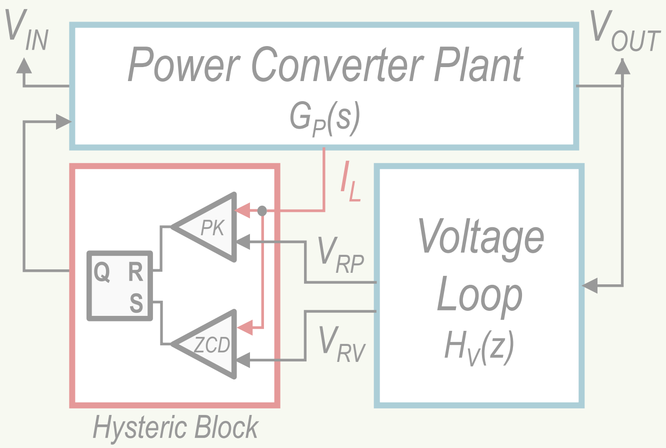
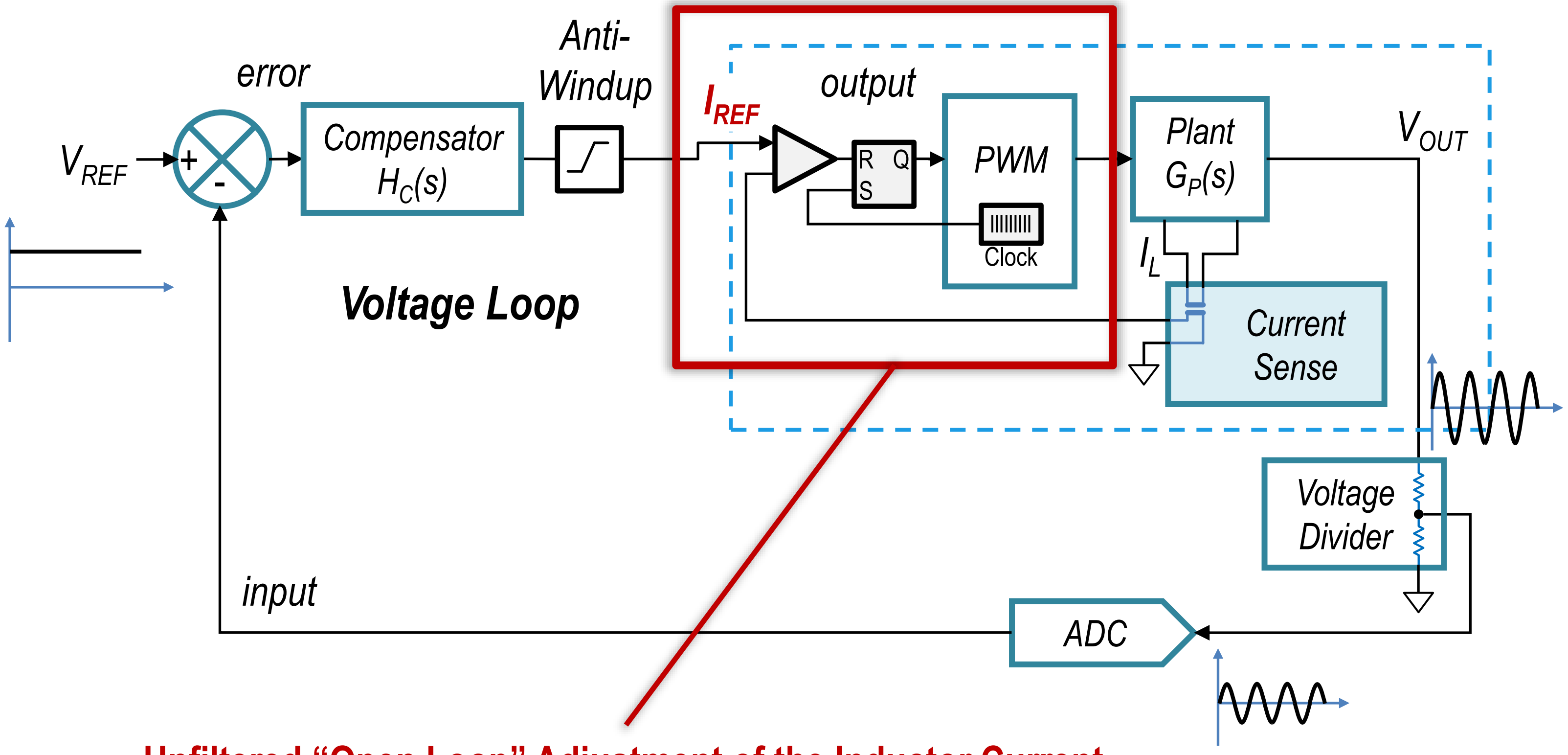


Hysteretic Mode Control

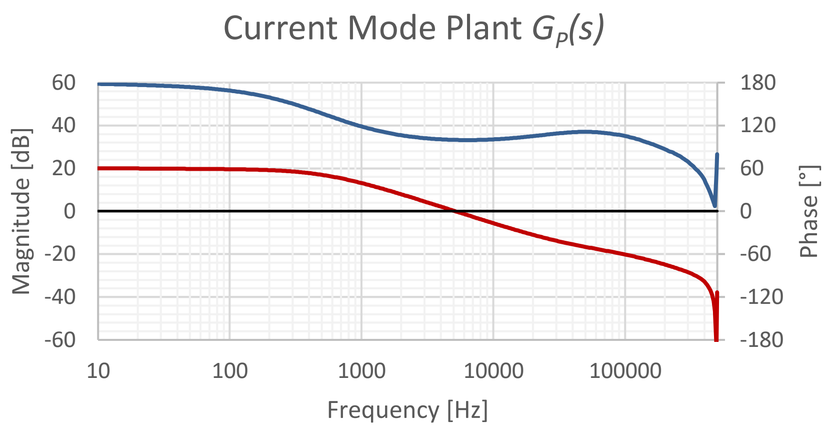


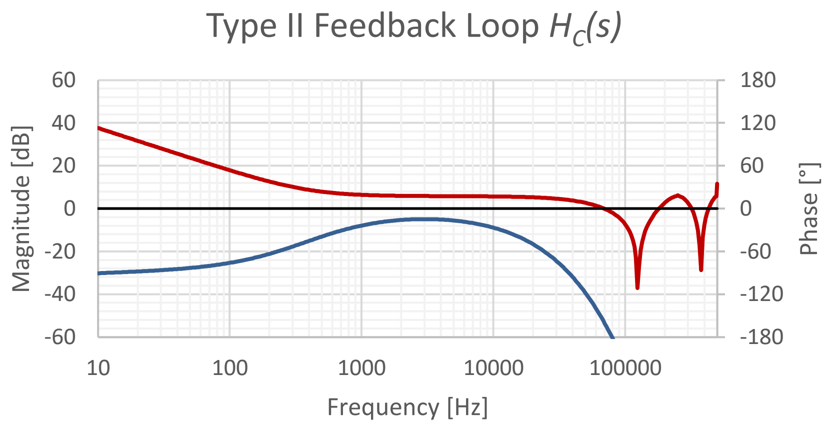
Digital Control Scheme PCMC

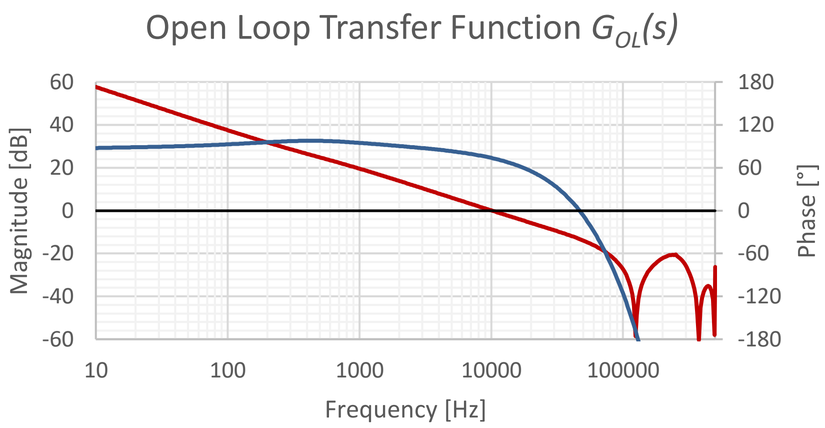
Peak Current Switch-Node Commutation



- **Unfiltered "Open Loop" Adjustment of the Inductor Current**
  - Injects Noise with every change in reference and load
  - Unfiltered PWM Signal Jitter
  - Indeterministic Current Limiting
  - Requires Synchronous Real Time Current Feedback

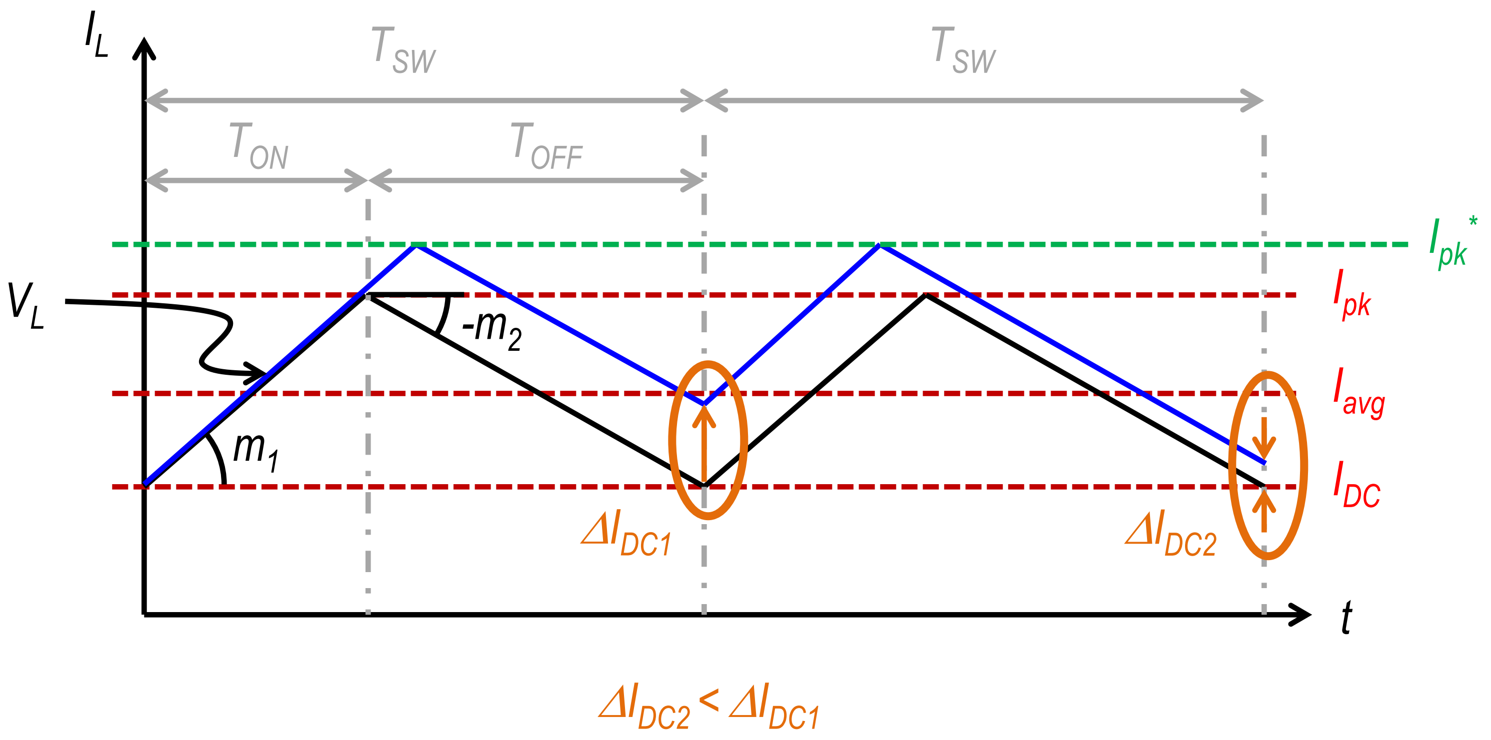






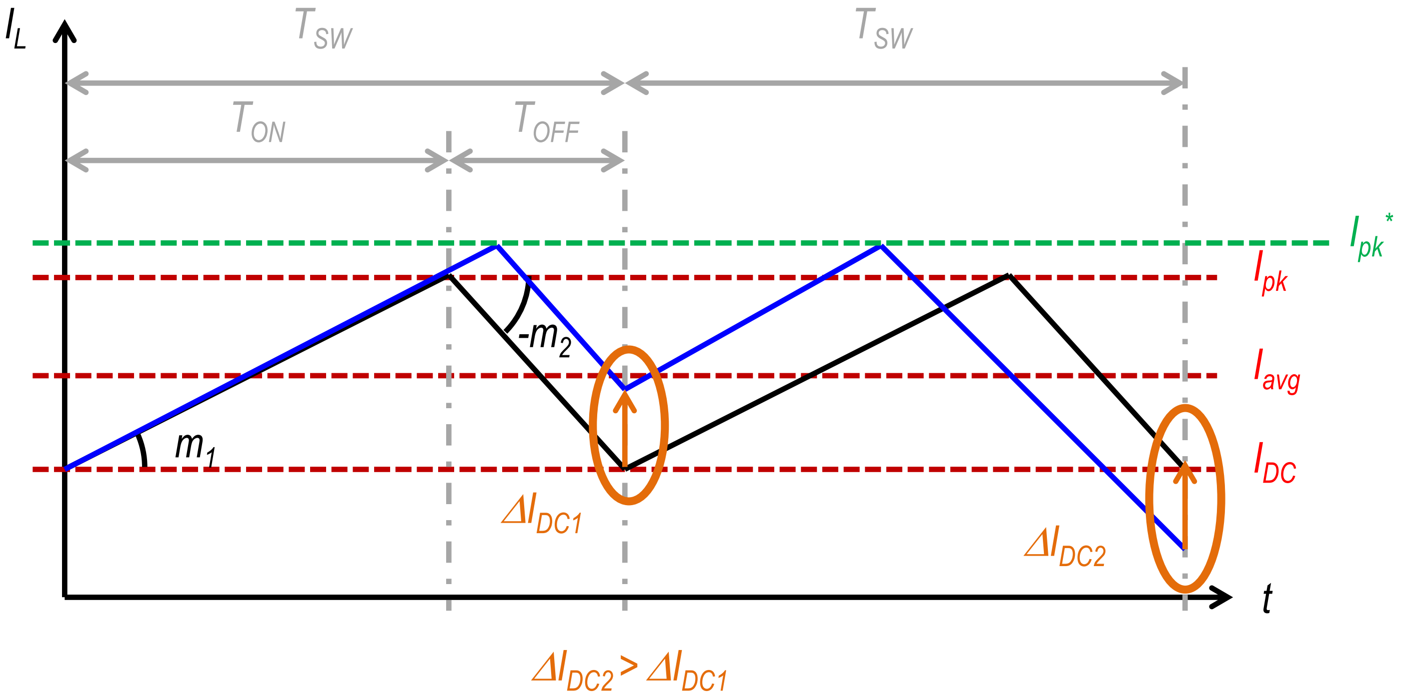
Peak Current Modulation

Fixed Frequency Continuous Conduction Operation at DC < 50%



Peak Current Modulation

Fixed Frequency Continuous Conduction Operation at DC > 50%



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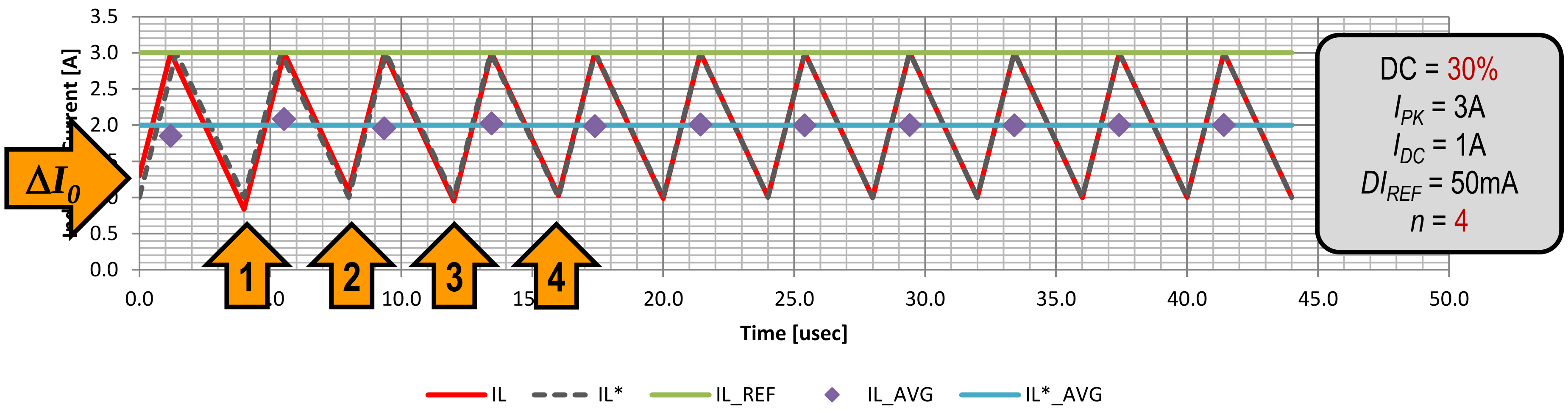
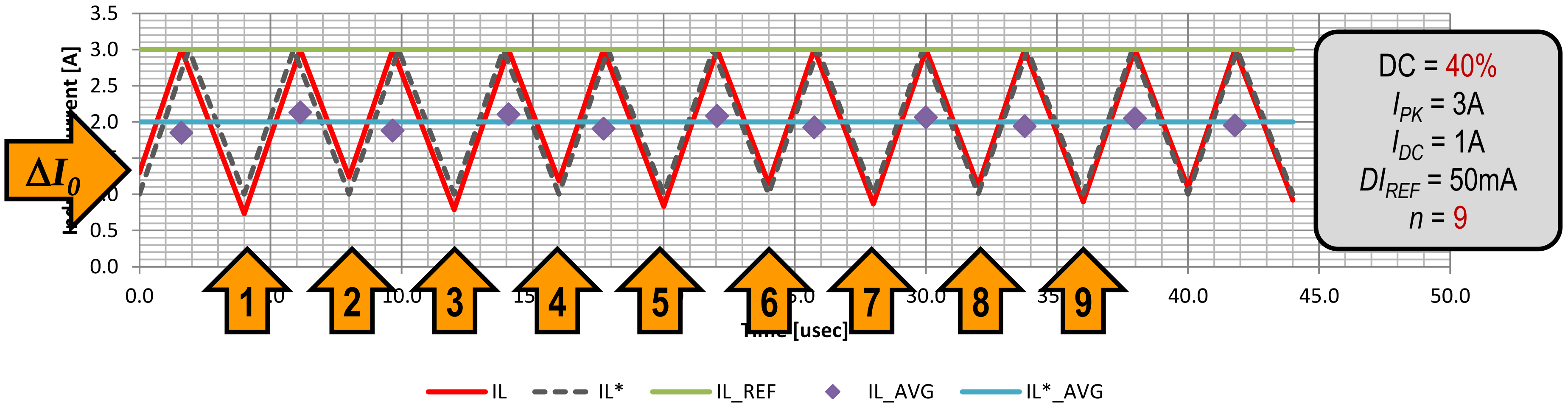
PCMC Current Modulation

Fixed Frequency Continuous Conduction Operation at DC < 50%





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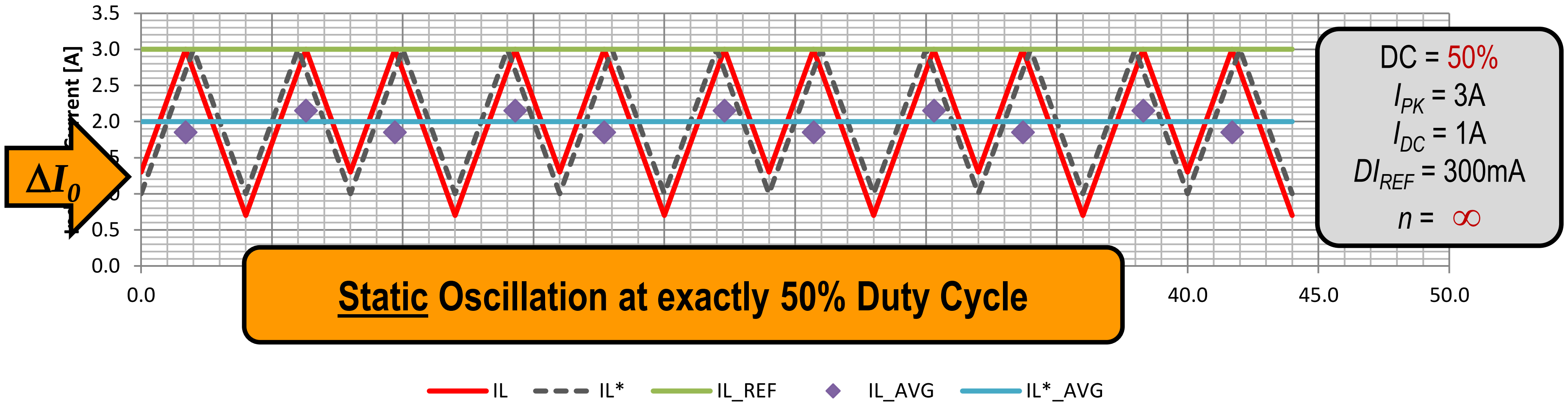

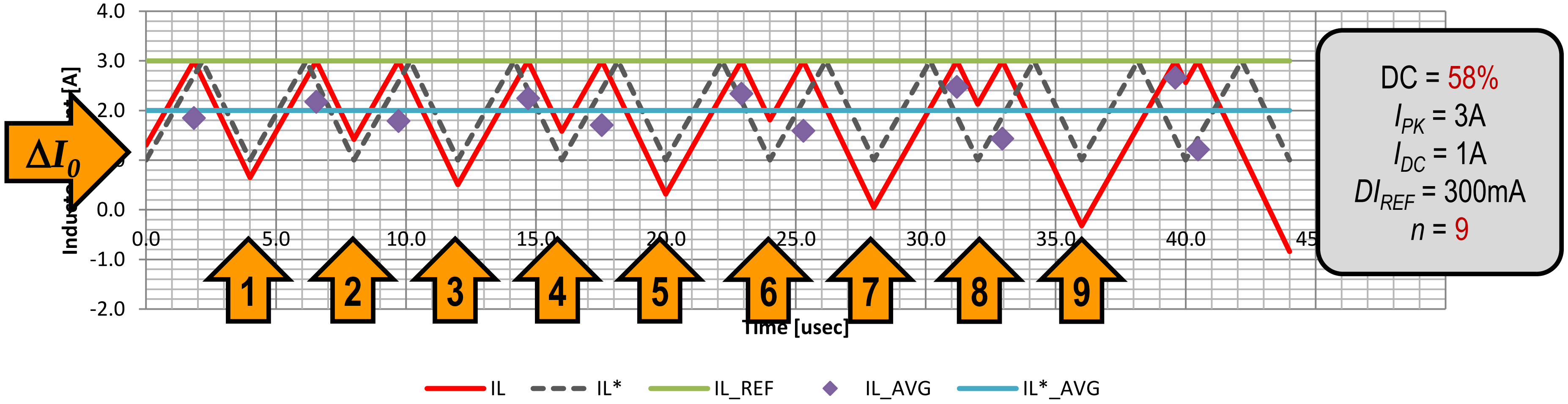

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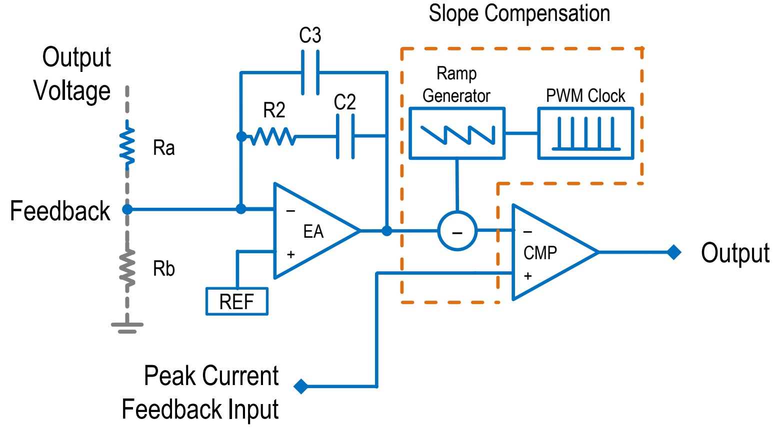
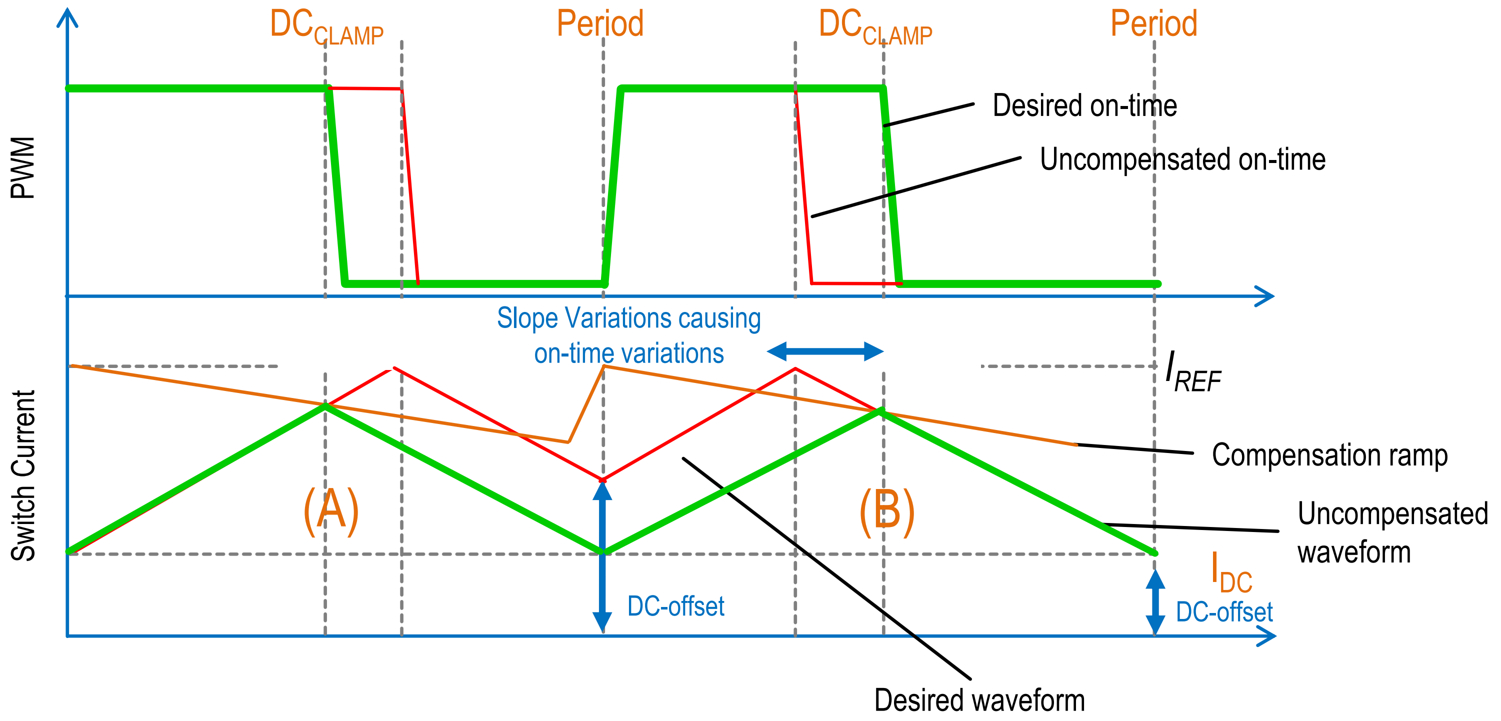
PCMC Current Modulation

Slope Compensation Implentation

Type II Peak Current Mode Control Compensator /w internal Slope Compensation





Response of voltage loop is slowed down with increasing duty cycle.
Side effects: Gain variations and Voltage Droop

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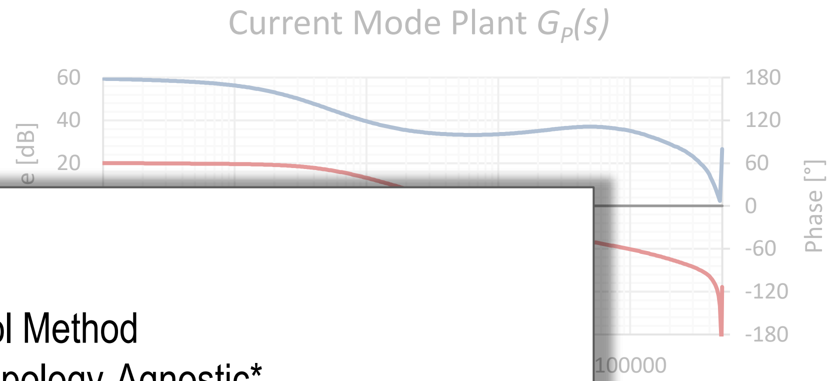
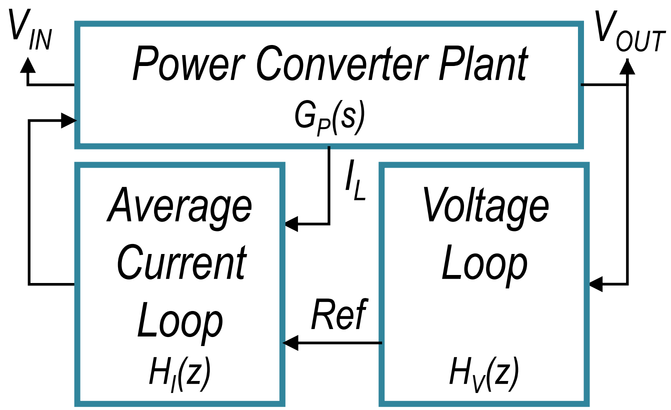
Digital Control Scheme PCMC

Peak Current Switch-Node Commutation



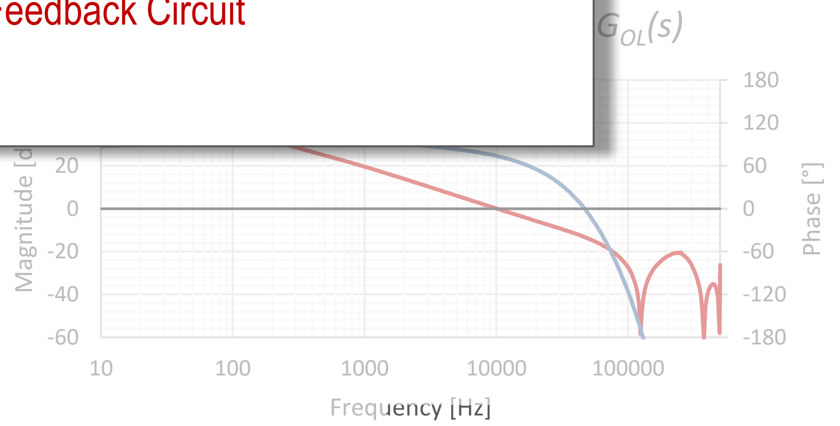
Solution

Average Current Mode Control



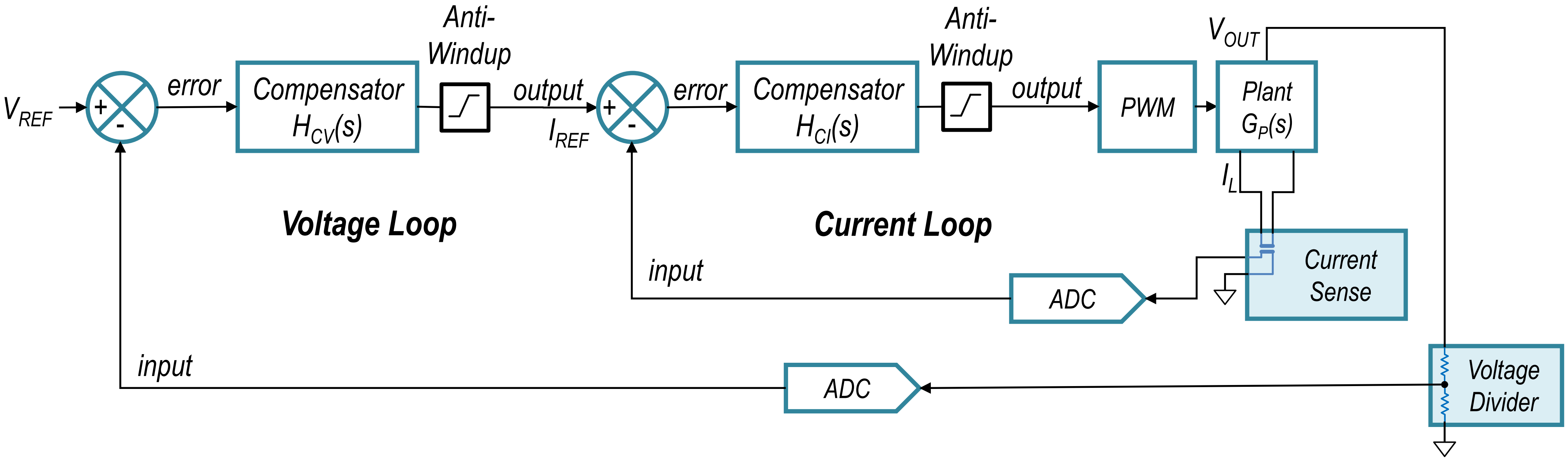
- Direct Control Method
- Universal, Topology-Agnostic*
- Constant Impedance
- Over Current Protection
- Constant Current Limit
- Applicable for
  - Fixed Frequency
  - Variable Frequency
  - Phase Shift
- Challenges
  - Complex Feedback Circuit

- Unfiltered "Open Loop" Adjustment of the Inductor Current
  - Injects Noise with every change in reference and load
  - Unfiltered PWM Signal Jitter
  - Indeterministic Current Limiting
  - Requires Synchronous Real Time Current Feedback



Digital Control Scheme ACMC

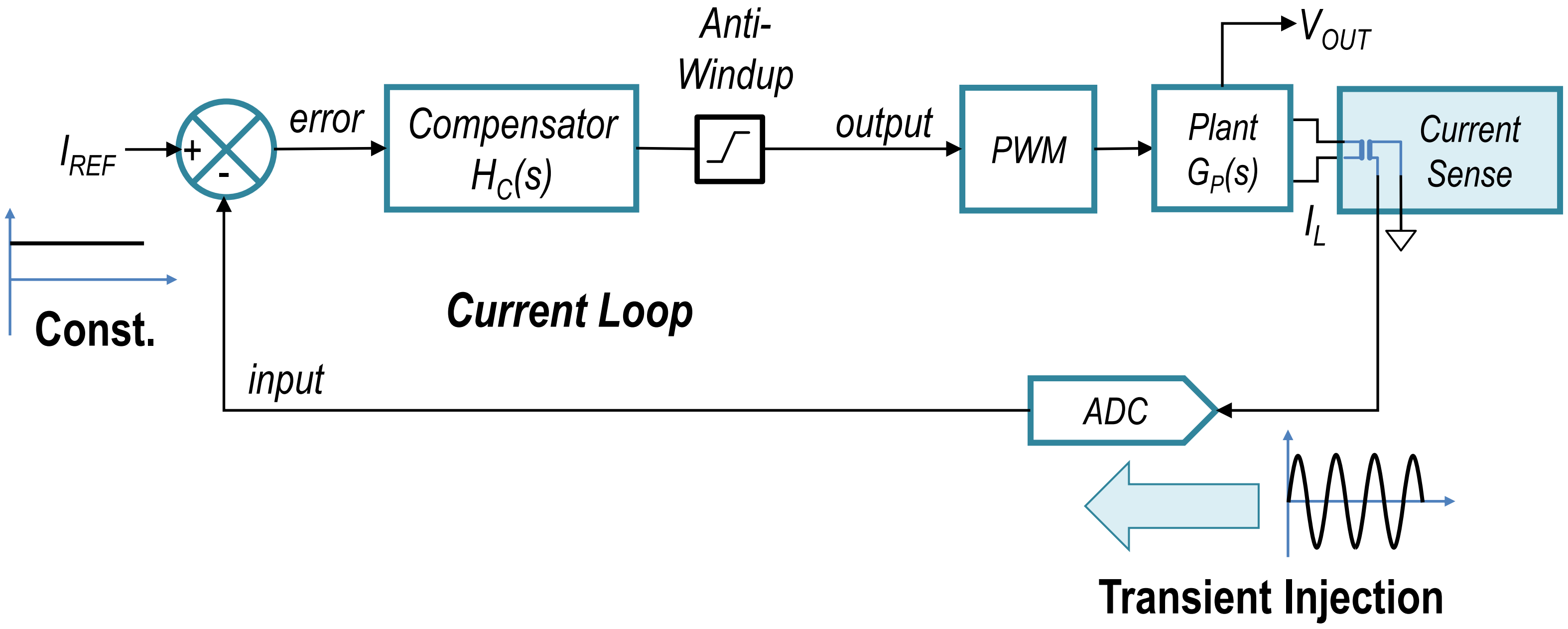
Cascaded Average Current Mode Control Loop(s)



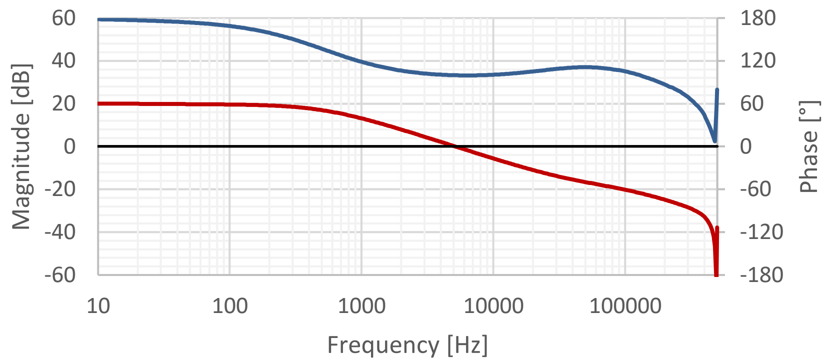
The average current feedback loop is established by cascading a dedicated voltage and current loop compensator, each tied to its respective feedback signal. Just like in peak current mode control, the outer voltage loop compensator output provides the reference for the inner current loop, where a second compensation filter adjusts the average inductor current by adjusting the modulated switch node control signal.

Digital Control Scheme ACMC

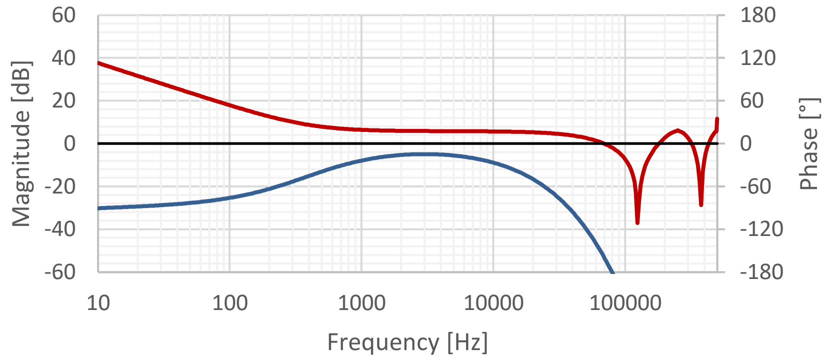
Step 1: Single Current Loop Controller



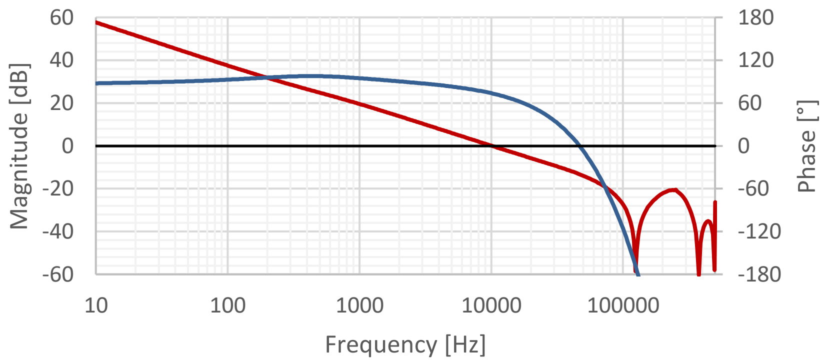
Current Mode Plant $G_P(s)$



Type II Feedback Loop $H_C(s)$



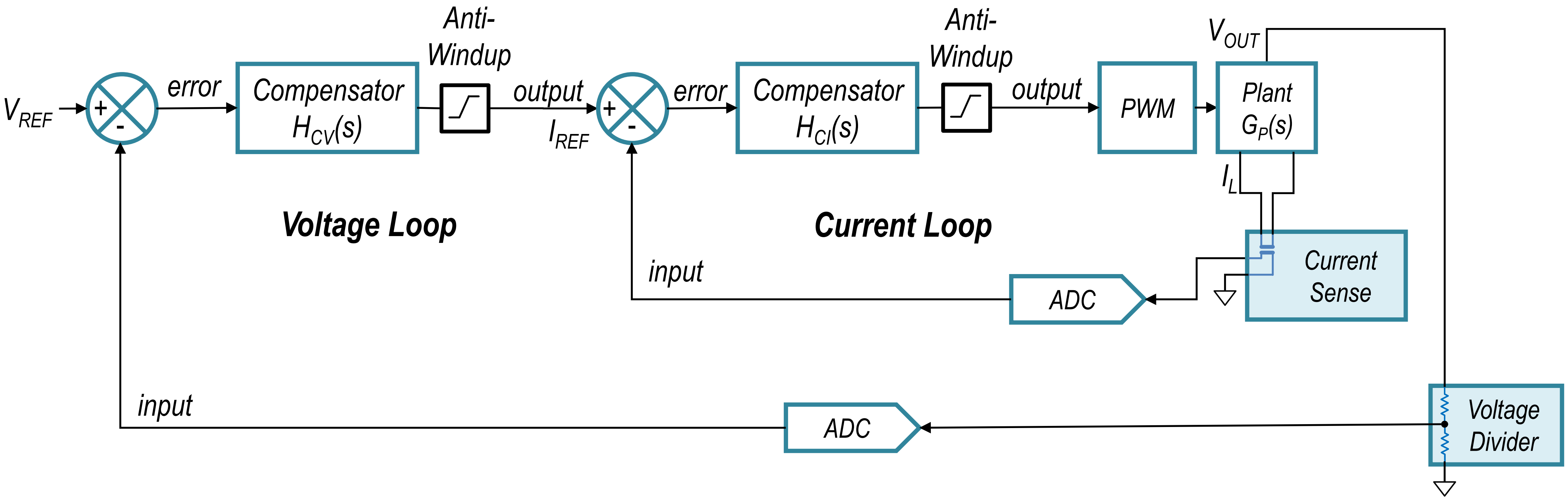
Open Loop Transfer Function $G_{OL}(s)$



When we measure the inner current loop, we find the current mode plant transfer function being almost identical to its peak current mode counter part, mainly shaped by one dominant plant pole.

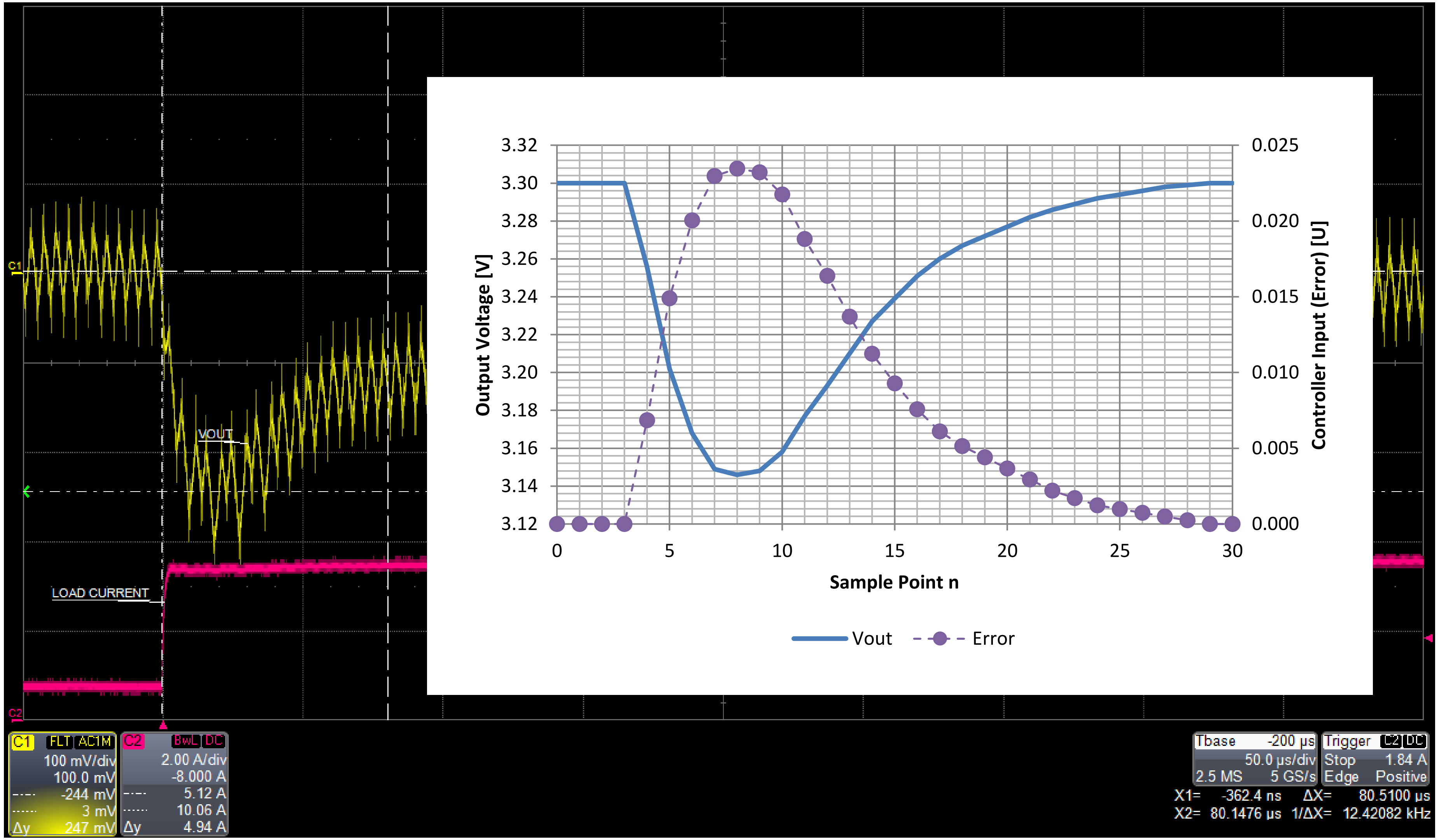
Digital Control Scheme ACMC

Step #2: Closing the Voltage Loop



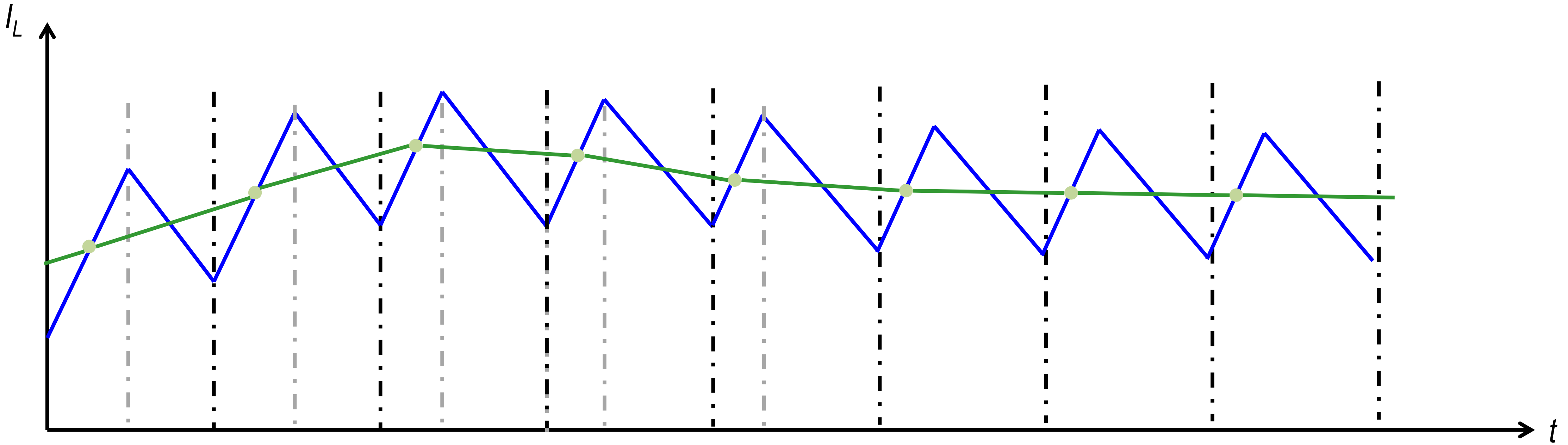
Average Current Mode Step Response

Control Loop Response vs. Output Voltage



Average Current Mode Step Response

Control Loop Current Response



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Digital Control Scheme ACMC

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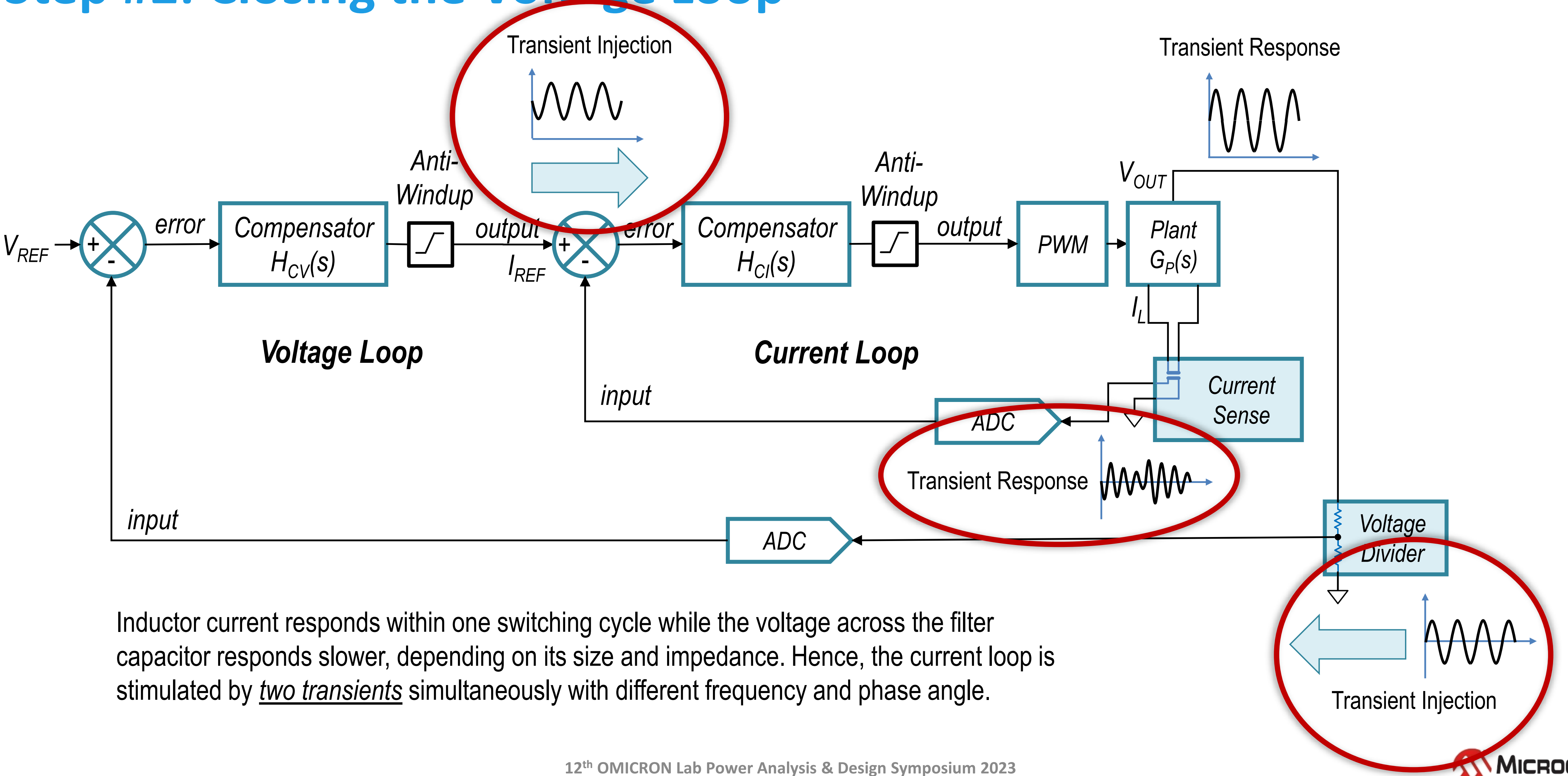
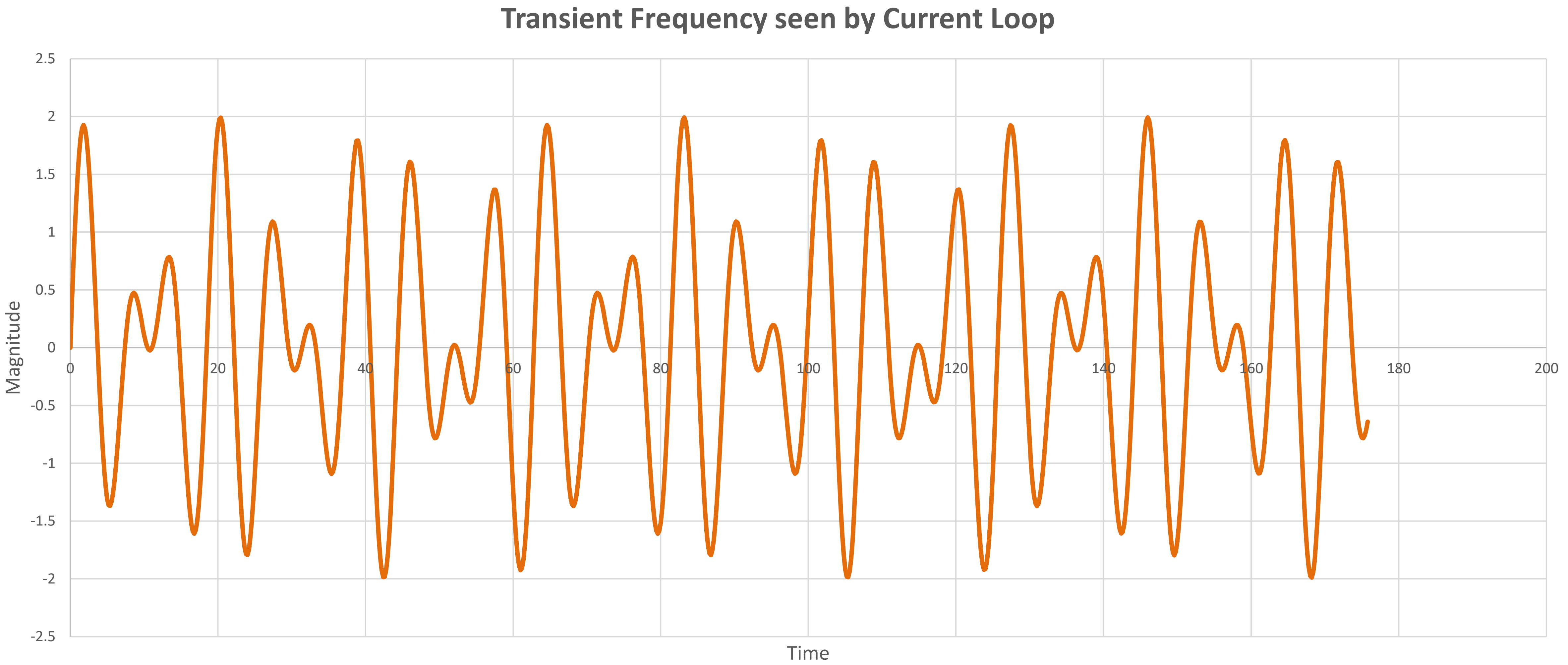


Inductor current responds within one switching cycle while the voltage across the filter capacitor responds slower, depending on its size and impedance. Hence, the current loop is stimulated by *two transients* simultaneously with different frequency and phase angle.

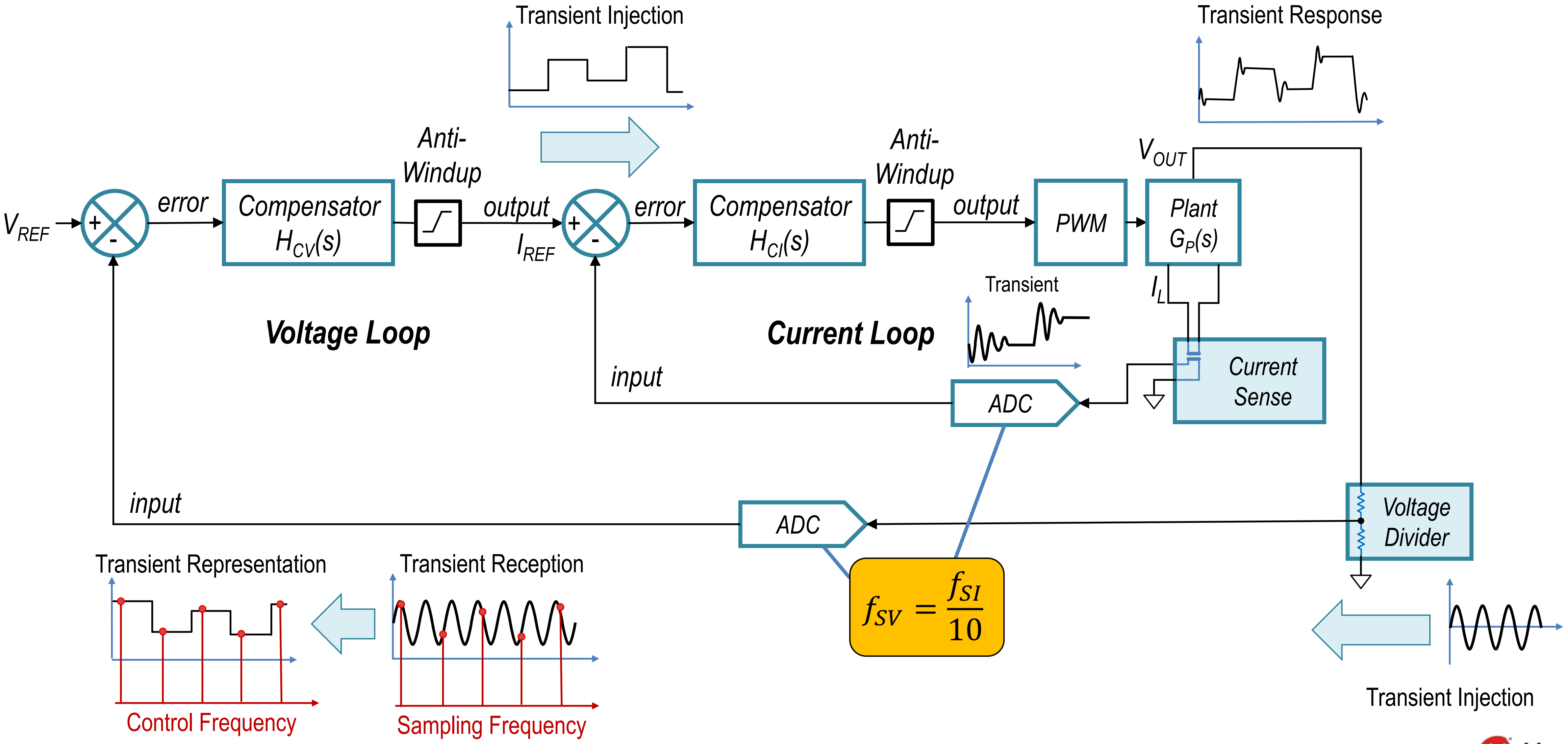
Current Loop Transient Profile

Transient signal waveform when stimulated on Reference and Feedback



Voltage-to-Current Loop Synchronization

Approach #1: Sample Frequency Decoupling



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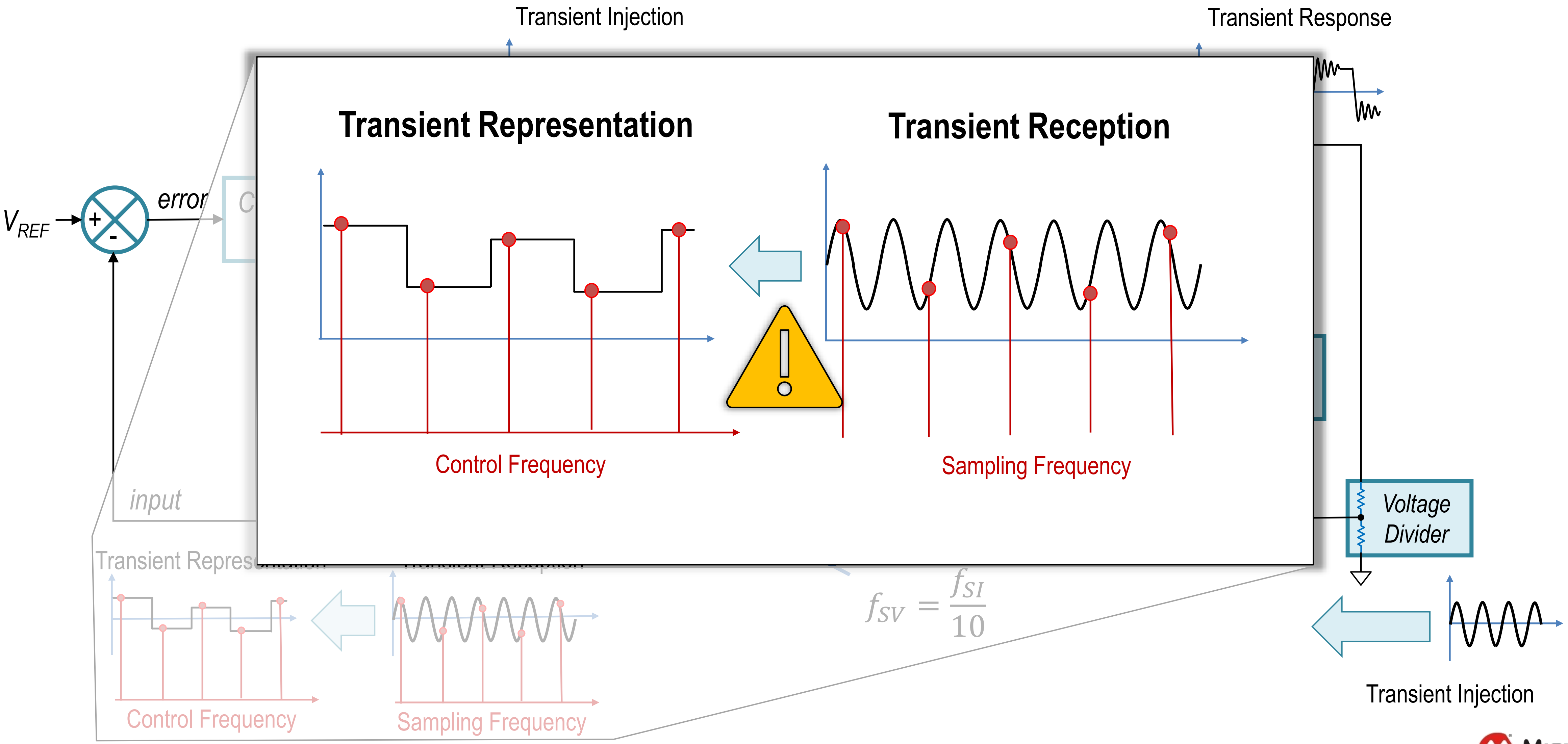
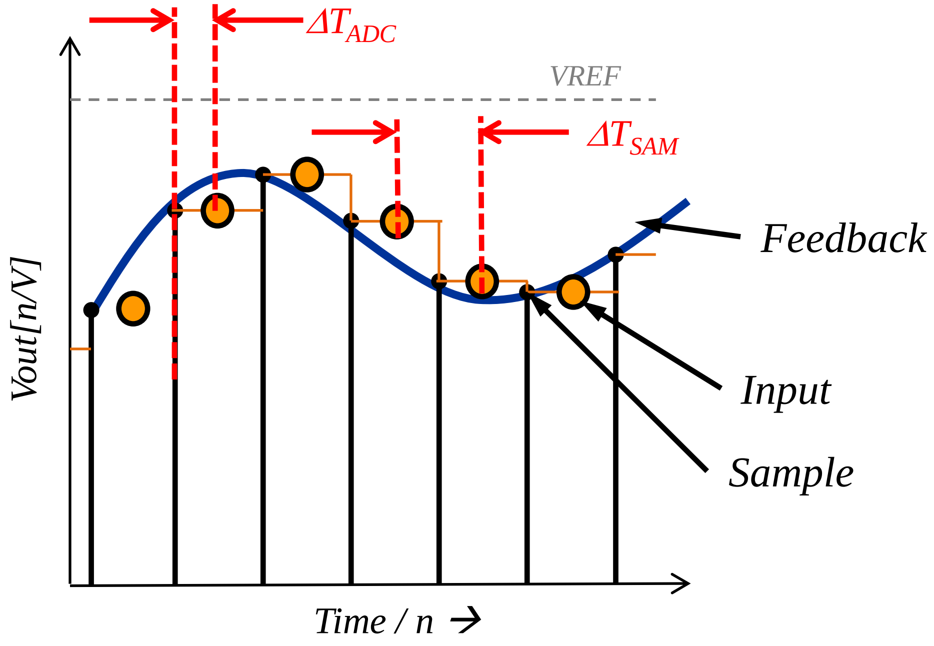


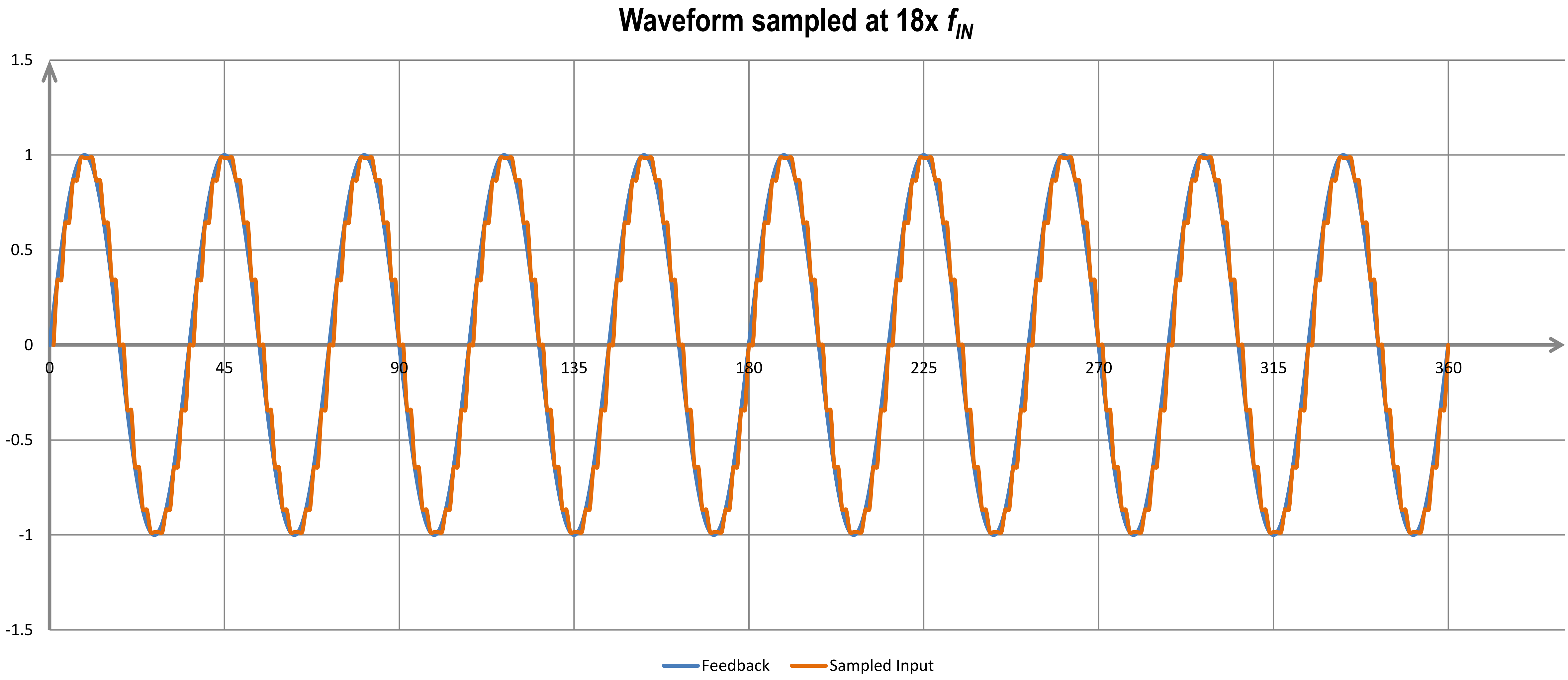
Discrete Time Domain Data Acquisition



- The acquired signal is represented in “instantaneous” steps
- Signal sampling and conversion invokes phase shift
- The last sample is valid until it is updated by the next sample

Alias Frequencies

Sufficient Oversampling Ratio (Alias-free Result)



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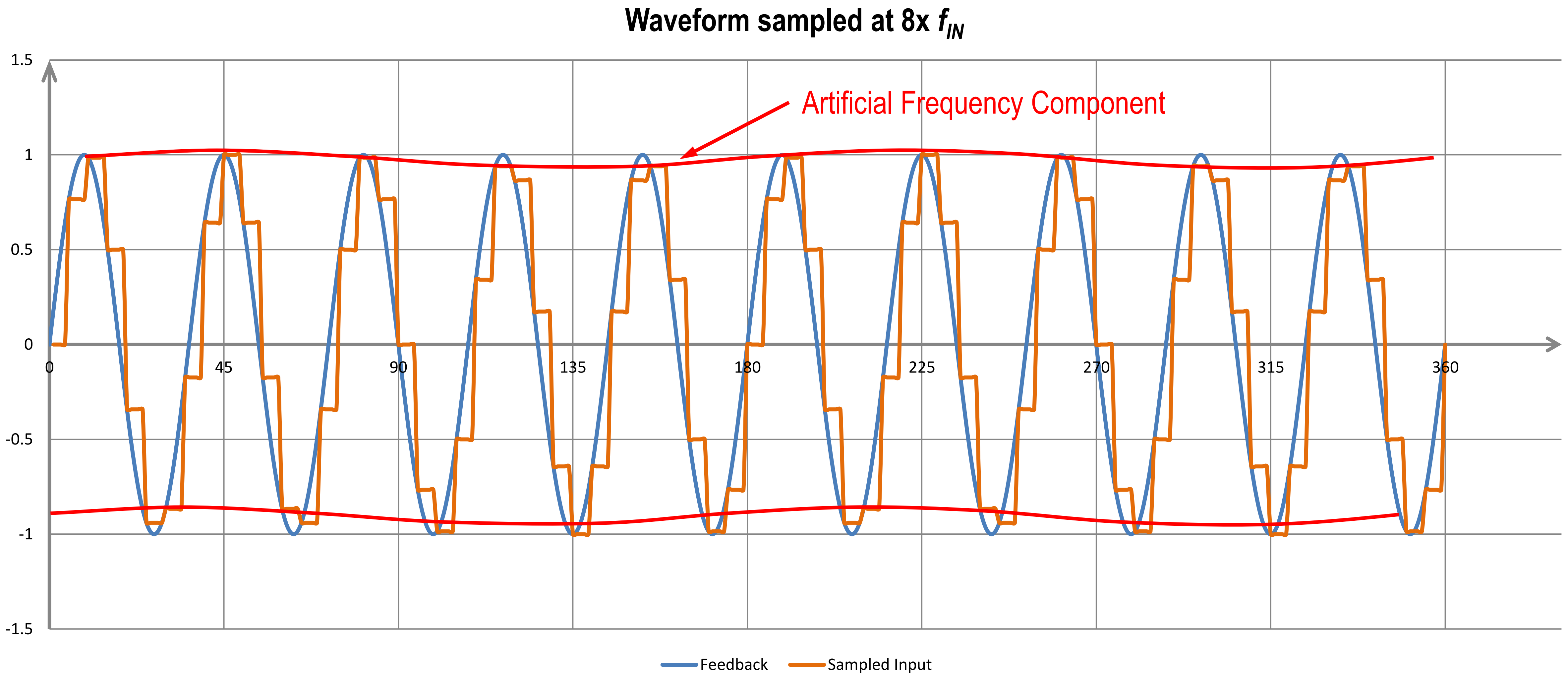
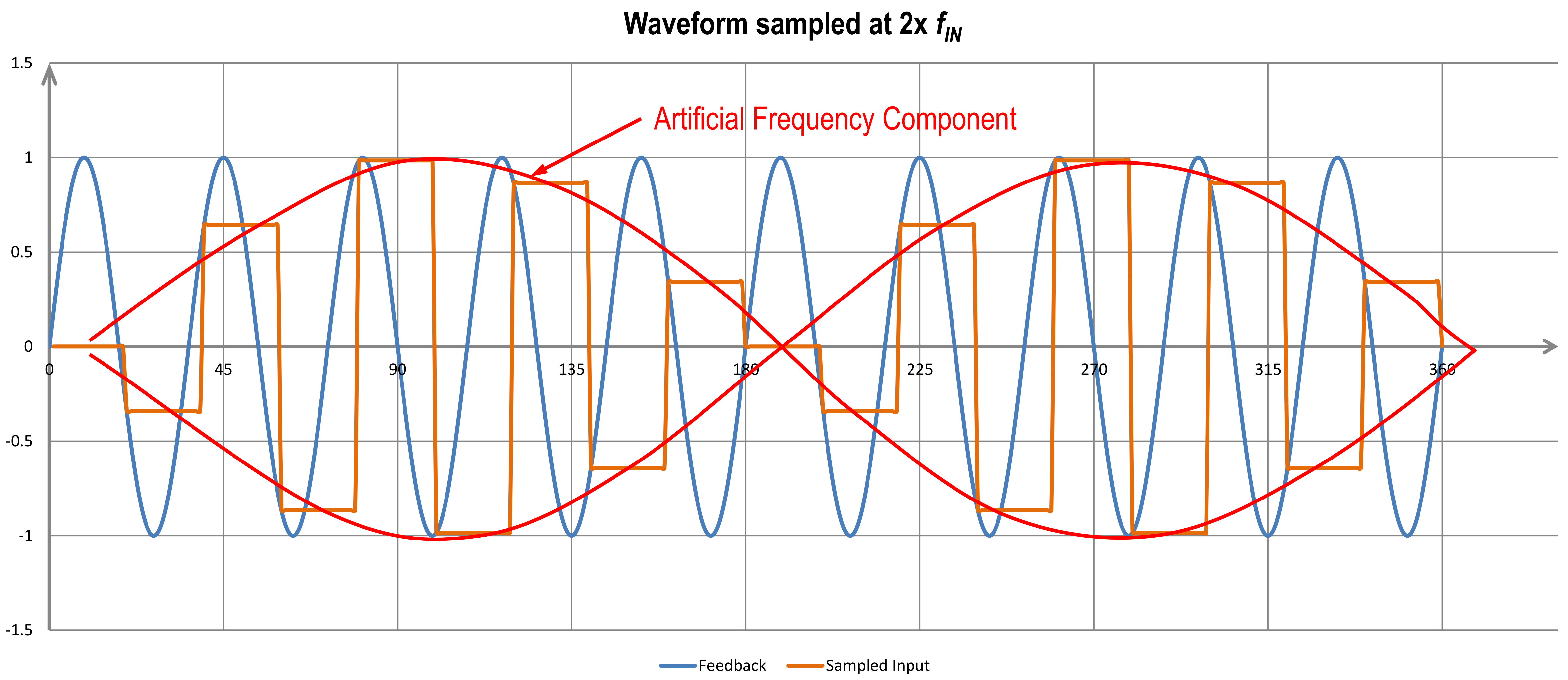
Alias Frequencies

First Visible Sub-Frequency Component @ $f_{IN} \approx 1/8^{th}$ of f_{SAMPLE}



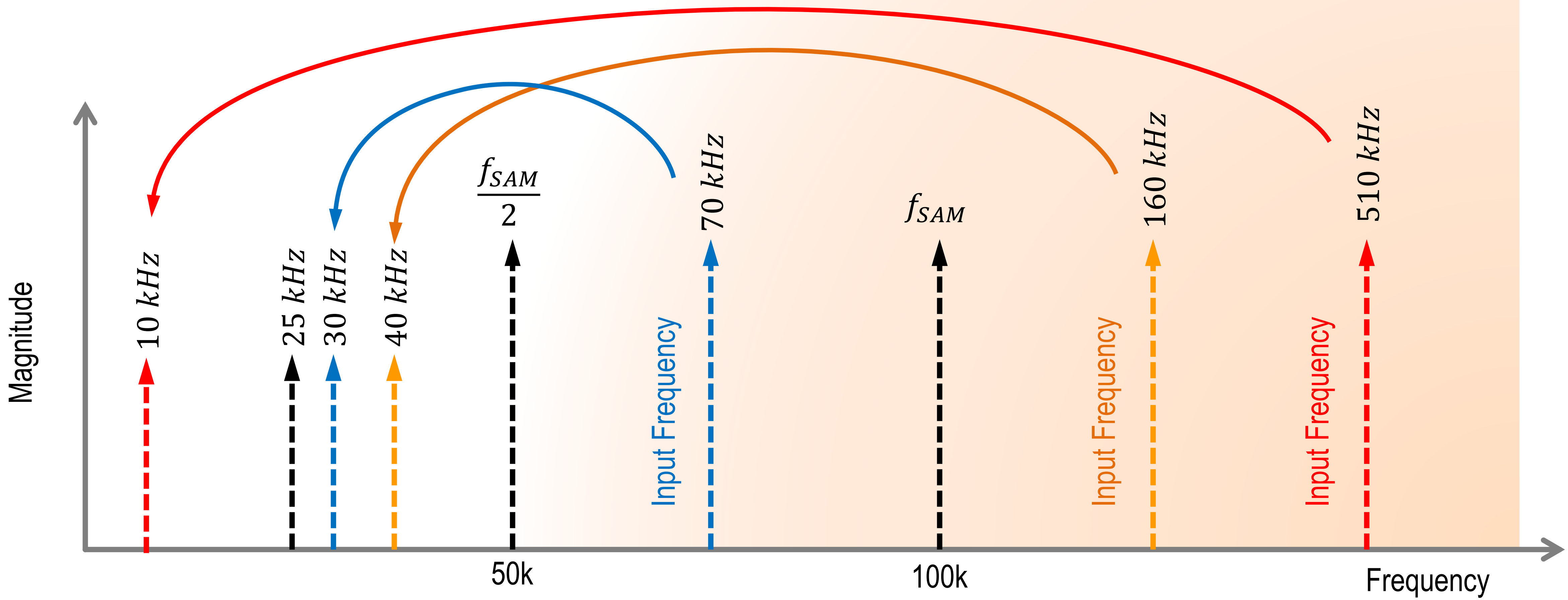
Aliasing

Highly distorted Result @ $f_{IN} = f_{NYQUIST} = ½ \text{ of } f_{SAMPLE}$



Aliasing Example

- Once injected, alias frequencies cannot be distinguished from real frequencies!



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Voltage-to-Current Loop Synchronization

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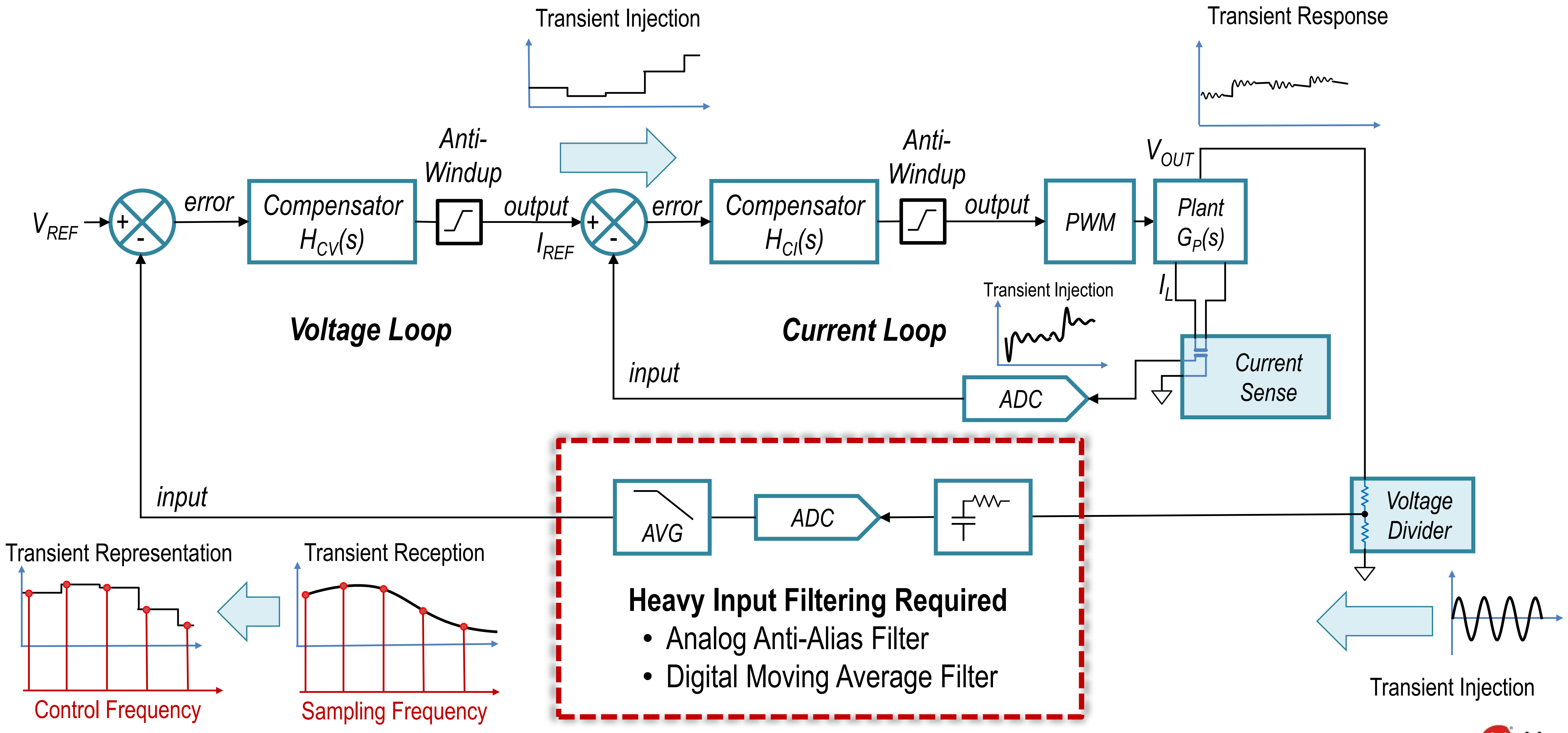

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Voltage-to-Current Loop Synchronization

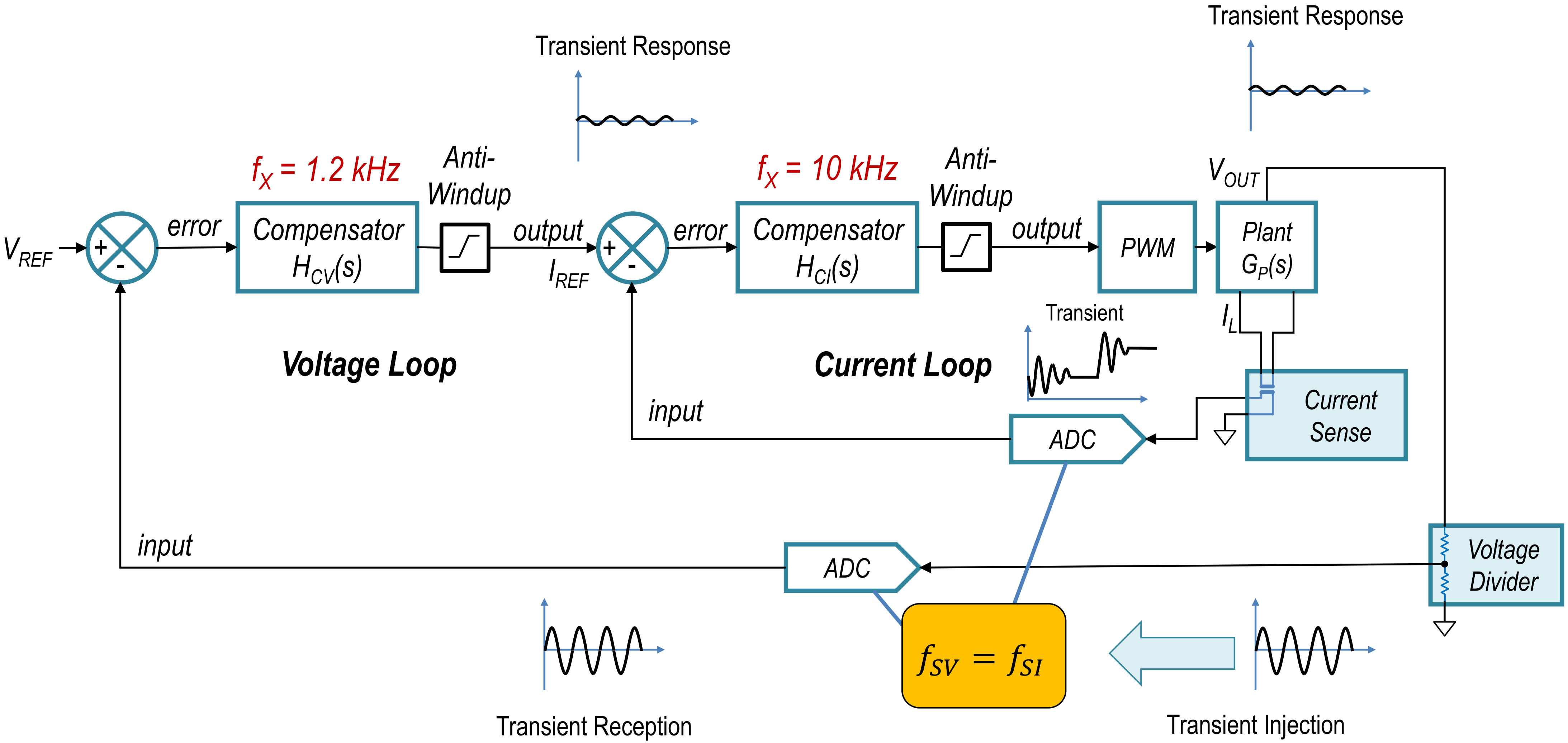
Approach #1: Sample Frequency Decoupling

- **Challenges**
  - Fast current response injects noise into voltage feedback
  - High frequency noise must be filtered preventing alias frequencies from affecting the voltage loop, making the voltage loop even slower
  - Slow voltage loop response injects step artefacts into output voltage
  - **Low bandwidth response**

- **Applicable**
  - Driving large capacitive loads (e.g. battery chargers)
  - Power Factor Correction

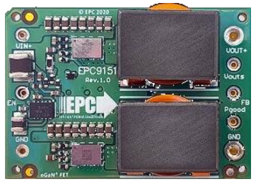
Voltage-to-Current Loop Synchronization

Approach #2: Low Gain Voltage Loop

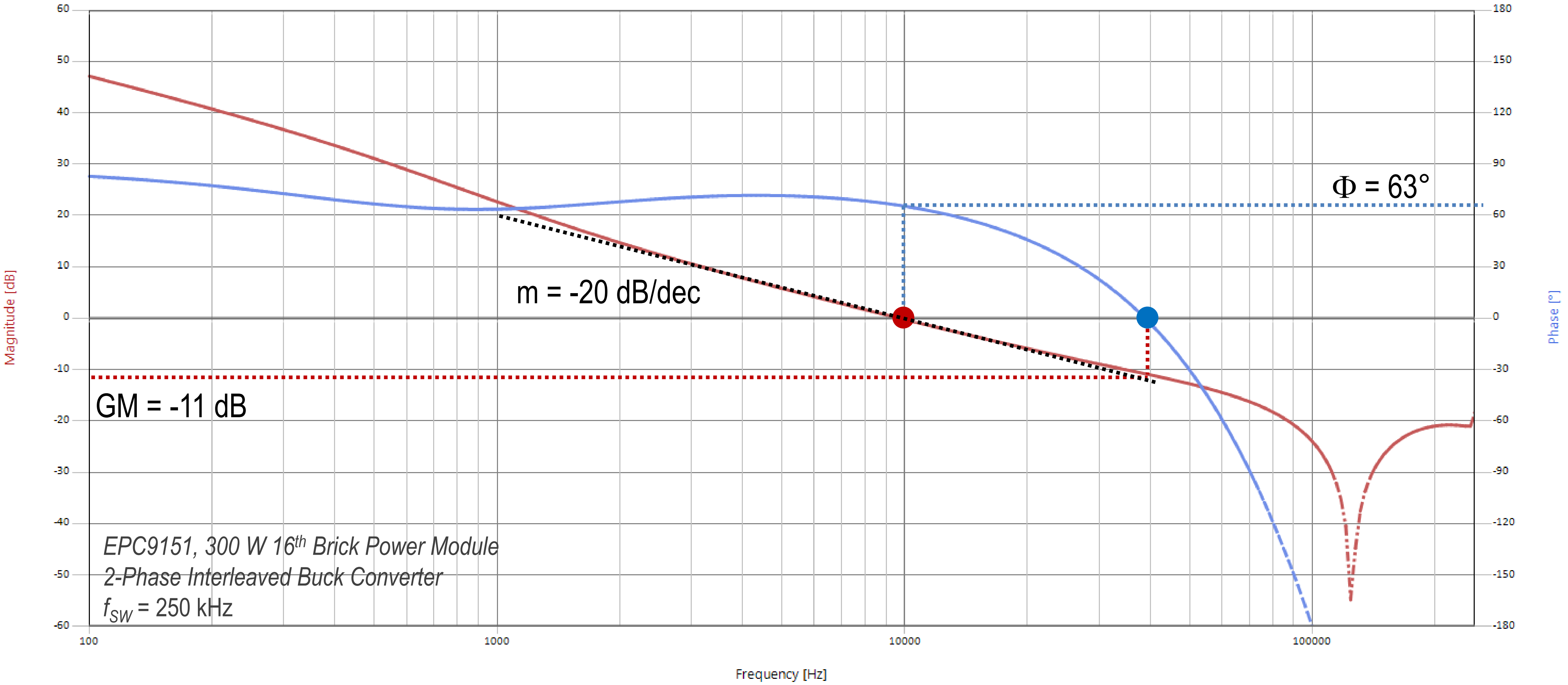


Voltage-to-Current Loop Synchronization

Fast Inner Current Loop Open Loop Transfer Function (f_X = 10 kHz)



EPC9151
300 W 16th Brick
Interleaved Buck Converter



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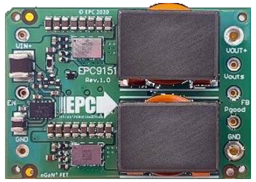
Voltage-to-Current Loop Synchronization

Slow Outer Voltage Loop Open Loop Transfer Function (f_X = 1.2 kHz)



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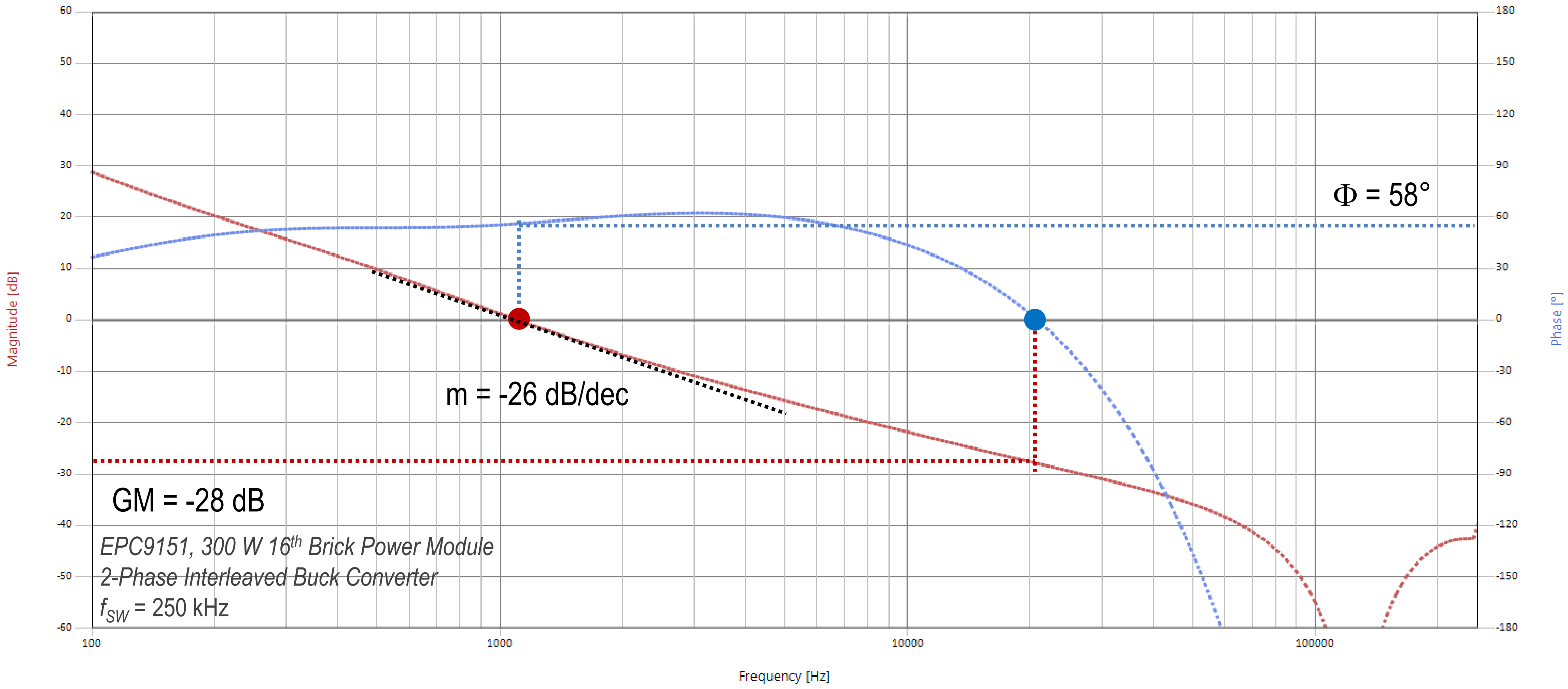

Voltage-to-Current Loop Synchronization

Approach #2: Low Gain Voltage Loop

- **Results**
  - Very good high frequency noise rejection without additional filtering
  - Minimum perturbation of current reference
  - **Low bandwidth response**

- **Applicable**
  - Battery chargers
  - LED Drivers
  - Low-Performance DC/DC Converters
  - Power Factor Correction

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- Enforced Phase-Locking Method
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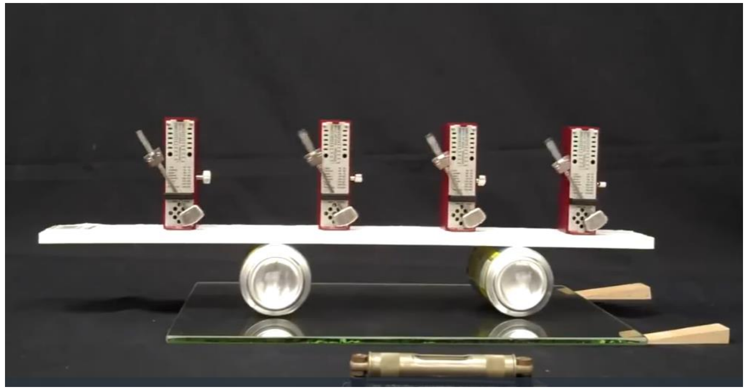
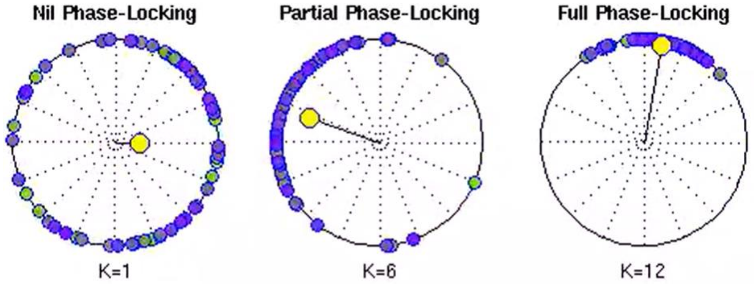
Kuramoto Synchronization *

Approach #3: Enforced Phase-Locking Method

- *This is *not* a Kuramoto model implementation but warm Thank You to Yoshiki Kuramoto for pointing us into the right direction
- And to OMCRON Lab giving us the tool we needed to work out how to implement it ☺



Kuramoto Oscillators



Nil, partial and full phase-locking in an all-to-all network of Kuramoto oscillators. Phase-locking is governed by the coupling strength K and the distribution of intrinisic frequencies ω. Here, the intrinsic frequencies were drawn from a normal distribution (M=0.5Hz, SD=0.5Hz). The yellow disk marks the phase centroid. Its radius is a measure of coherence.

- The Kuramoto model in Mechanics describes the synchronization of a large set of coupled oscillators.
- **Famous example:** self-synchronization of metronomes swinging at different frequencies being forced into synchronization by being coupled through a moving base.

“Kuramoto” Synchronization*

Approach

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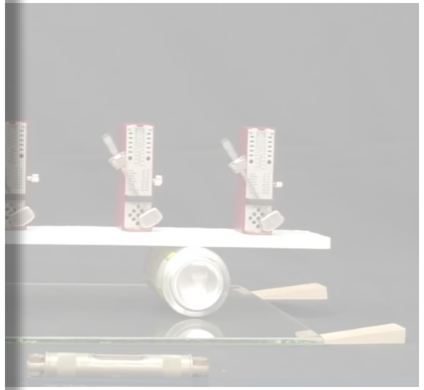
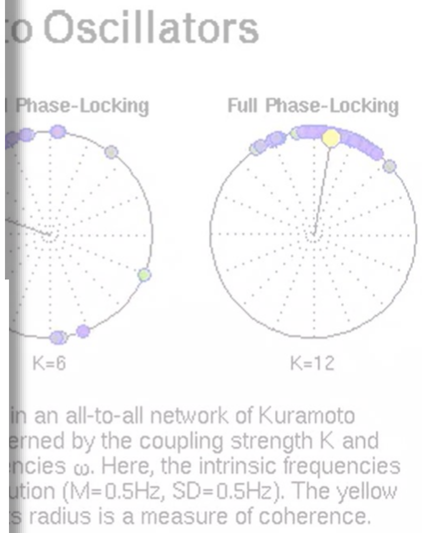
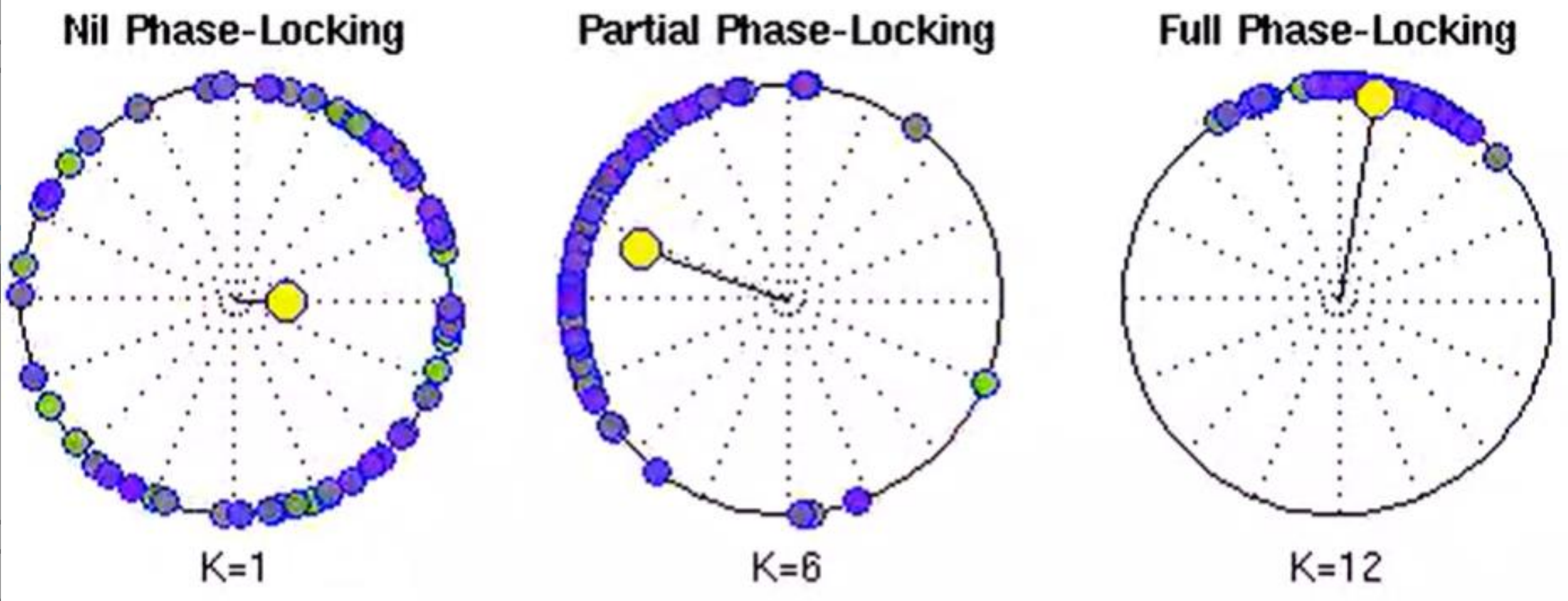




Kuramoto Oscillators

*Screenshot of animation on Wikipedia



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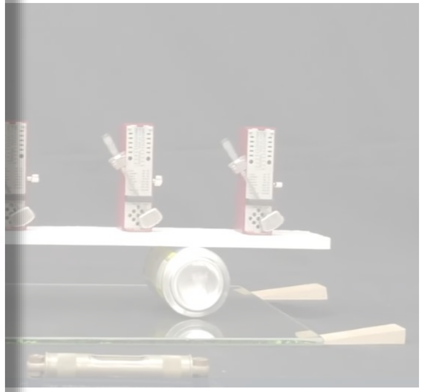

Kuramoto Oscillators

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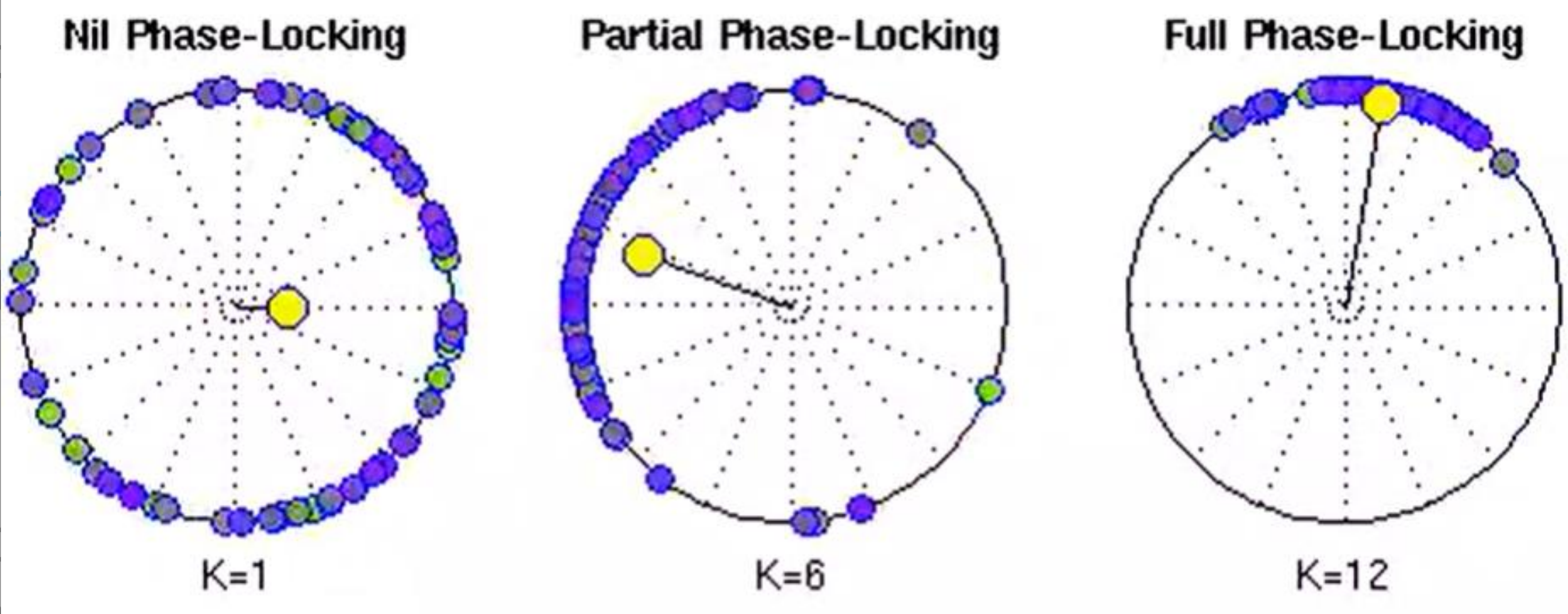
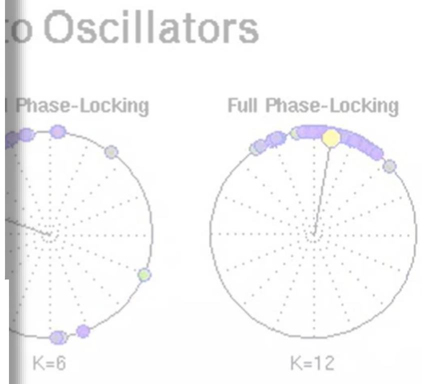


Nil, partial and full phase-locking in an all-to-all network of Kuramoto oscillators. Phase-locking is gov… c frequencies ω. Here, t… (M=0.5Hz, SD=0.5H… easure of coherence.

Does not apply for power supplies as the plant is not a strong coupling medium.

But is there another way to enforce full phase-locking?



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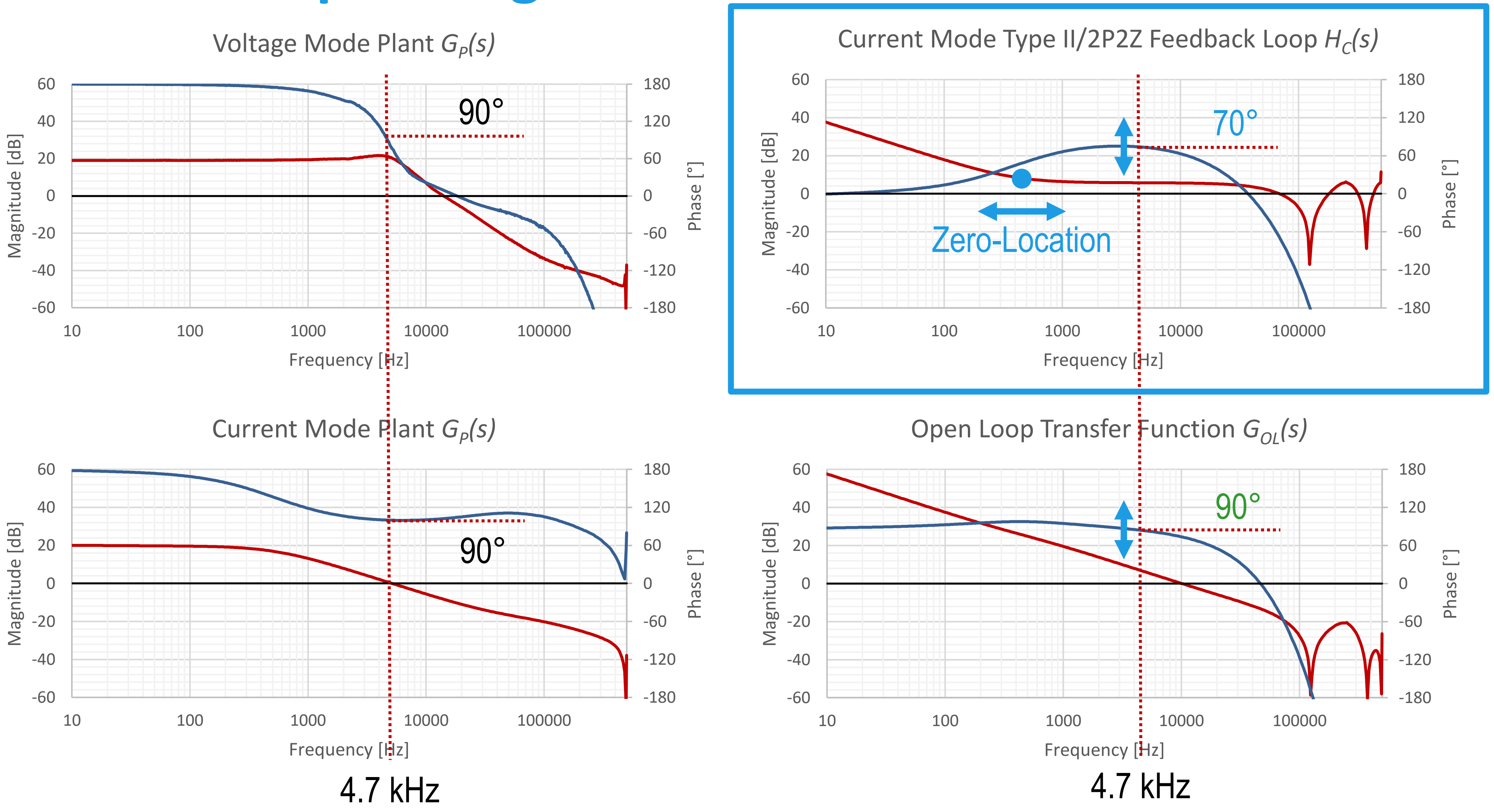
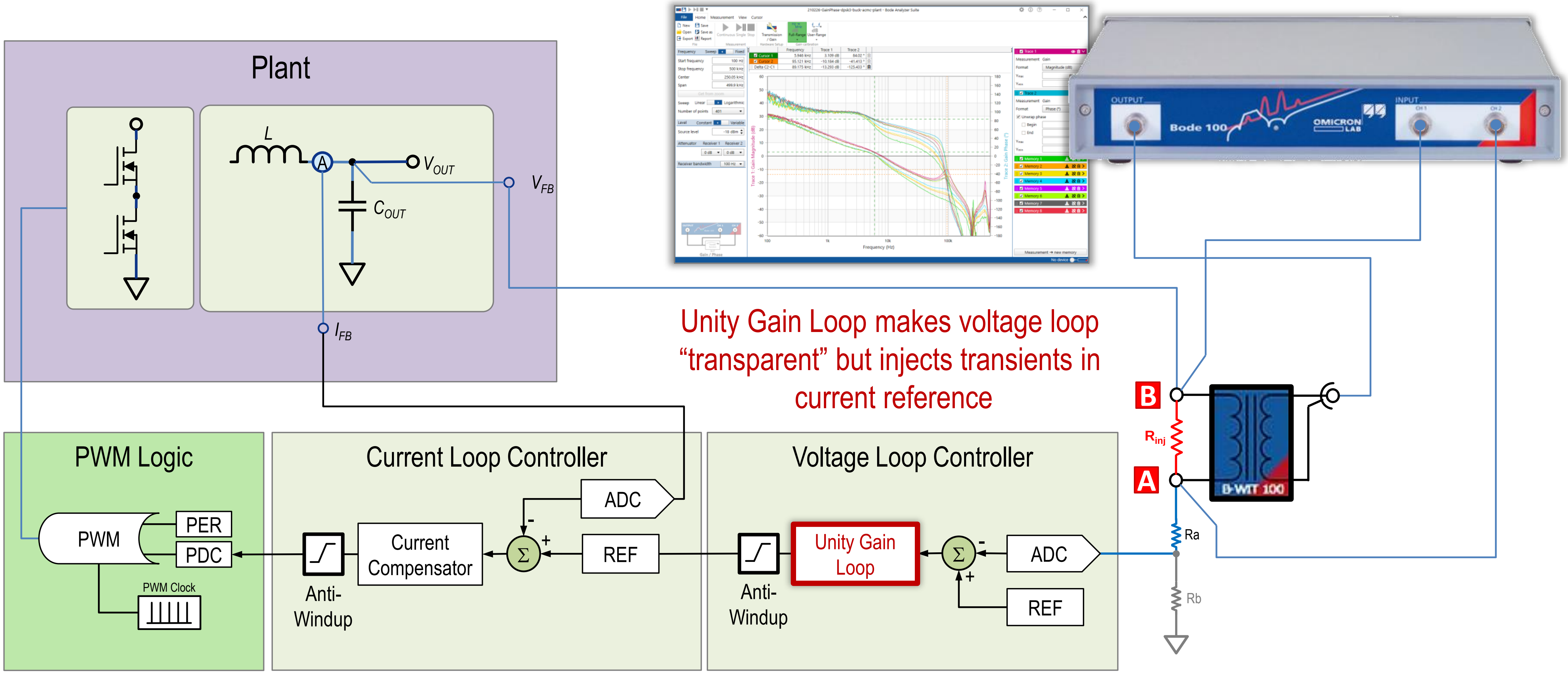
Enforced Phase-Locking Method

Inner Current Loop Tuning



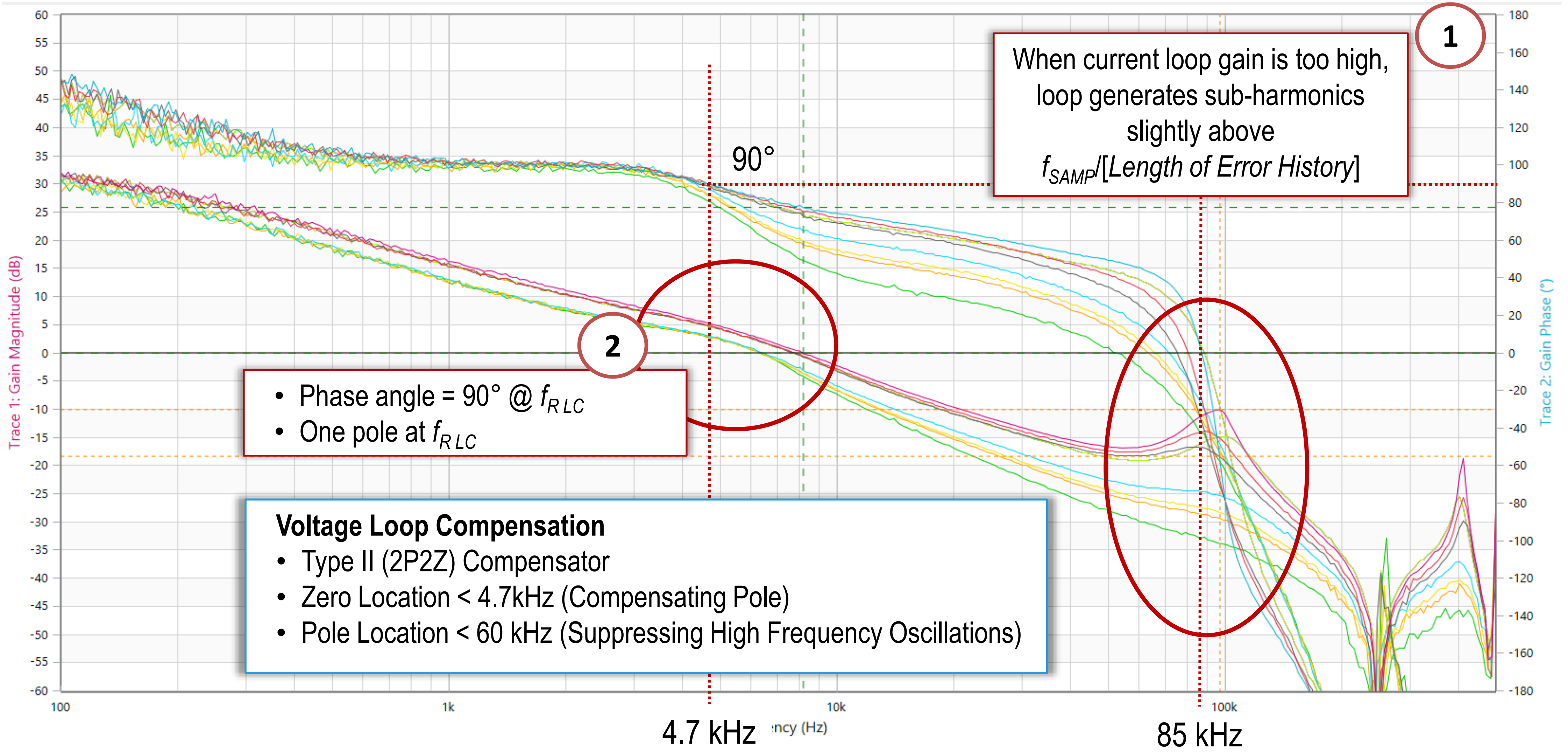
Alternate Current Plant Measurement

Current Plant seen from Voltage Loop



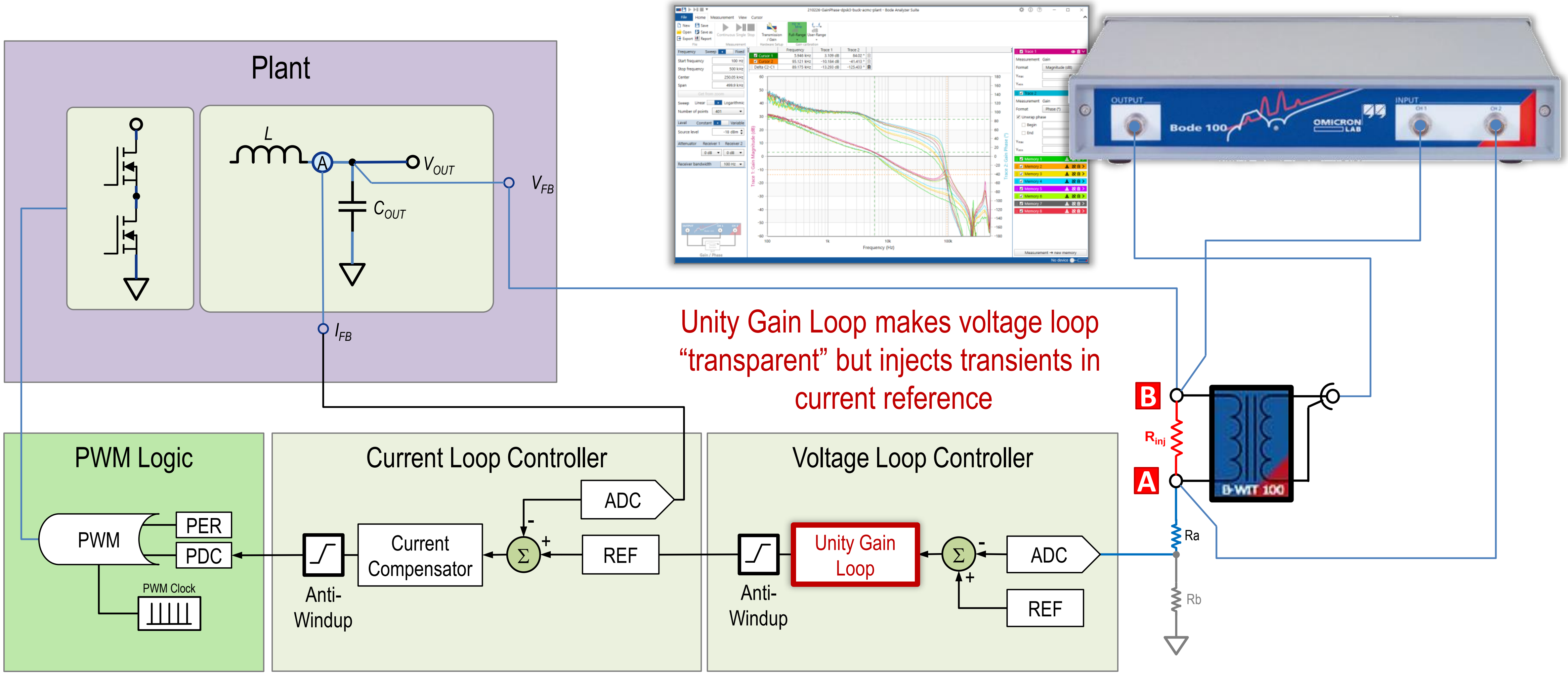
Enforced Phase-Locking Method

Results: Voltage Response of Current Loop Plant



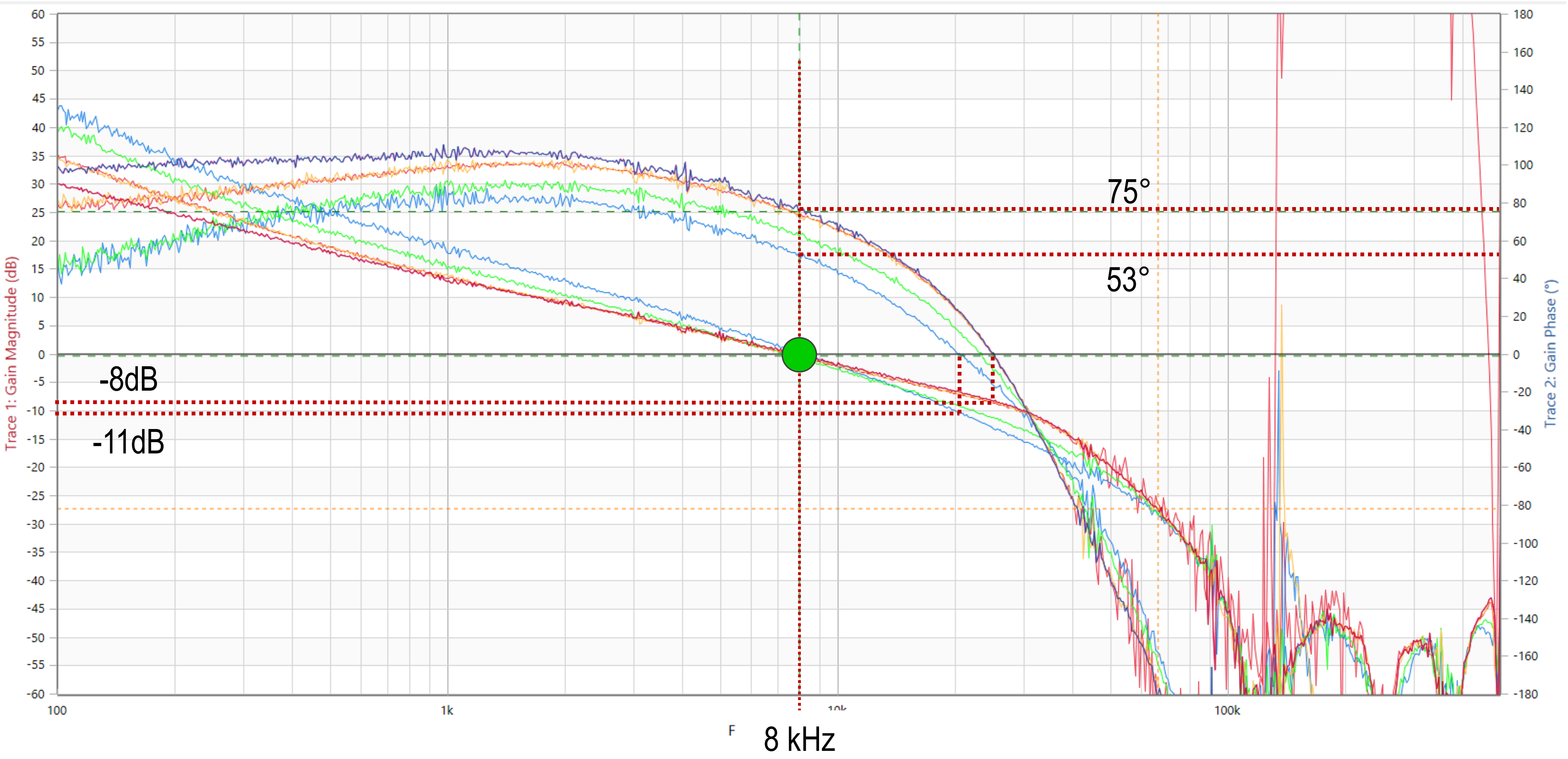
Alternate Current Plant Measurement

Current Plant seen from Voltage Loop



Enforced Phase-Locking Method

Average Current Mode Control Open Loop Transfer Function Results



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Enforced Phase-Locking Method

Wrap-Up

- **Most Recent Results**
  - Enforced Phase-Locking of Voltage and Current loop result in a stable and reliable system
  - As a result, Current Loop is slower than the Voltage Loop
  - Until today, results only verified on forward-type converters with fast current sense circuits

- **Future Work**
  - Evaluation of application in other topology types
  - Evaluation of impact of current feedback bandwidth/phase shift limitations

Agenda

Power Supply Control Modes

Average Current Mode Control Implementation

Enforced Phase-Locking Method

Summary

Summary

- **Average Current Mode Control is a universal control mode applicable in**
  - Constant Current and Constant Voltage Sources
  - PFC and DC/DC Converters
  - Battery Chargers & LED Drivers
  - Allows current-oriented control algorithms (e.g. MPPT, Bidirectional Control)
  - Sustained Current Limit capability
- **Less restrictive on current feedback quality**
  (simplifies current sense circuits)

- **Higher CPU load in digital control loop implementations**
- **Classic configurations have limited bandwidth**
- **Promising: Phase-Locking may be key to mitigate bandwidth limitations**

Q & A

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Thank You!

May the power be with you!

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