

Designing Digital Control Loops and Firmware for Switch-Mode Power Supplies



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

Digital Control of Switch-Mode Power Supplies

Presented by Andreas Reiter

April 17th 2024



SMART | CONNECTED | SECURE



Power
Conversion

Agenda



Digital Power Supply Control Overview



Rapid Prototyping



System Firmware Development & Test



Summary

Agenda



Digital Power Supply Control Overview



Rapid Prototyping



System Firmware Development & Test



Summary

Different Flavors of Digital Control

- **Encapsulated**
 - Switchers and PWM Controllers with digital logic providing enhanced features, usually configured in hardware (e.g. resistors, capacitors)
- **Integrated, Software Configurable**
 - Switchers and PWM Controllers with digital interfaces (e.g. I2C/PMBus™) to be configured by external, proprietary software (PC) or an external MCU
- **Integrated, Programmable**
 - Switchers and PWM Controllers with open MCU core and dedicated peripherals require firmware development design & programming tools
- **Discrete, Programmable**
 - Bare MCUs/DSPs to be fully programmed by end-user, requiring external auxiliary power supply and components

DSP Special Requirements



- **Low-Noise Design Guidelines**

- Power Supply and Power Integrity
- Signal Integrity and ADC Front-End Design



- **Protection & Safety**

- FuSa Manuals (ISO26262) provided by CPU vendor



- **Firmware Robustness & Quality Guidelines**

- Motor Industry Software Reliability Association MISRA-C
- (A)SIL Standards IEC 61508, ISO 26262, IEC 60730

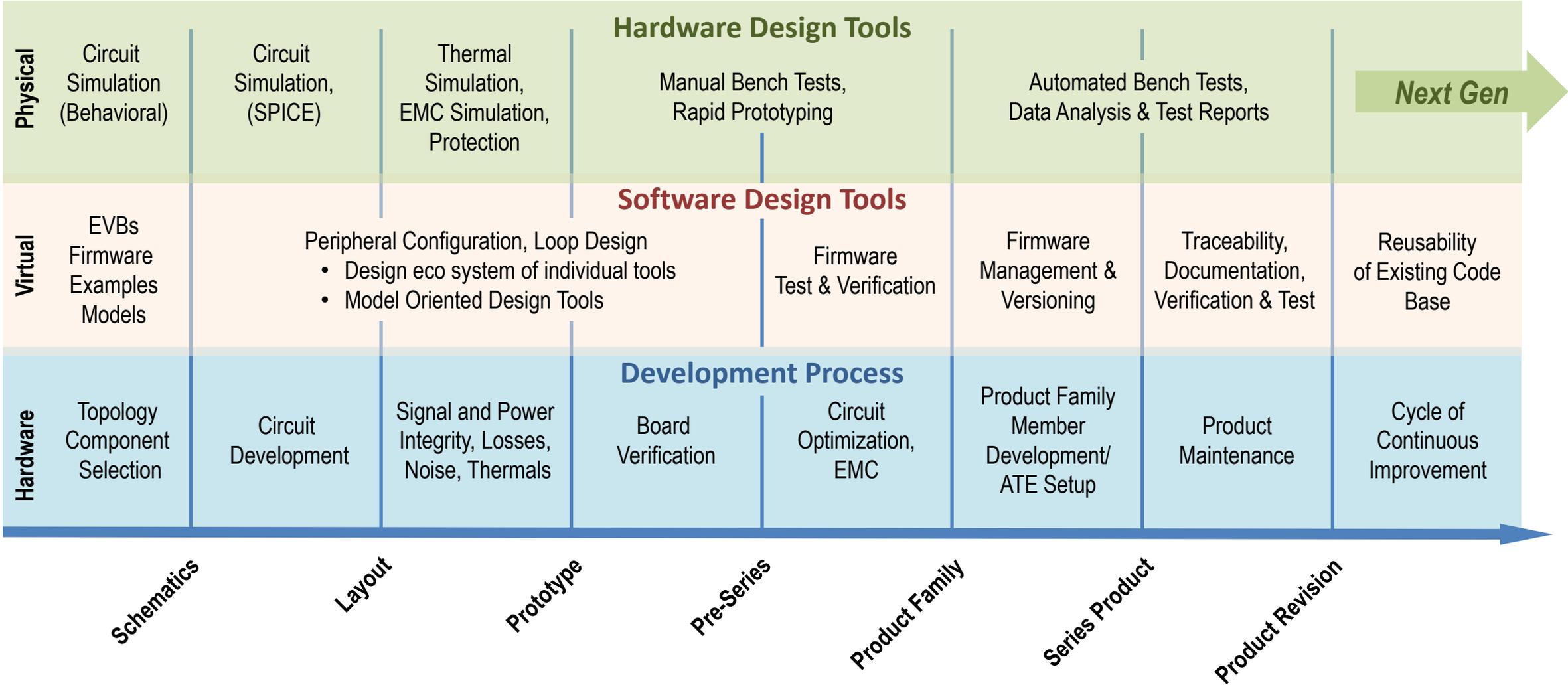


- **Firmware Management & Versioning**

- Git, Distributed Team Collaboration Versioning Tool (e.g. Github, Bitbucket)
- **(Automotive) Software Process Improvement Capability dEtermination**
(A)SPICE

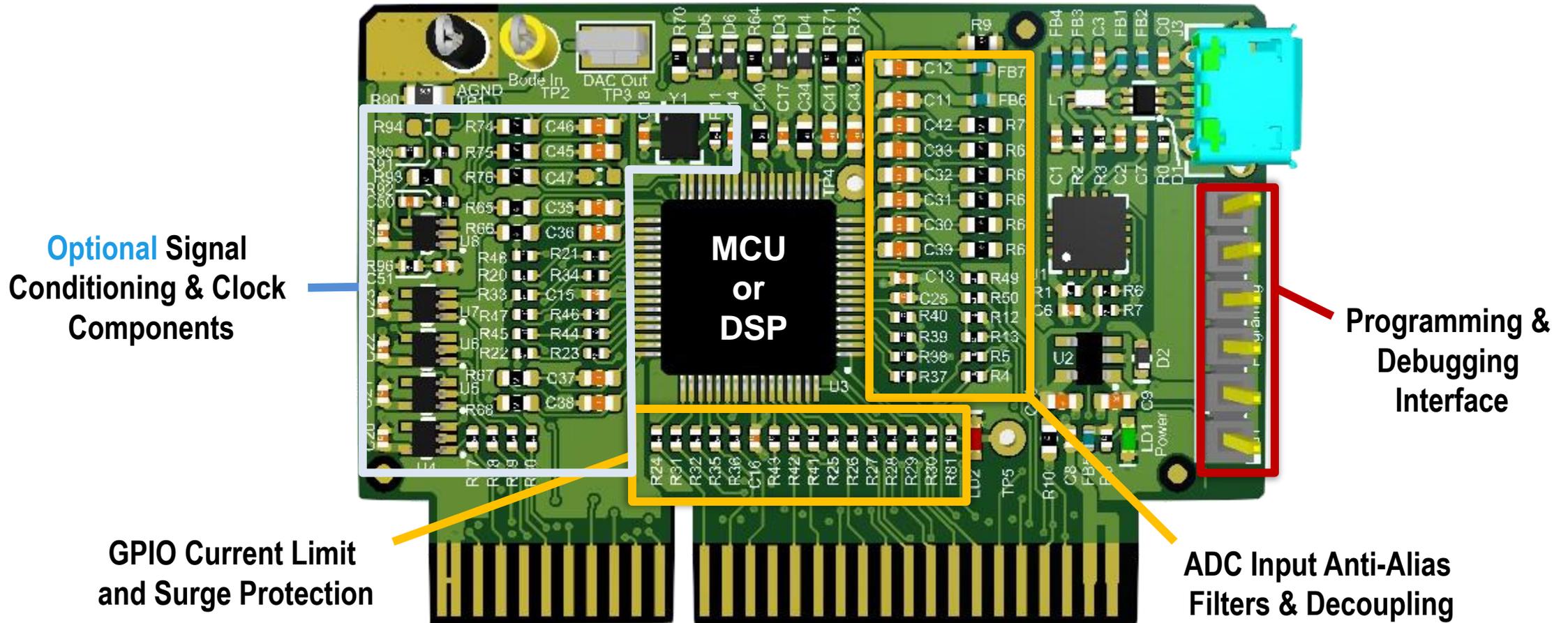
Switch-Mode Power Supply Design Process

From Schematics to Production and beyond



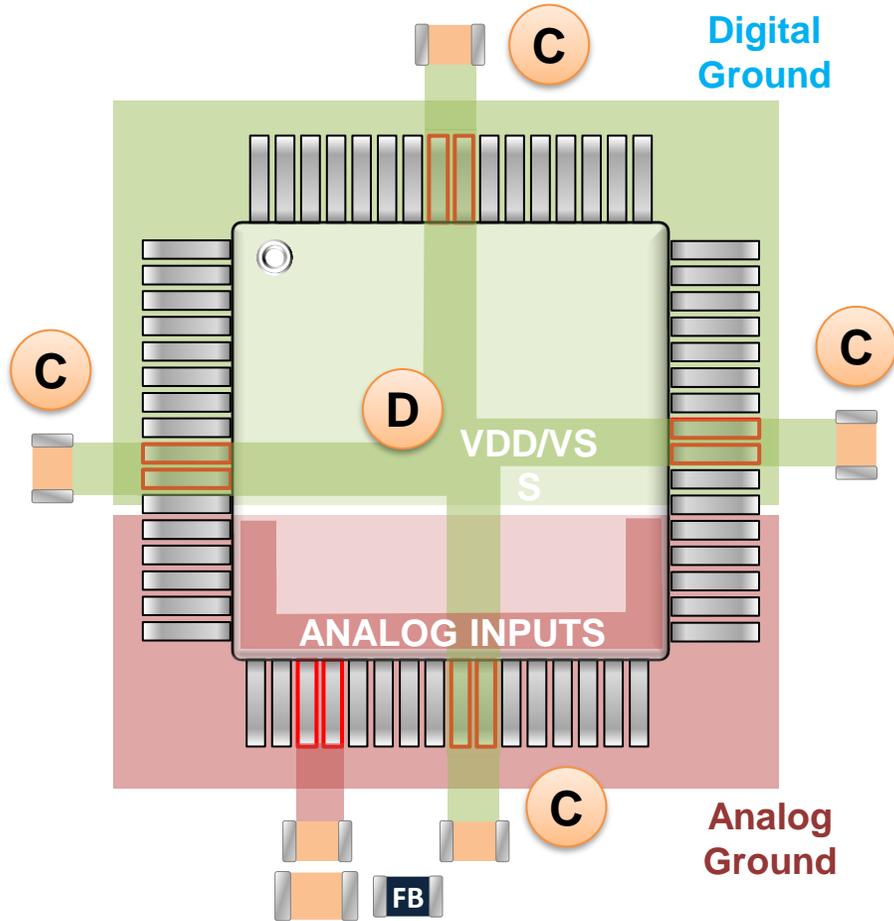
EVBs & Circuit Design Guidelines

Example: dsPIC33CK512MP606 Digital Power Plug-In Module

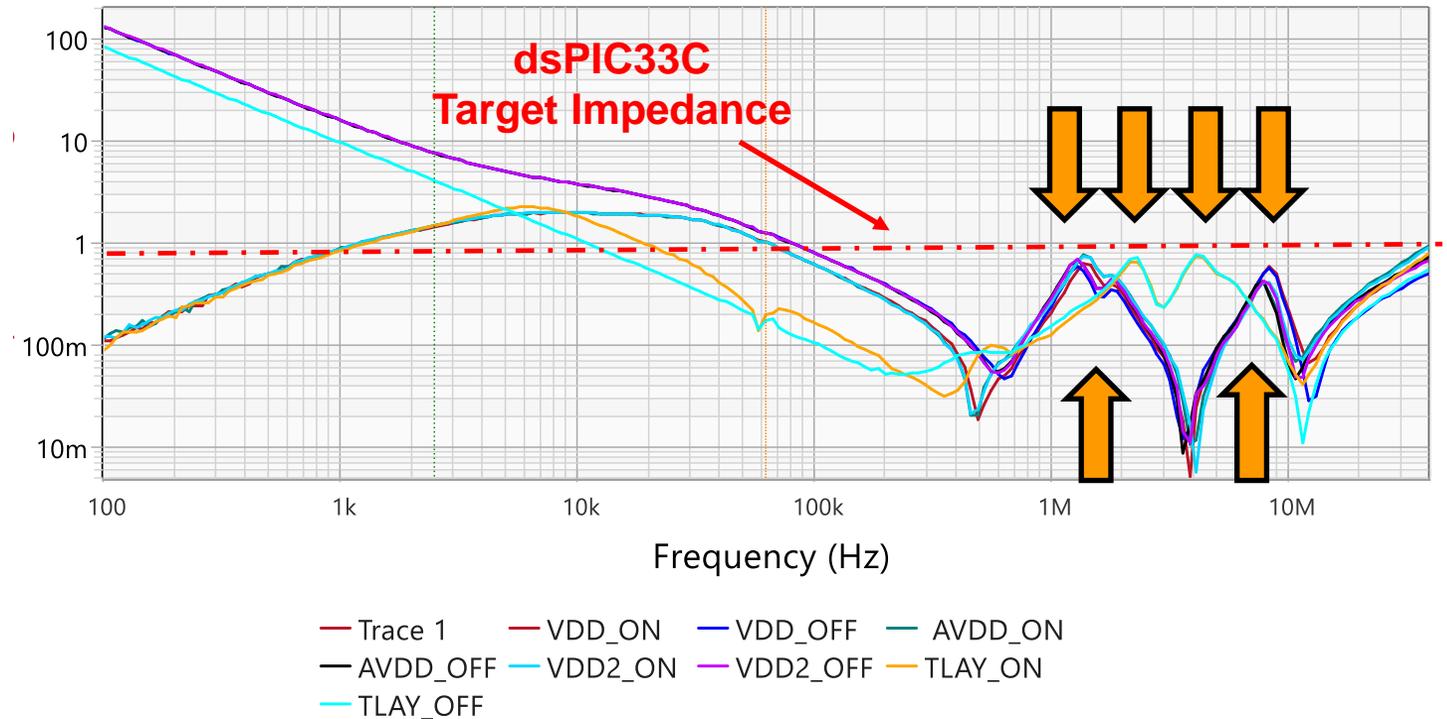


Low-Noise Design Guidelines

Supply Rail Impedance Profile Measurement



VDD Impedance profile measured at every decoupling capacitor (unpowered and powered)



Digital Power Development Hardware

- **Starter Kits**

Compact boards for conceptual evaluation and basic education, no further tools required

- **Evaluation Boards**

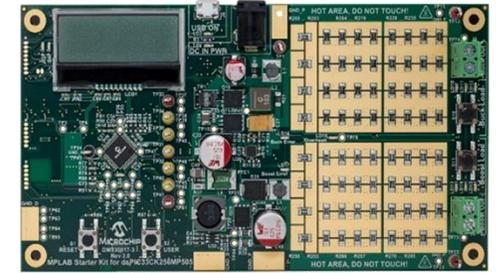
Dedicated designs build to showcase control methods, topologies and component performance

- **Development Boards**

Robust, well protected topology boards designed for firmware development and enhanced debugging and analysis

- **Reference Designs**

“Close to Production” designs templates



Agenda



Digital Power Supply Control Overview



Rapid Prototyping



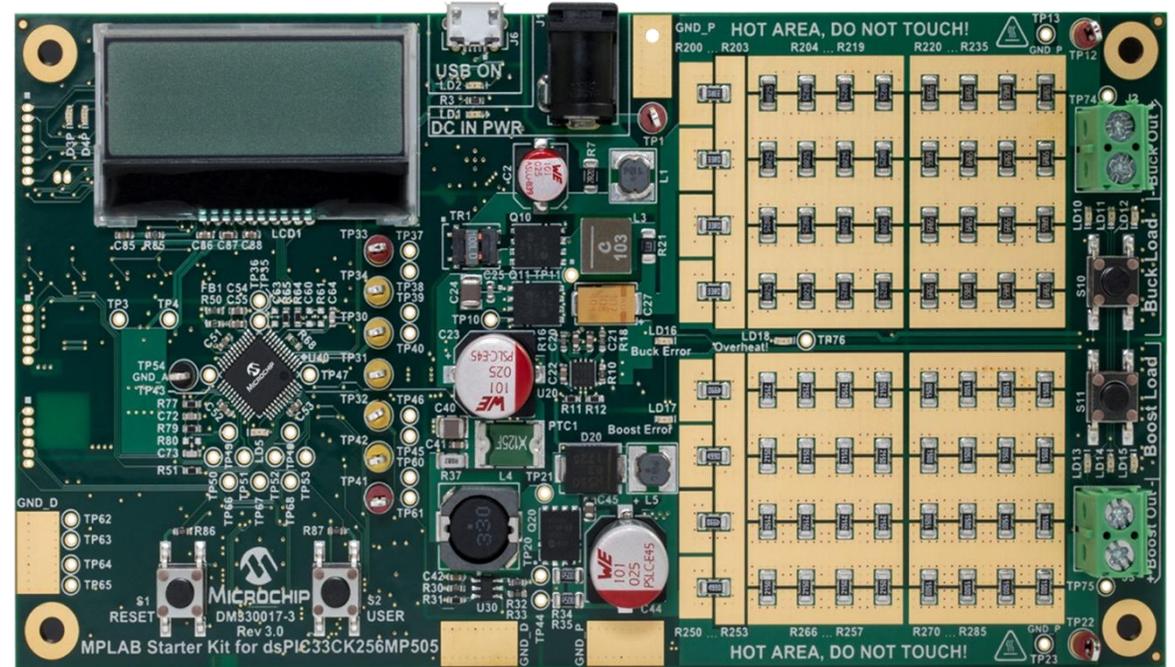
System Firmware Development & Test



Summary

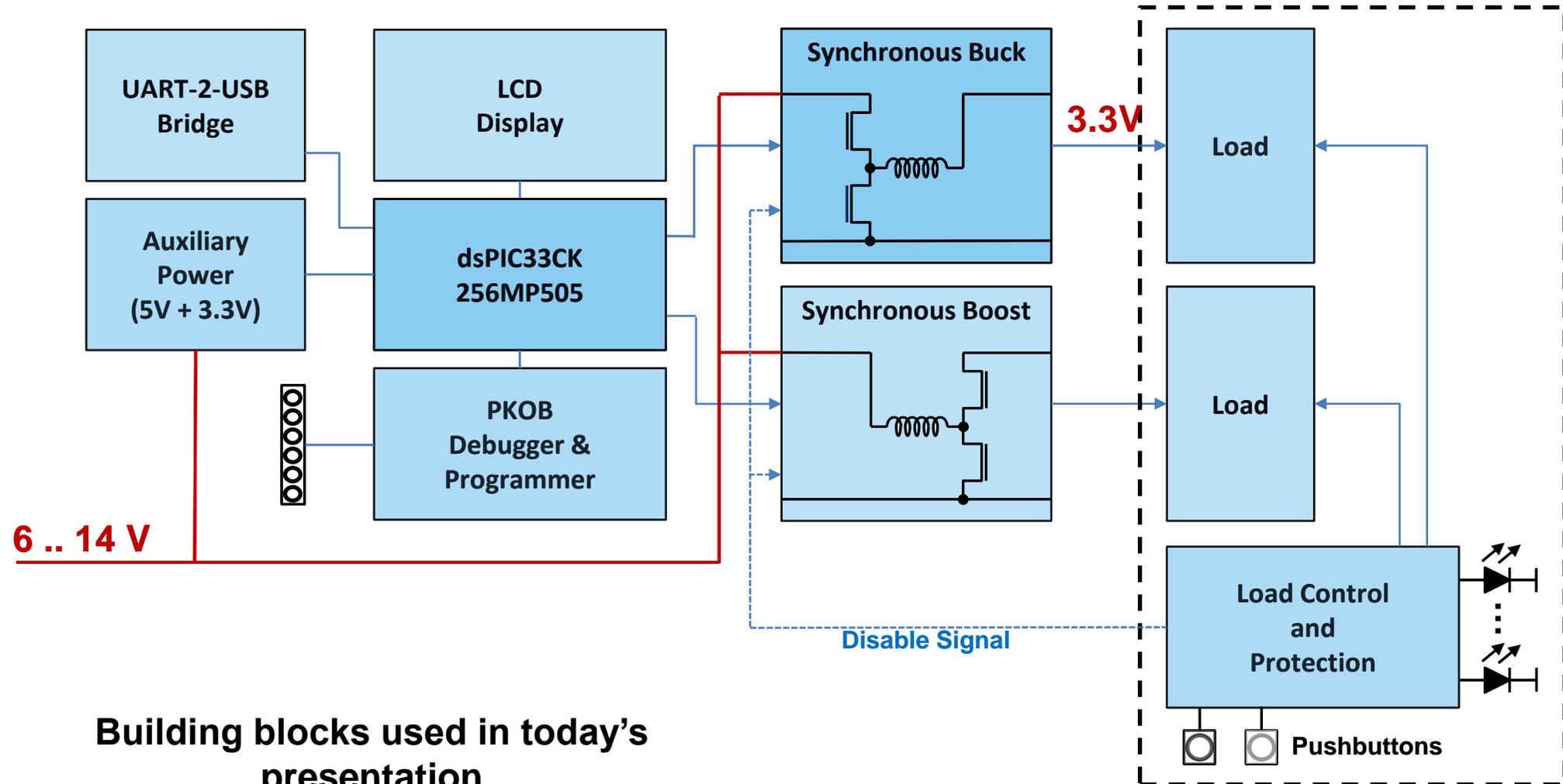
dsPIC33C Digital Power Starter Kit (DPSK3)

- On-board dsPIC33CK256MP505 DSC
- PIC24F Auxiliary Microcontroller managing loads and protection circuit auto recovery
- Two Independent DC/DC Converter Topologies:
 - Synchronous Buck Converter
 - Asynchronous Boost Converter
- Independent resistive loads
 - Four selectable Constant Load Levels
 - Three Selectable Step Load Levels
- Protection circuitry
 - Over Current Protection (OCP)
 - Over Voltage Protection (OVP)
 - Over Temperature Protection (OTP)
- Development Features
 - PKOB4 On-Board Programmer/Debugger
 - LC Display User Interface
 - USB/UART Bridge (Standard VCP)



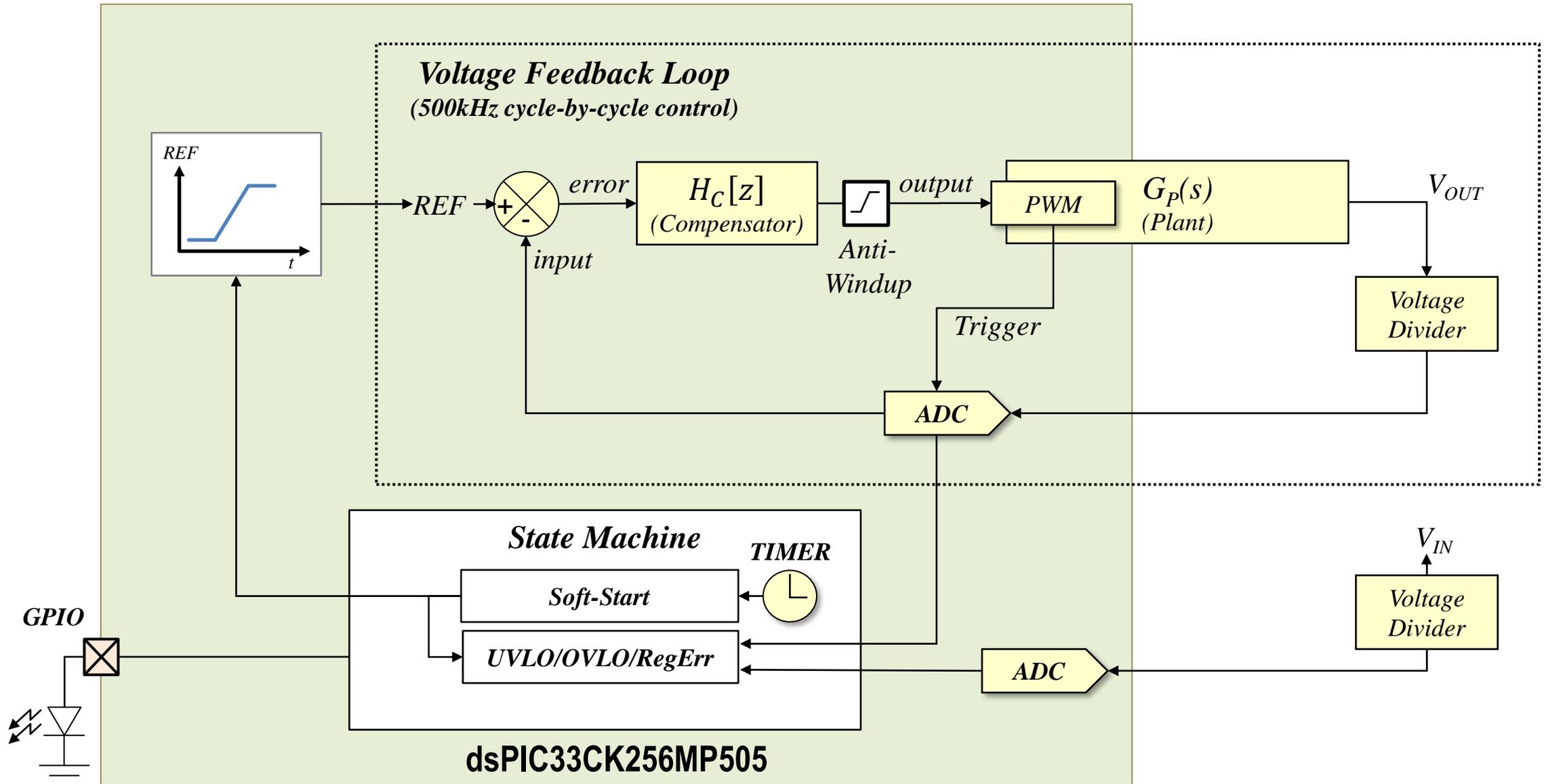
Part-No: DM330017-3

dsPIC33C Digital Power Starter Kit 3 (DPSK3)

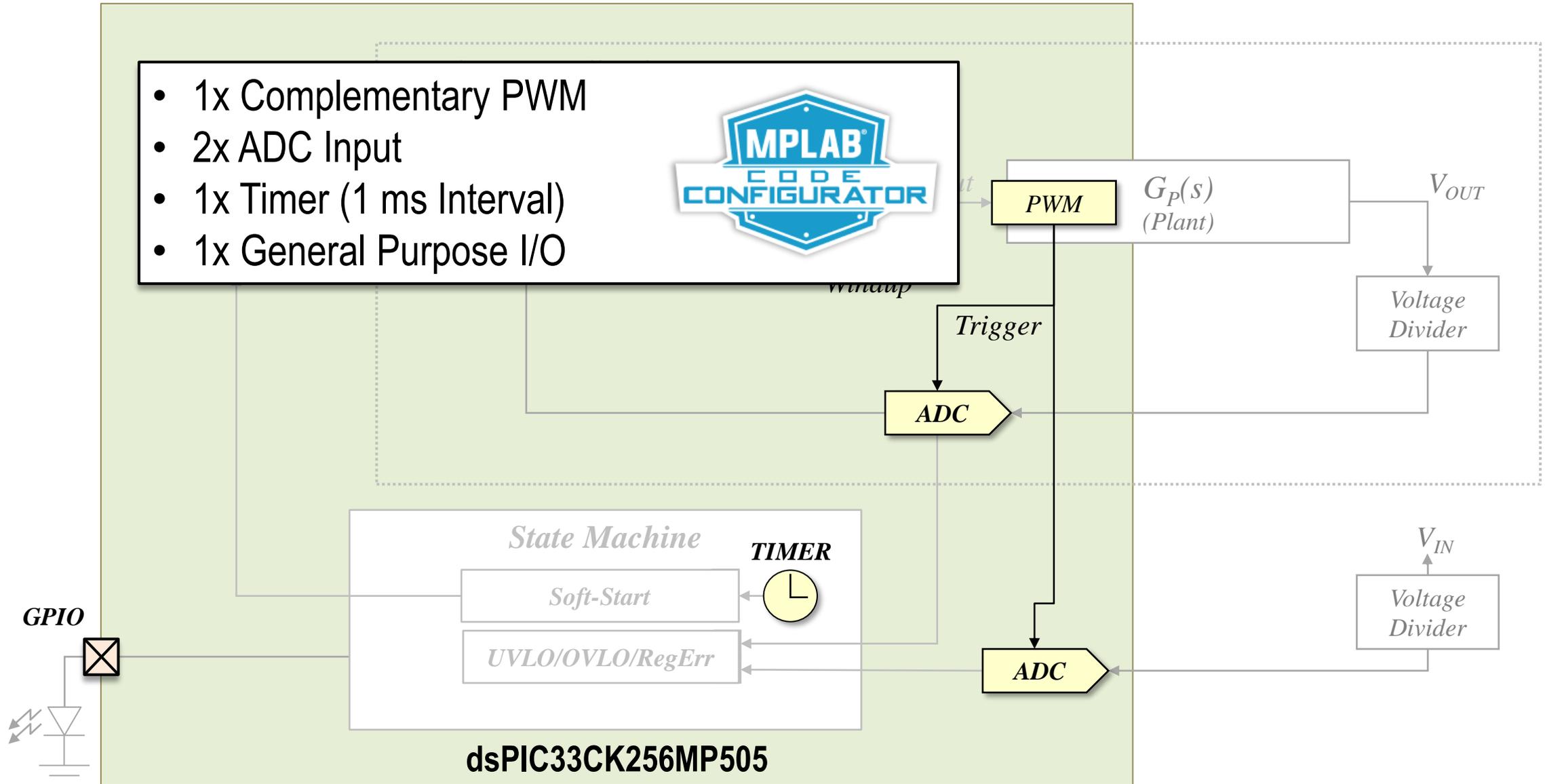


Building blocks used in today's presentation

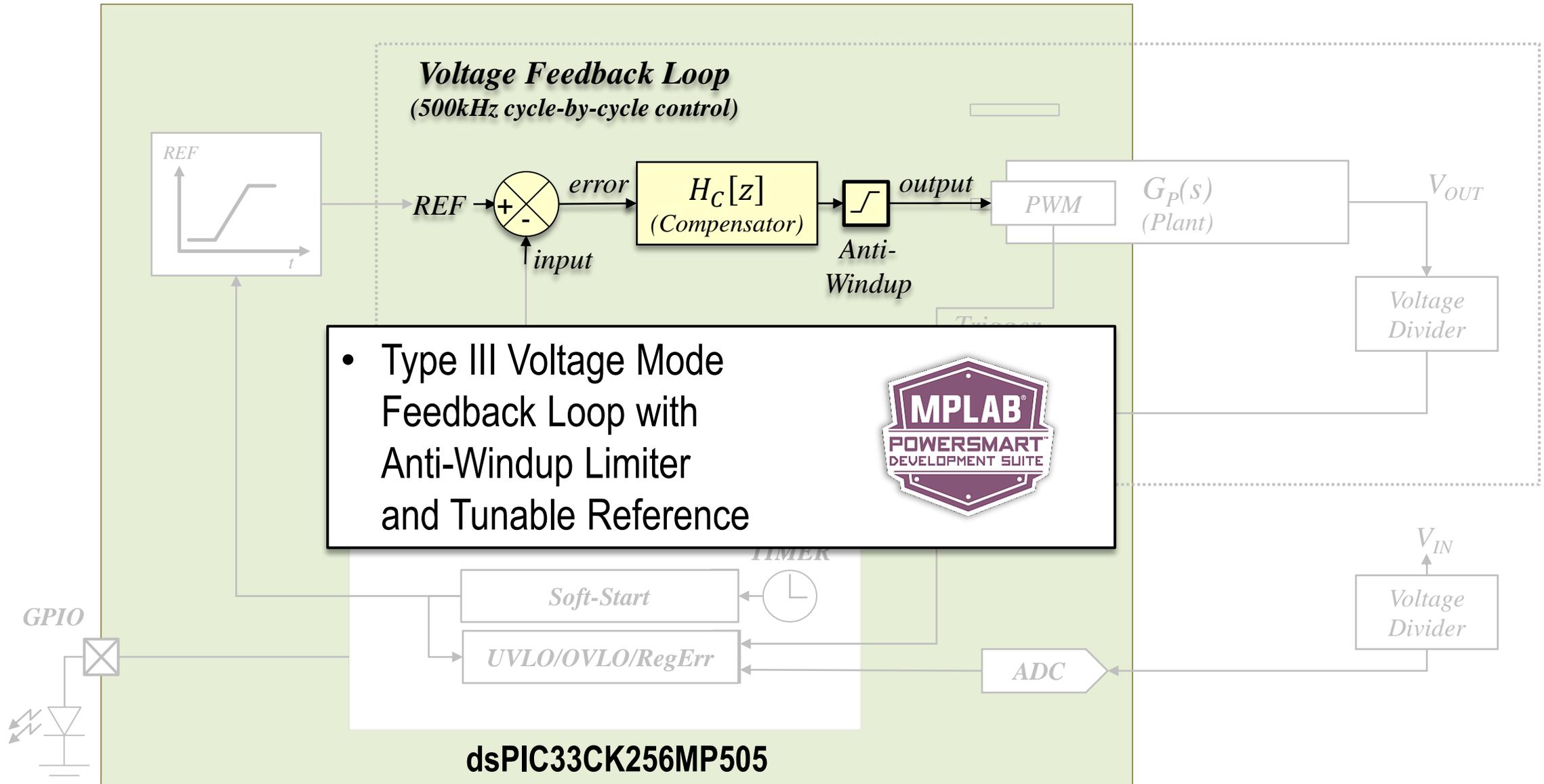
Control Software Block Diagram



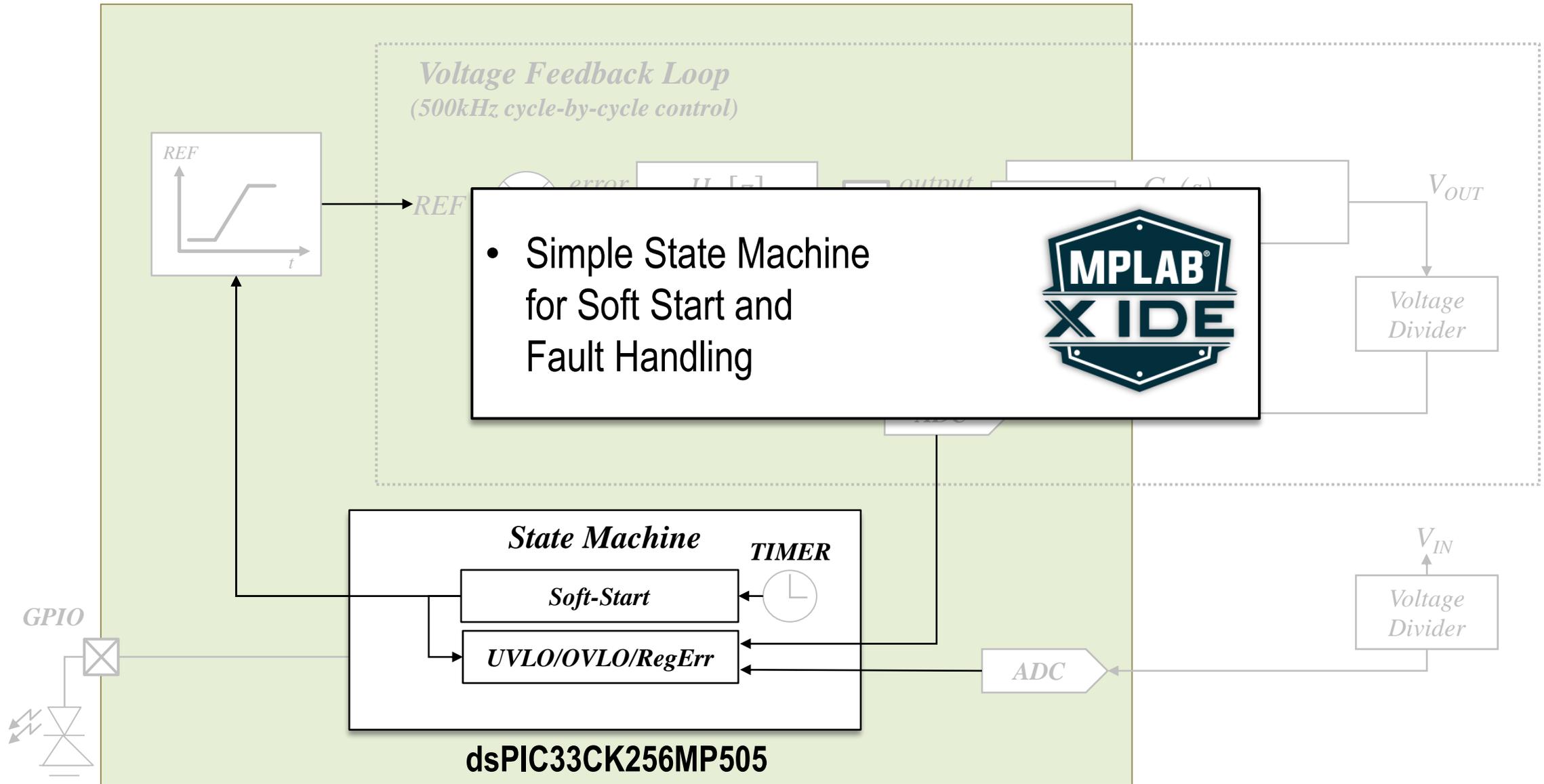
Control Software Block Diagram



Control Software Block Diagram



Control Software Block Diagram

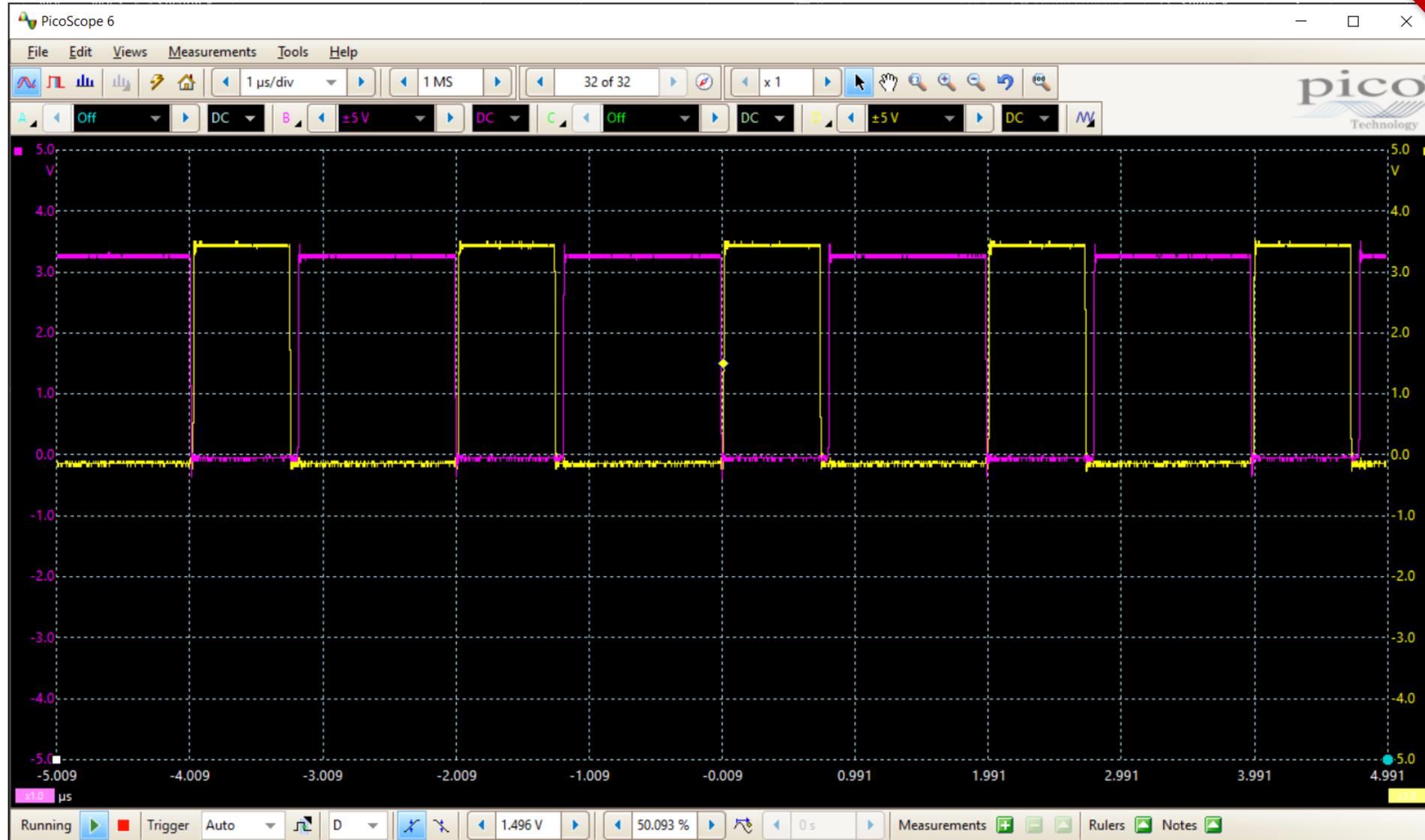


MCU Configuration MPLAB® Code Configurator

The screenshot displays the MPLAB X IDE v6.05 interface with the MPLAB Code Configurator (MCC) plugin. The main window shows the configuration for a dsPIC33CK256MP505 microcontroller in the QFN48 package. The Pin Manager is active, showing a grid view of pin configurations for three ports: Port A, Port B, and Port C. The grid shows the module, function, and direction for each pin, with some pins configured as inputs or outputs.

Module	Function	Direction	Port A				Port B				Port C									
			0	1	2	3	0	1	2	3	0	1	2	3						
Clock	CLKI	input																		
	CLKO	output																		
	OSCI	input																		
	OSCO	output																		

Program & Run Target Device



Complete Rapid Prototyping Course



Creating a Digital Power Supply

mu.microchip.com/creating-a-digital-power-supply-from-scratch

MICROCHIP UNIVERSITY

Sign In

Creating a Digital Power Supply from Scratch

This class covers the entire process of creating a digital power supply. (Nov 2021)

Register | Free

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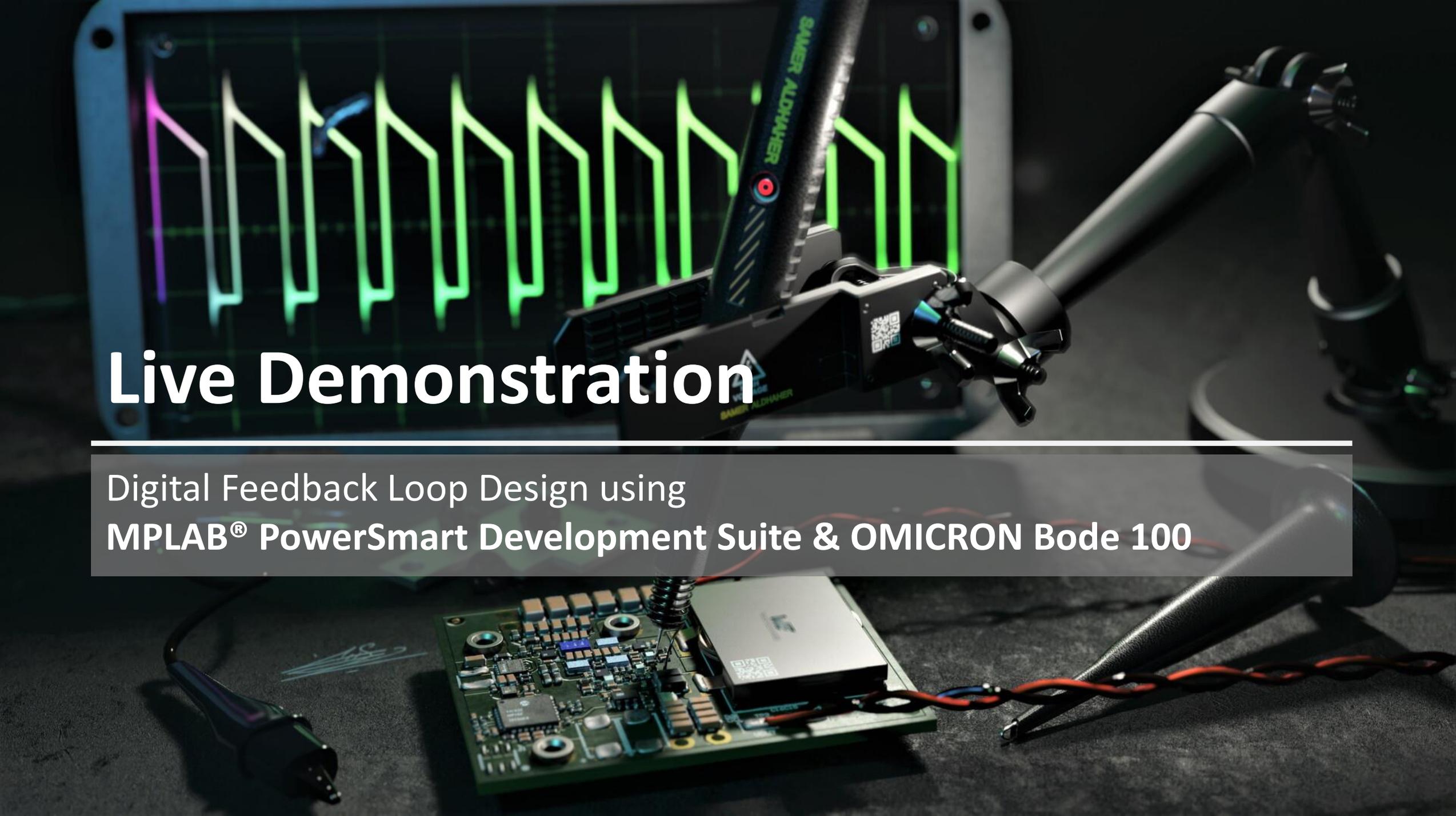
Share Post

About this course

This class covers the entire process of creating a digitally controlled synchronous buck power supply based on the

- Curriculum (73 min)**
- Syllabus
- Course Introduction (1 min)

Evaluation Environment

The image features a robotic arm in the foreground, holding a probe over a green printed circuit board (PCB). The PCB is populated with various electronic components, including a large silver component with a QR code. In the background, a screen displays a glowing green waveform, likely representing a digital signal. The overall scene is set in a dark environment, emphasizing the illuminated elements.

Live Demonstration

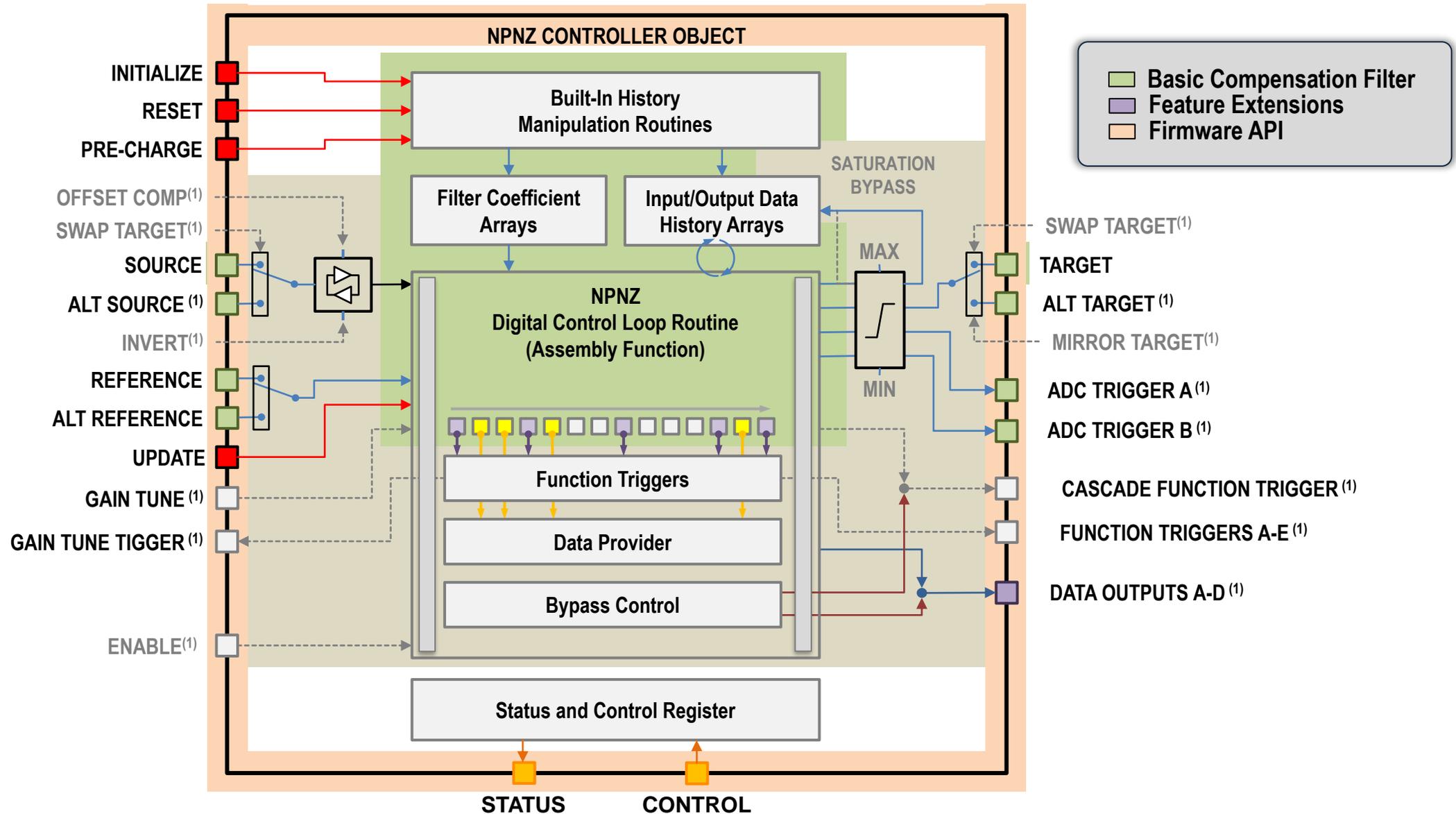
Digital Feedback Loop Design using
MPLAB® PowerSmart Development Suite & OMICRON Bode 100

MPLAB® PowerSmart™ Development Suite

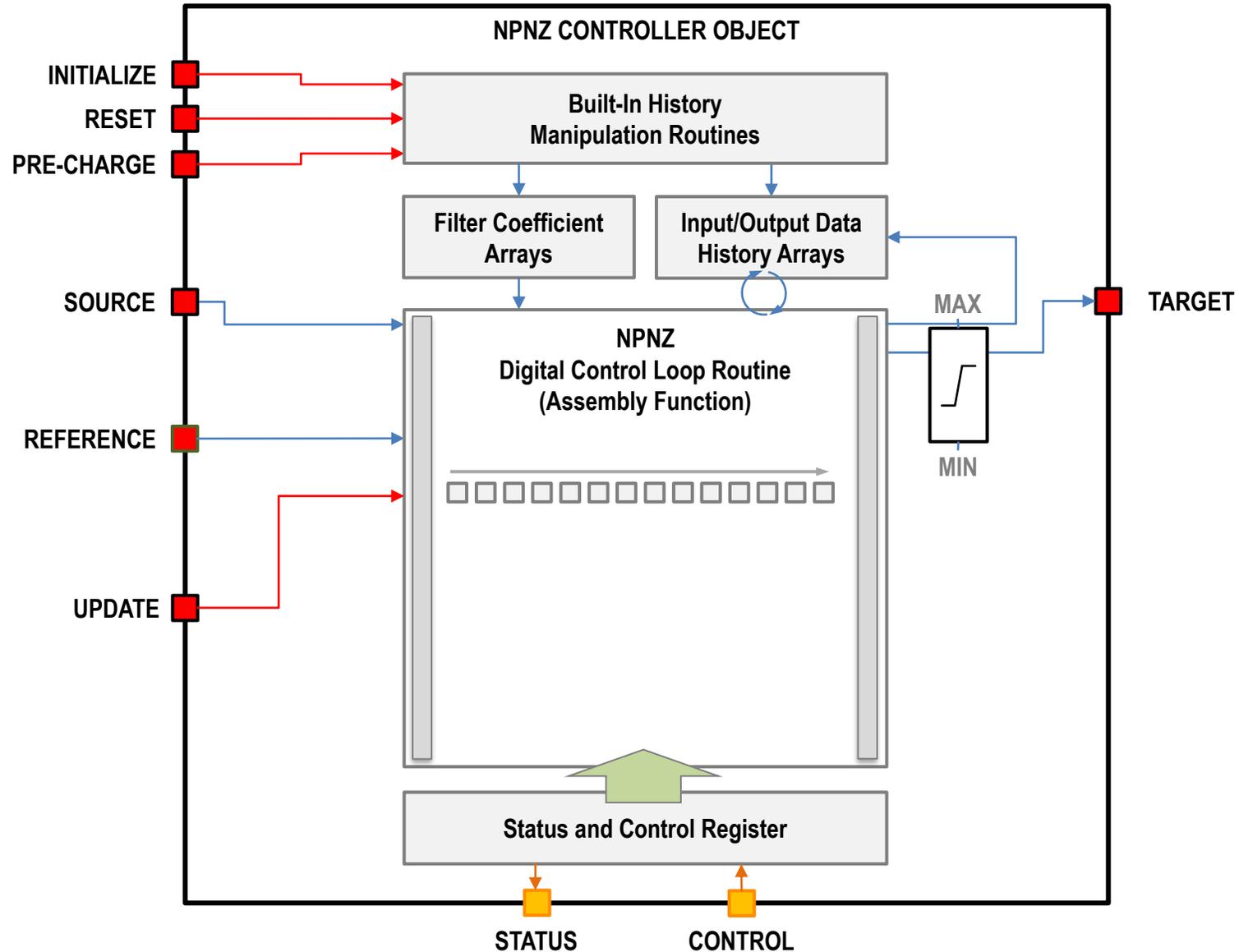
The screenshot displays the MPLAB PowerSmart Development Suite interface. The main window shows a block diagram titled "DPSK3 Type III (VMC)". The diagram illustrates a feedback loop system. A reference signal (REF) is summed (Σ) and fed into a "Voltage Loop Compensator H(z)" block, which is highlighted with a red border and labeled "Compensator Gain". This block is identified as "vComp 3P3Z Feedback Loop". The output of the compensator goes to a "PWM" block, which is also highlighted with a red border and labeled "Plant Gain". The PWM signal drives a "Converter Voltage Plant G(s)" block, also highlighted with a red border and labeled "Plant Gain". The output of the plant is VOUT. A feedback path from VOUT goes through a "TV(s)" block and an "ADC" block (with VREF input) back to the summing junction. The entire system is labeled "Voltage Mode Controller".

On the left side, the "Project Explorer" shows a tree structure with "MPLAB X IDE Project" expanded to show "Power Supply Control", "DPSK3 Type IV (VMC)", and "DPSK3 Type III (VMC)". A green arrow points from the "DPSK3 Type III (VMC)" entry to the "Feedback Loop Block" label. Below the Project Explorer is the "Component Library" with a search bar and a list of components including "Voltage Mode Control (VMC)", "Peak Current Mode Control (PCMC)", "Average Current Mode Control (ACMC)", "Generic Filter Libraries", and "Moving Average Filter". A "Description" box at the bottom left states: "Single, discrete Voltage Mode Control (VMC) loop controlling the output of a single power stage." A status bar at the bottom left shows a green checkmark and the text "Status: MPLAB® X IDE project loaded successfully".

Complete Feedback Loop Block Diagram



Basic Feedback Loop Block Diagram



Control Loop Adjustment

The screenshot displays the PowerSmart Digital Control Library Designer interface. The main window is titled "PowerSmart Digital Control Library Designer v1.9.15.709 - [New PowerSmart Project.pspj]". The interface includes a menu bar (File, View, Tools), a toolbar, and a central workspace. On the left, the "Controller" configuration panel is visible, with tabs for "Source Code Configuration" and "Advanced". The "Controller Selection" section shows "Controller Type" set to "4P4Z - Discrete Type IV Compensator" and "Scaling Mode" set to "4 - Fast Floating Point Scaling". The "Input Gain" section includes "Input Data Resolution" (12 Bit) and "Input Signal Gain" (0.500000). The "Compensation Filter Settings" section shows "Sampling Frequency" (500k Hz) and "Cross-over Frequency of Pole At Origin" (600 Hz). A red box highlights the "Pole & Zero Placement" section, which lists:

Pole 1:	75k Hz	Zero 1:	2k Hz
Pole 2:	100k Hz	Zero 2:	4k Hz
Pole 3:	180k Hz	Zero 3:	18k Hz

The central workspace displays a Bode plot with "Frequency Domain" selected. The plot shows Magnitude/Gain [dB] on the left y-axis (ranging from -40 to 40) and Phase [°] on the right y-axis (ranging from -180 to 180). The x-axis is Frequency [Hz] on a logarithmic scale (ranging from 100 to 100,000). The plot includes curves for Gain (z) in solid red, Phase (z) in solid blue, Gain (s) in dotted red, and Phase (s) in dotted blue. Vertical dashed lines indicate Pole Locations (green) and Zero Locations (yellow). The legend at the bottom identifies these elements: Gain (z), Phase (z), Gain (s), Phase (s), Pole Locations, and Zero Locations. A red arrow points to the "Compensator Type Selection" text, and another red arrow points to the "Pole & Zero Placement" text. The right sidebar contains "Bode Plot Settings" with fields for Frequency (Start: 100 Hz, Stop: 250k Hz, Points: 801), Magnitude/Gain (Min: -60 dB, Max: 60 dB, Div: 10 dB), Phase (Min: -180°, Max: 180°, Div: 30°), and Options (Unwrap Phase, Show s-Domain). The status bar at the bottom indicates "Coefficients generated successfully" and "Refresh Period: 18 ms".

Plant Measurement Setup

PowerSmart Digital Control Library Designer v2.3.0.1007 - [D:\Firmware\MCU16ASMP5...

File View Tools ?

Name Prefix: vComp

Create Array of Control Loops

Number of Control Loops: 1

Controller Source Code Configuration Advanced

Use P-Term Loop Controller for Plant Measurements

Nominal Feedback Level: 2047

Nominal Control Output: 3186

Fractional: 0.7781982421875

Scaler: -1

Enable Feedback Loop Gain Modulation (AGC)

Enable User Extensions

✓ Saving File:

Refresh Period: 10 ms Table Options

Nominal Feedback Level Calculator

Voltage Feedback Shunt Amplifier Current Transformer Digital Source

Circuit

Reference: 3.3 V

ADC Resolution: 12 Bit

Minimum: 0

Maximum: 4095

Nominal Sense Voltage: 3.298 V

R1: 1.0k Ω

R2: 1.0k Ω

Amplifier Gain: 1.000 V/V

Differential (signed)

Signal Gain:

Nominal Output Level Calculator

Fixed Frequency Variable Frequency Phase Shifted PWM

PWM Time Base

Device Type: dsPIC33C

Clock Frequency: 4.0G Hz

Divider: 1

Resolution: 250.0p sec

Maximum: 65535

Calculation

PWM Frequency: 500.0k Hz

PWM Period: 2.0u sec

PWM Period Count: 8000 ticks

Effective Resolution: 12.966 bit

Nominal Duty Ratio: 39.836 %

Signal Gain:

Bode Plot Settings

Frequency

Start: 10 Hz

Stop: 250k Hz

Points: 801

Magnitude/Gain

Min: -90 dB

Max: 90 dB

Div: 15 dB

Phase

Min: -180 $^\circ$

Max: 180 $^\circ$

Div: 30 $^\circ$

Options

Unwrap Phase

Show s-Domain

Input Gain Declaration

Output Gain Declaration

Plant Measurement

Unity Gain Loop (Proportional Controller):

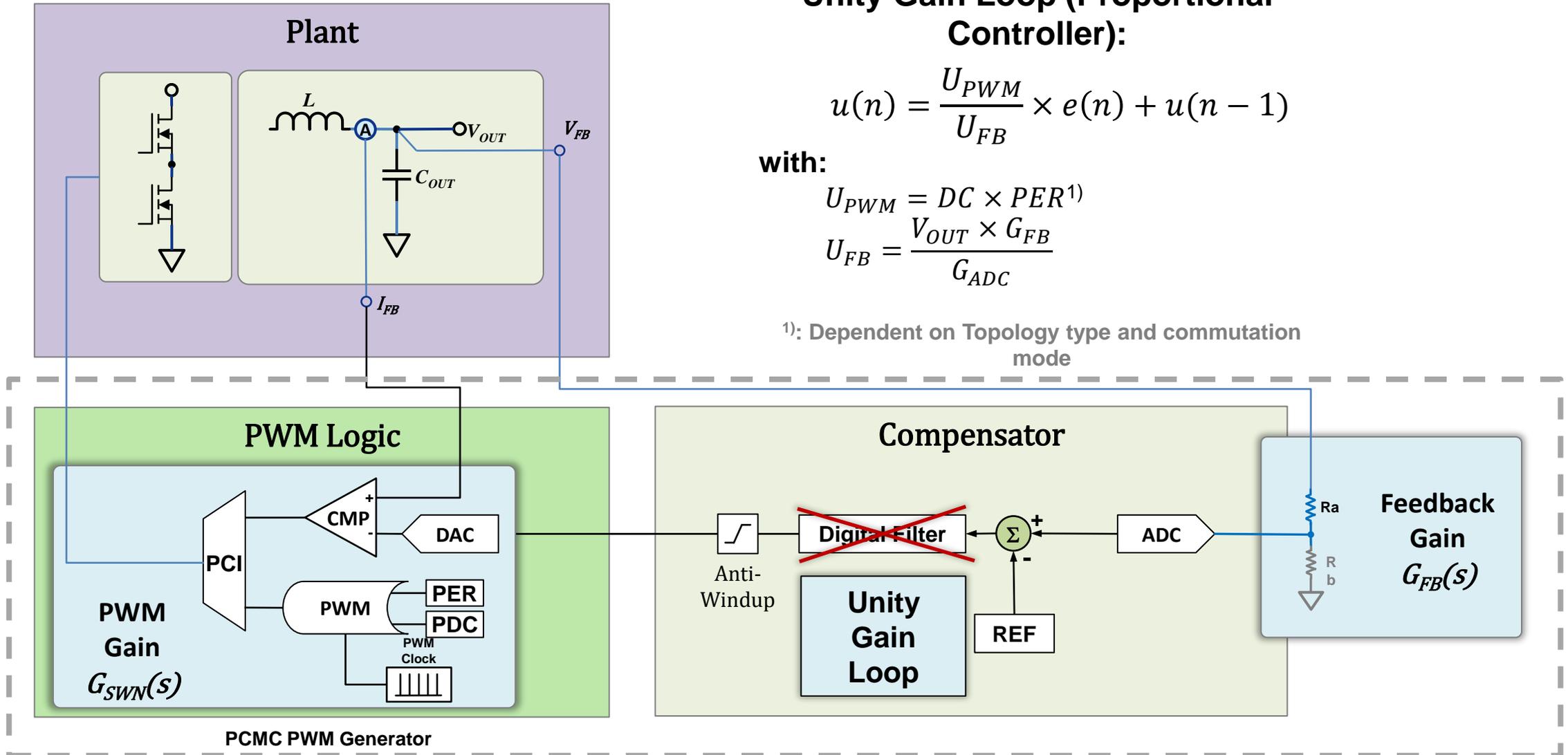
$$u(n) = \frac{U_{PWM}}{U_{FB}} \times e(n) + u(n - 1)$$

with:

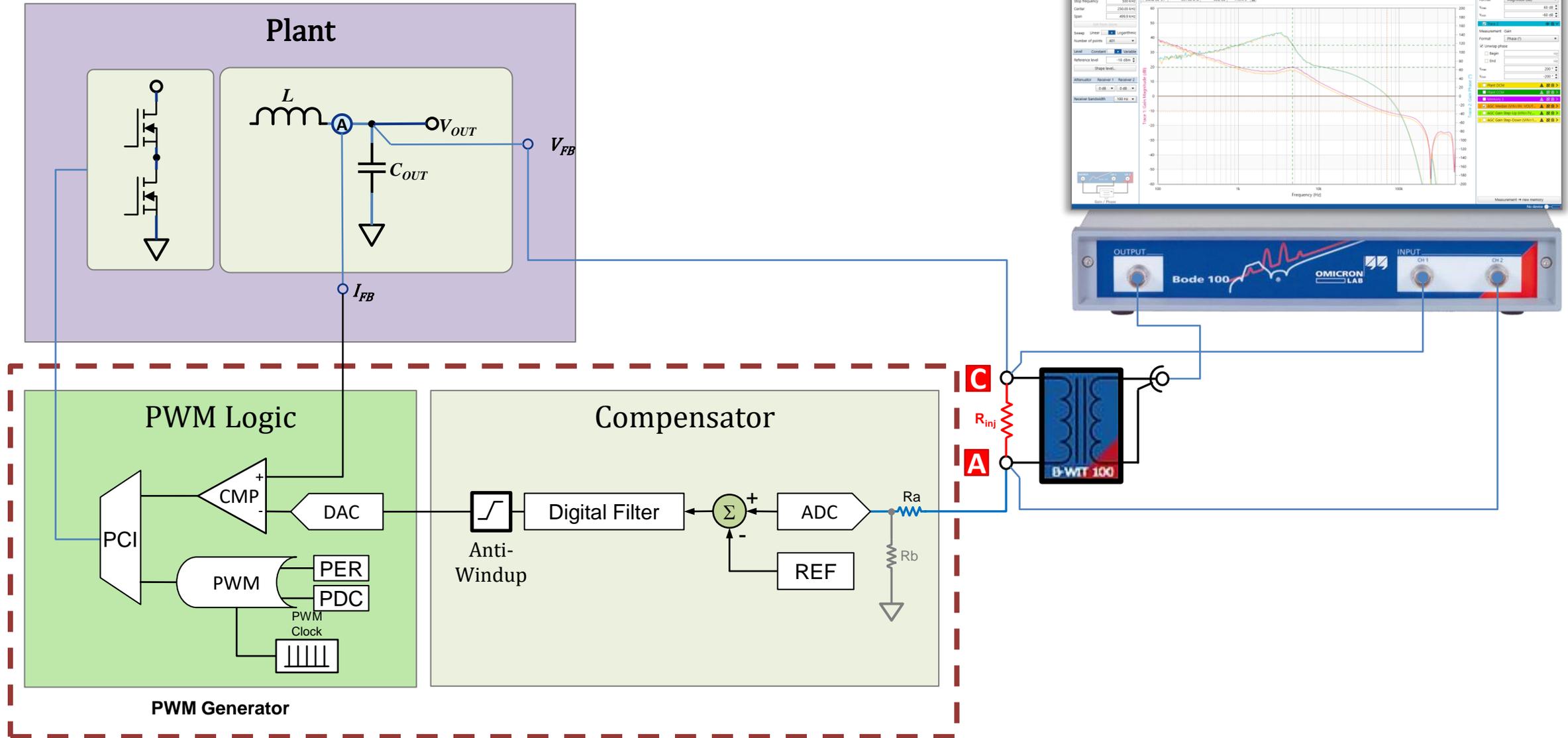
$$U_{PWM} = DC \times PER^{1)}$$

$$U_{FB} = \frac{V_{OUT} \times G_{FB}}{G_{ADC}}$$

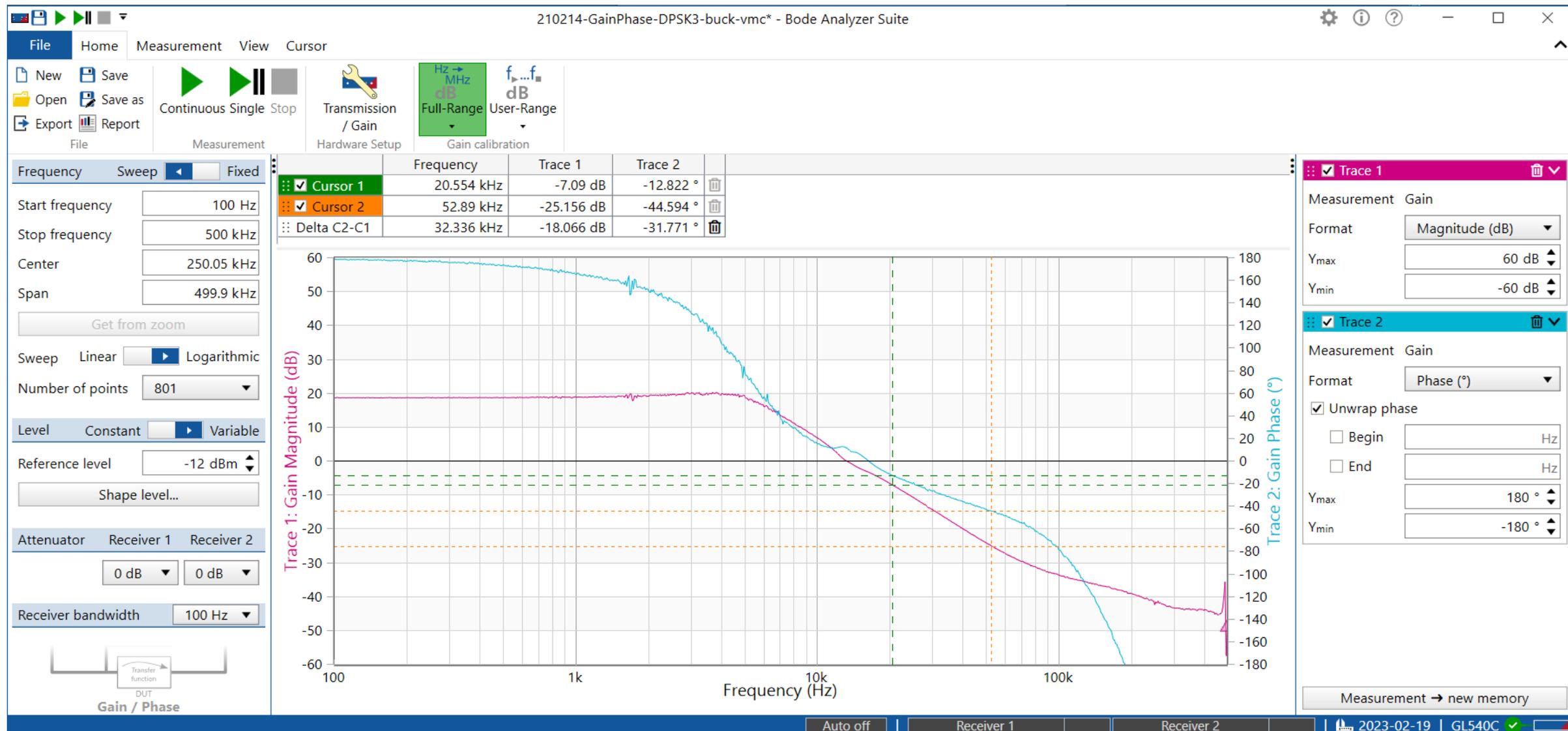
1): Dependent on Topology type and commutation mode



Measurement Setup



Plant Measurement Result



Control Loop Adjustment

The screenshot displays the PowerSmart Digital Control Library Designer v1.9.15.709 interface. The main window is titled "Frequency Domain" and shows a Bode plot of the control loop. The plot displays Magnitude/Gain [dB] on the left y-axis (ranging from -40 to 60) and Phase [°] on the right y-axis (ranging from -180 to 180). The x-axis is Frequency [Hz] on a logarithmic scale (ranging from 100 to 100,000). The plot shows the magnitude and phase of the system (z) and the compensator (s). Vertical dashed lines indicate Pole Locations (green) and Zero Locations (yellow). The compensator type is set to "4P4Z - Discrete Type IV Compensator". The scaling mode is "4 - Fast Floating Point Scaling". The input gain is set to 0.500000. The compensation filter settings include a sampling frequency of 500k Hz and a cross-over frequency of pole at origin of 600 Hz. The pole and zero locations are listed in the table below:

Pole	Frequency [Hz]	Zero	Frequency [Hz]
Pole 1	75k	Zero 1	2k
Pole 2	100k	Zero 2	4k
Pole 3	180k	Zero 3	18k

Annotations in red text and arrows highlight the "Compensator Type Selection" and "Pole & Zero Placement" sections.

Compensator Type Selection

Pole & Zero Placement

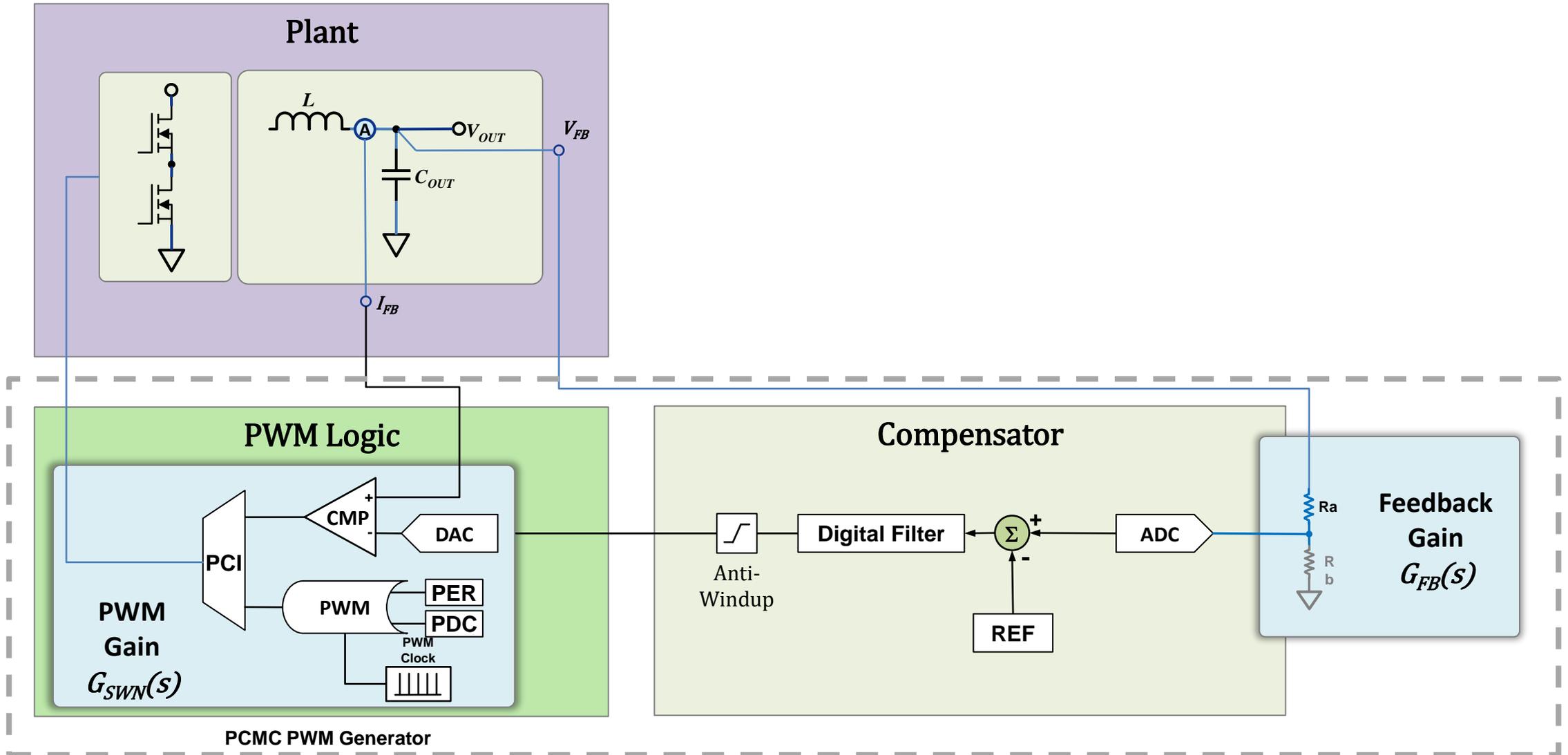
Bode Plot Settings

Parameter	Value	Unit
Start	100	Hz
Stop	250k	Hz
Points	801	
Min	-60	dB
Max	60	dB
Div	10	dB
Min	-180	°
Max	180	°
Div	30	°

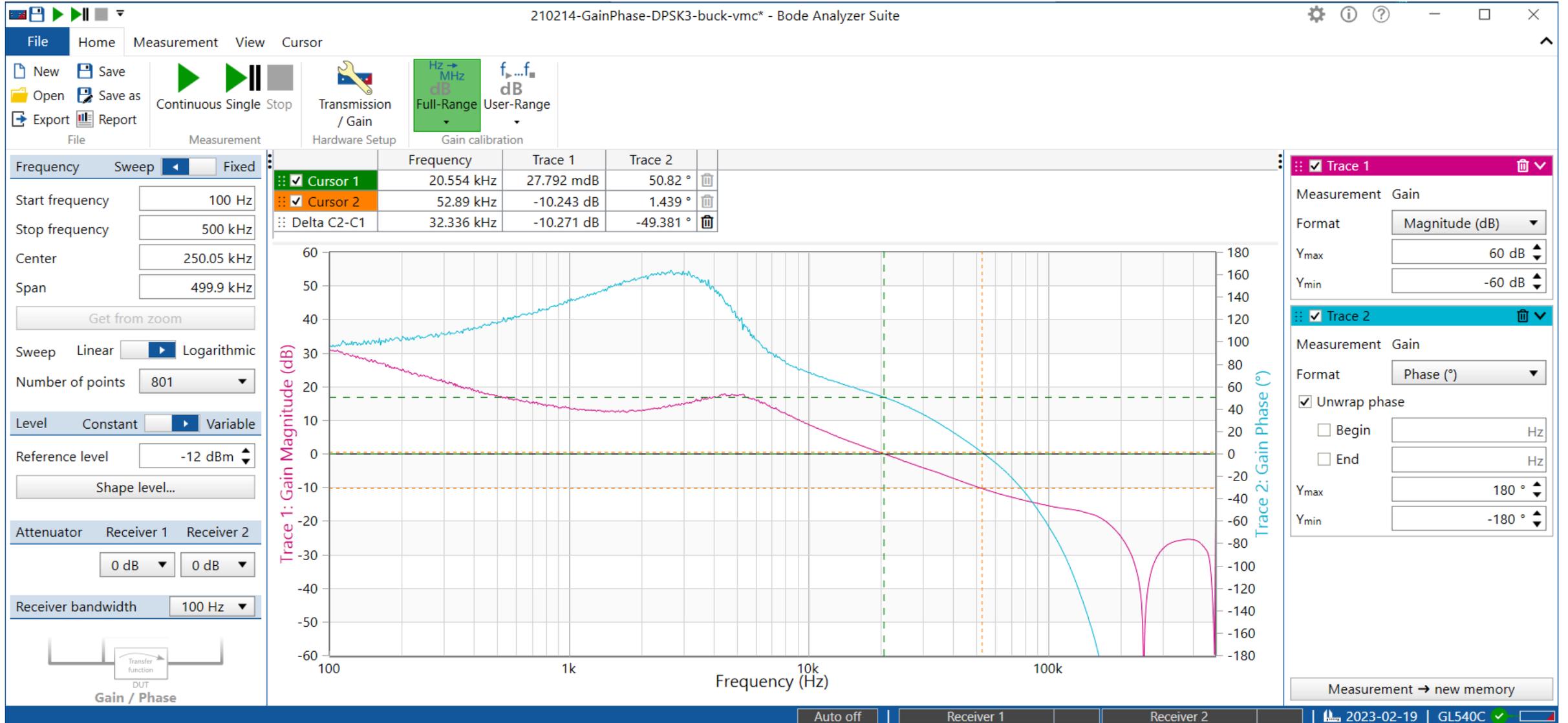
Options: Unwrap Phase, Show s-Domain

Refresh Period: 18 ms Table Options

Open Loop Measurement



Open Loop Gain Measurement



Agenda



Digital Power Supply Control Overview



Rapid Prototyping



System Firmware Development & Test



Summary

Application Example

Intermediate DC/DC Bus Converter

Interleaved, non-isolated synchronous Buck Converter

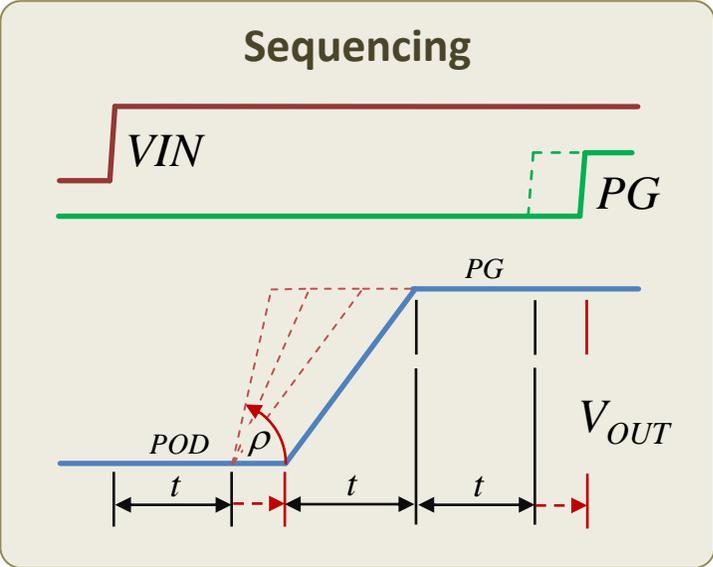
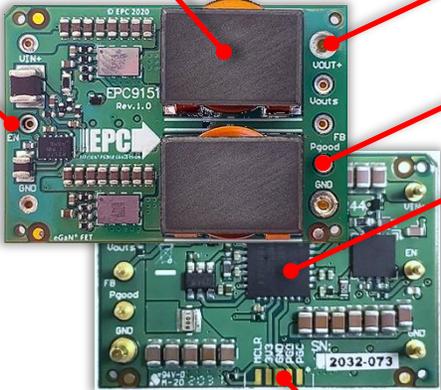
48V Rail Input Power with Enable Pin

Single 9-15V Output

Power Good Output

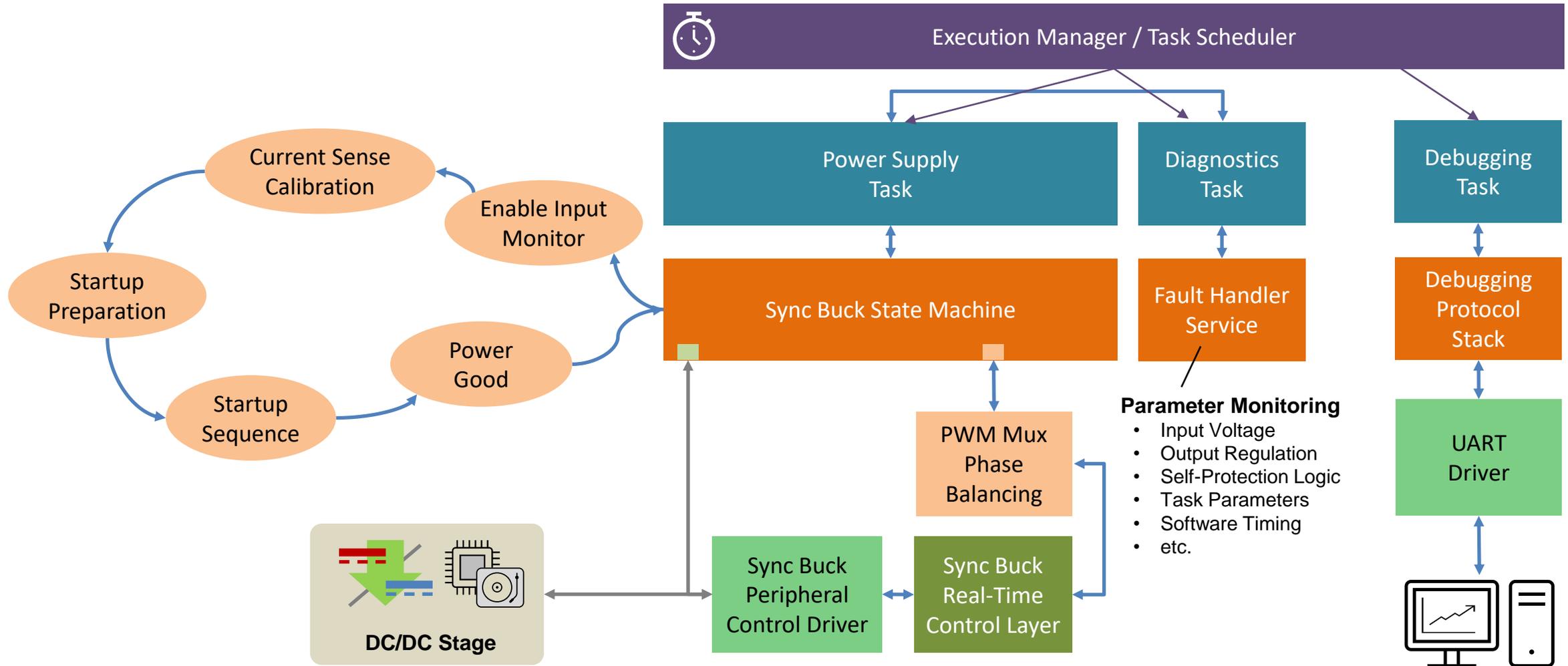
Single Core DSC

Debugging Port / UART Interface



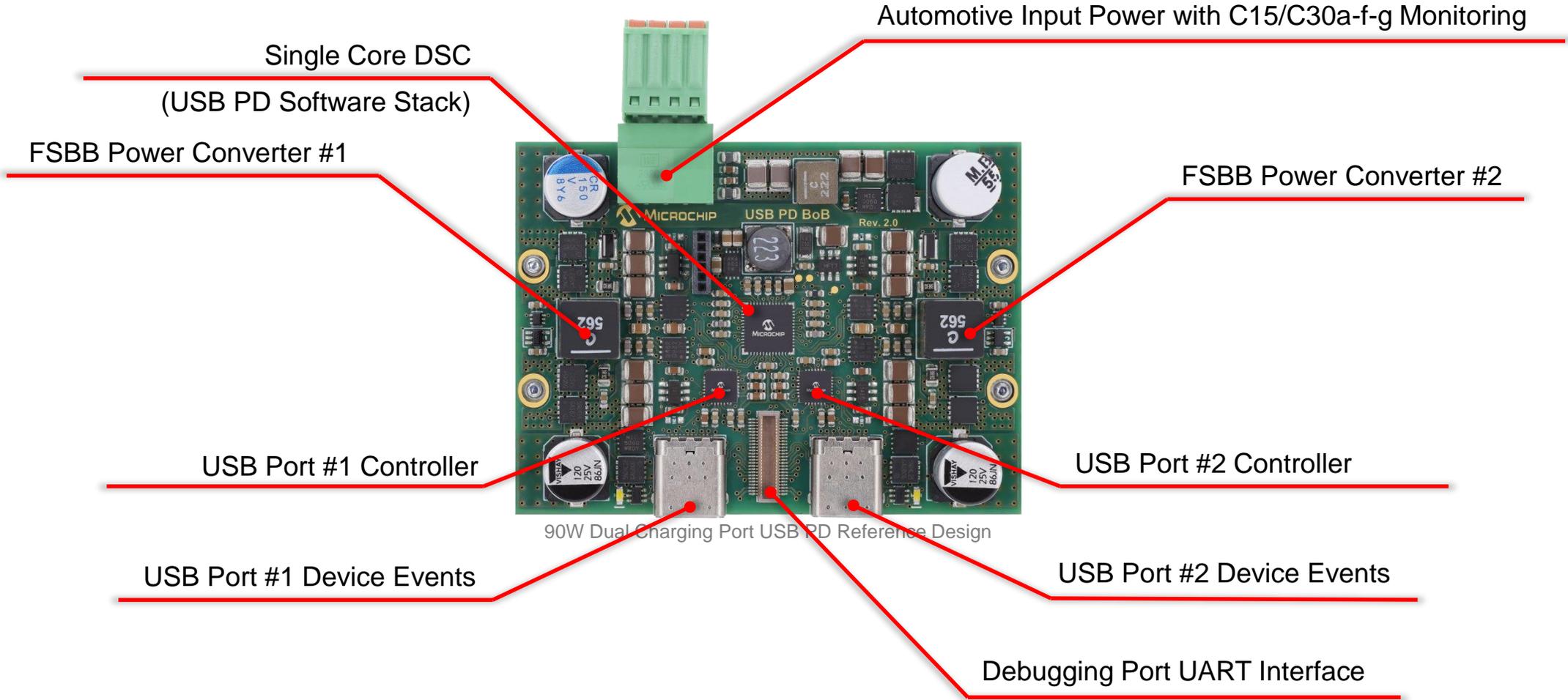
Application Example

Intermediate DC/DC Bus Converter



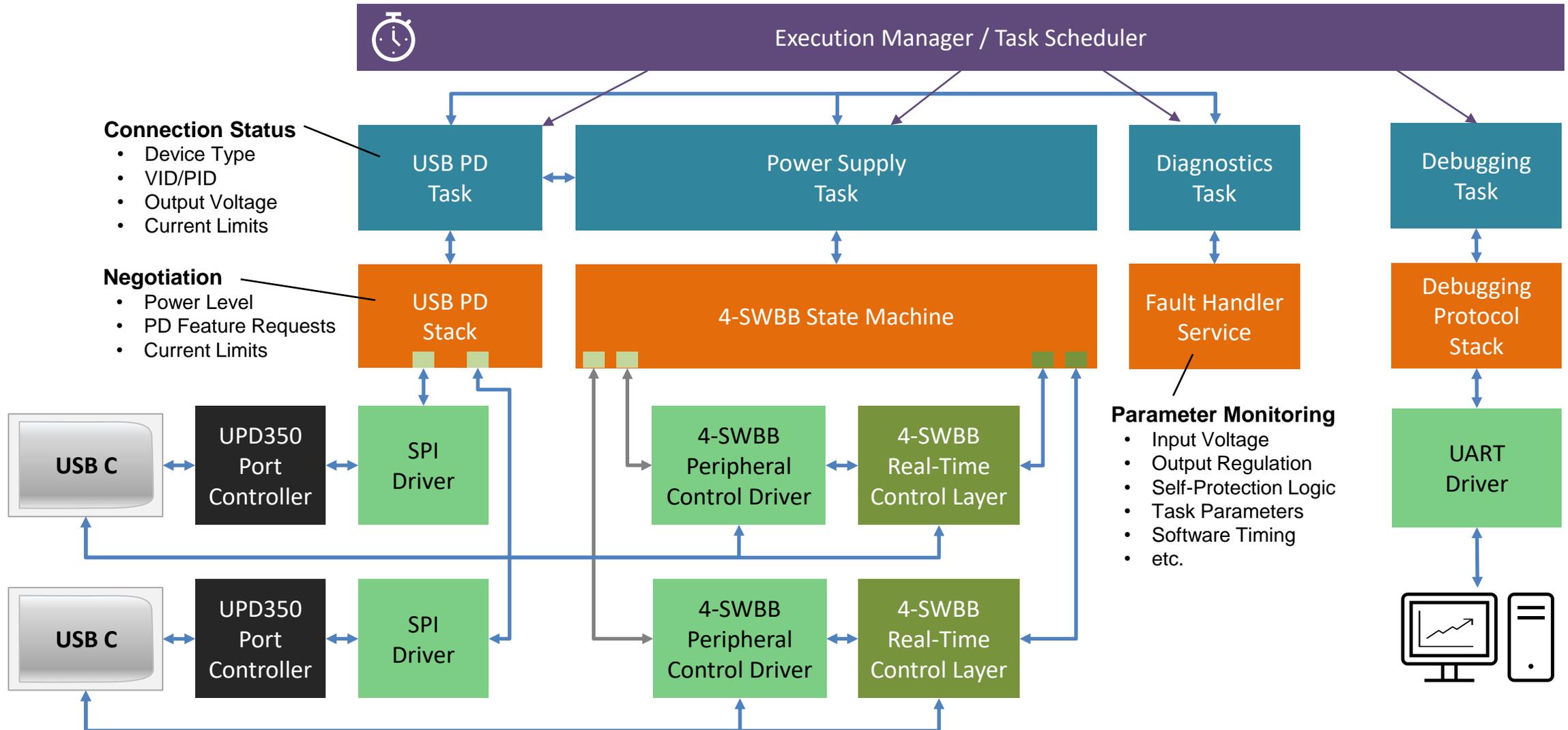
Application Example

Dual Charging Port USB PD Design



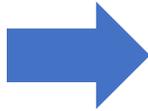
Application Example

Dual Charging Port USB PD Design



Application Example

Data Center AC/DC Power Supply

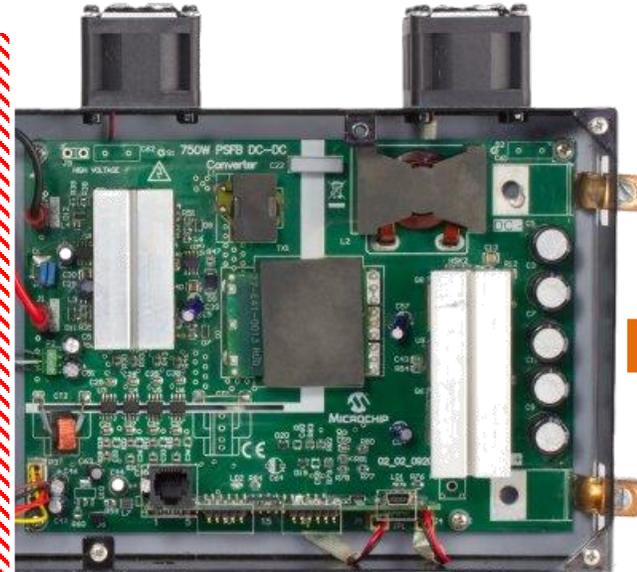


AC-Input
Power Factor Correction

Primary Controller

- AC Input Tracking
- Power Factor Correction
- Bulk Voltage Regulation
- Auxiliary Power Control
- P2S Communication
- Energy Metering

Isolation



DC-Output
400V-to-48/12V Conversion

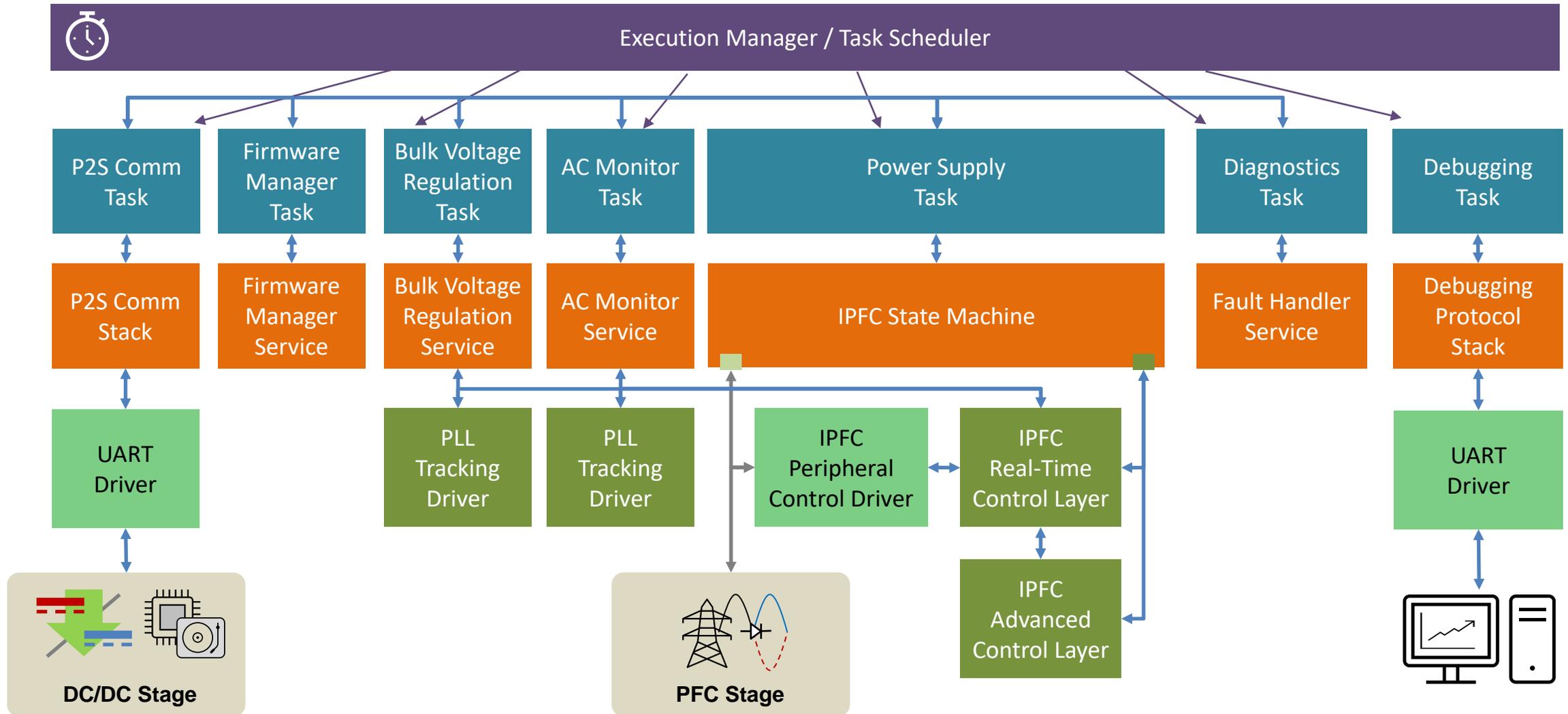
Secondary Controller

- DC Output Regulation
- Current Sharing / Redundancy
- Fan Control
- S2P Communication
- Host Communication
- Firmware Update Management



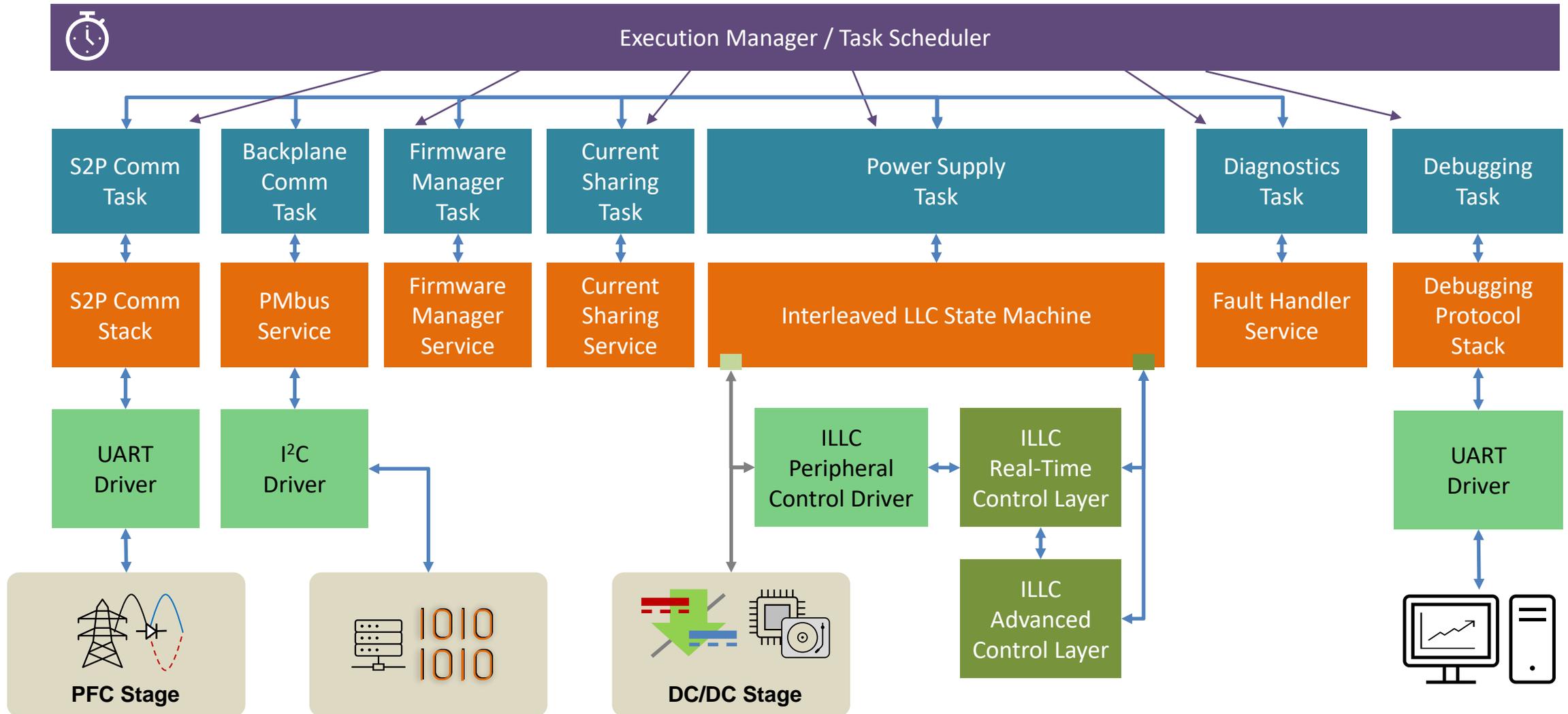
Application Example

Data Center AC/DC Power Supply – Primary Side Firmware



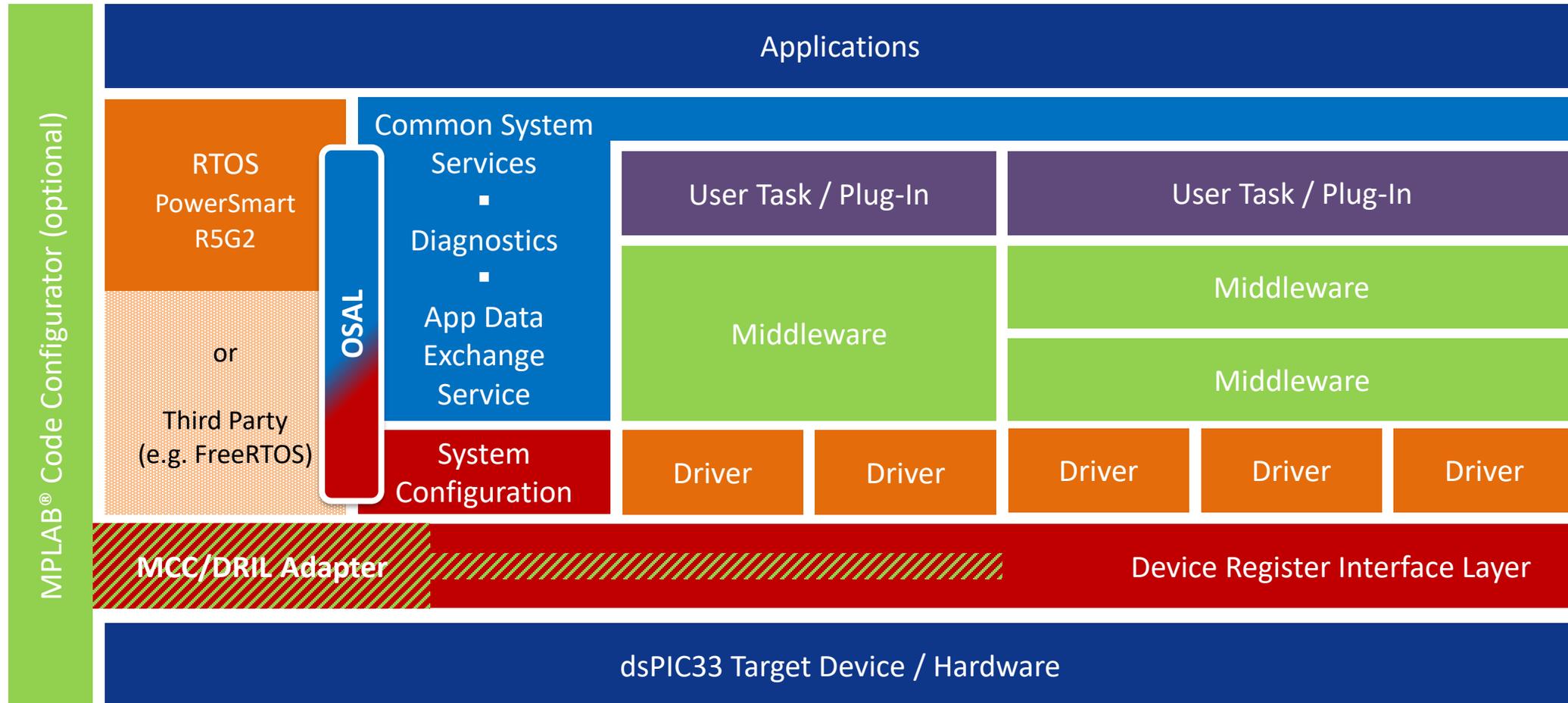
Application Example

Data Center AC/DC Power Supply – Secondary Side Firmware



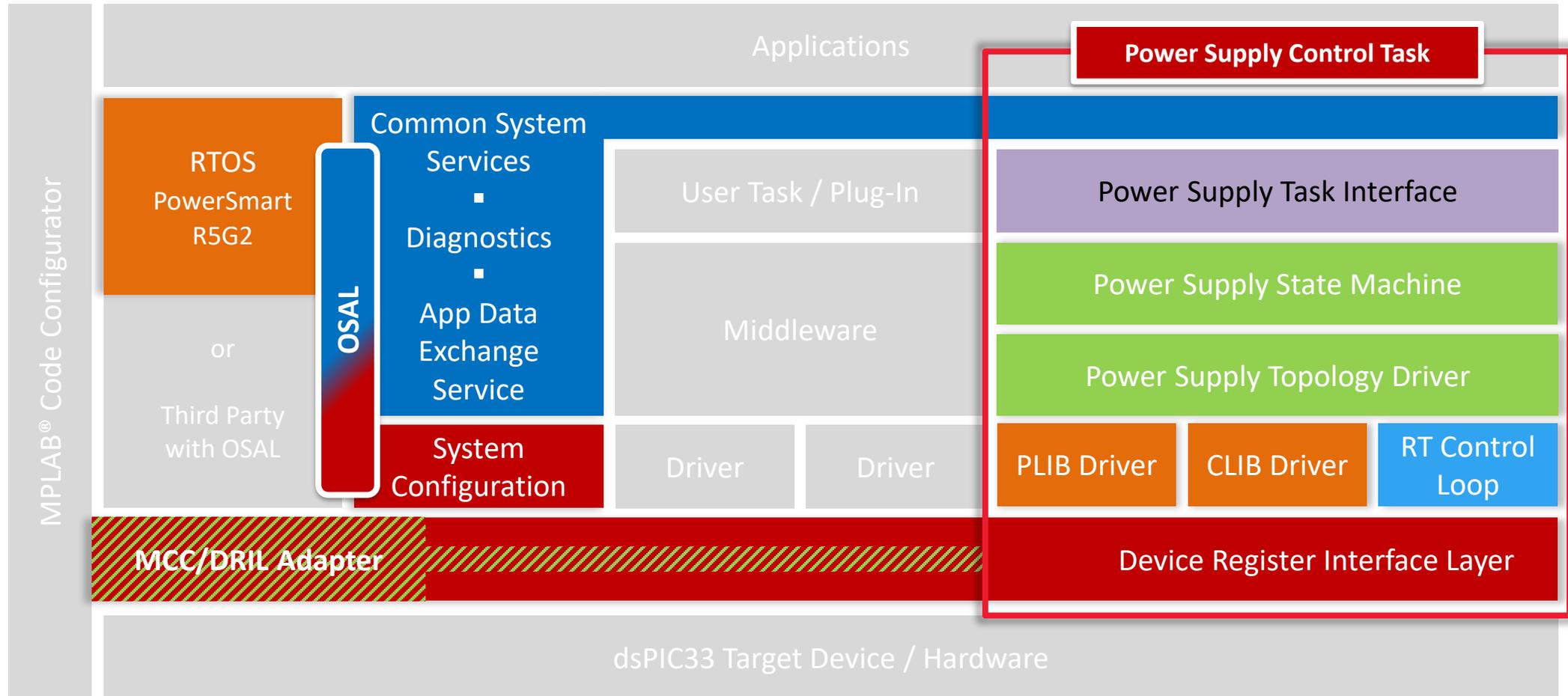
MPLAB® PowerSmart™ Development Suite

MPLAB® PowerSmart™ Software Framework for dsPIC33 DSCs



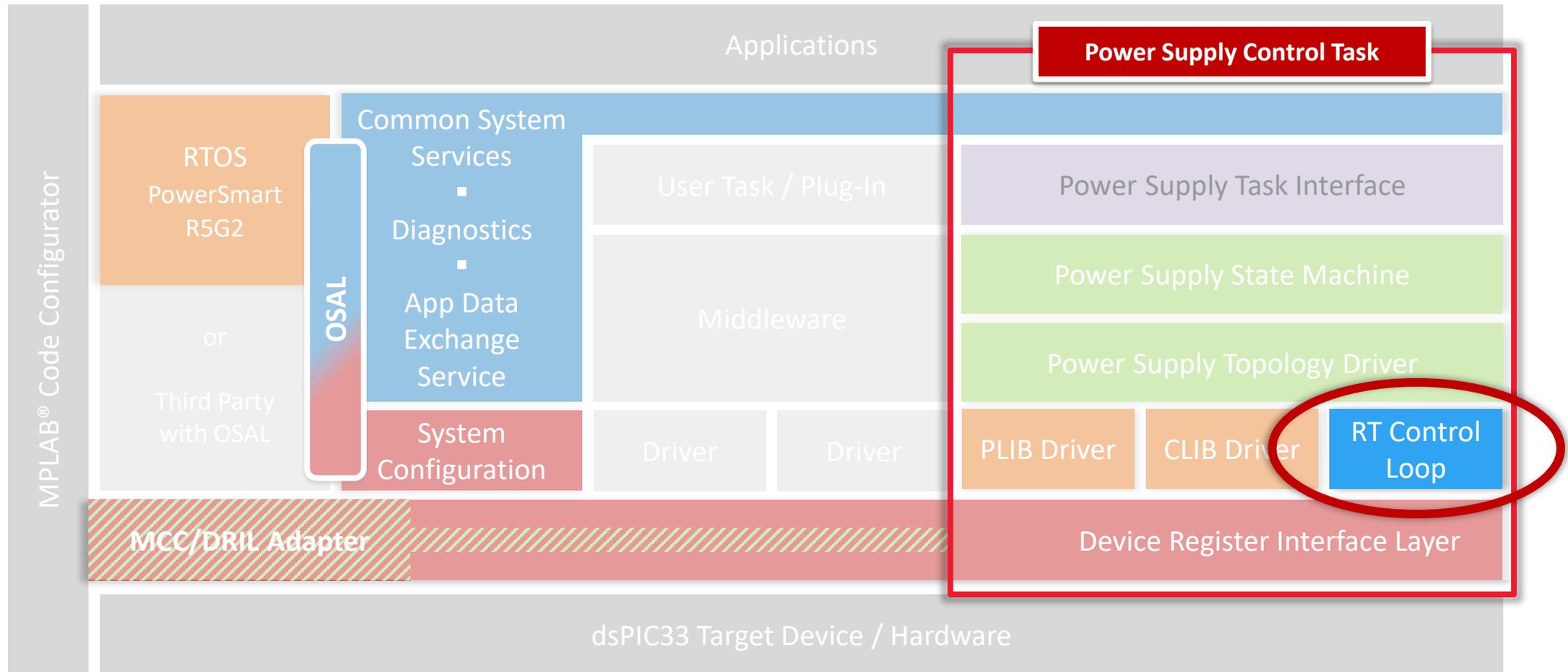
MPLAB® PowerSmart™ Development Suite

MPLAB® PowerSmart™ Software Framework for dsPIC33 DSCs



MPLAB® PowerSmart™ Development Suite

MPLAB® PowerSmart™ Software GUI Components for dsPIC33 DSCs



Model Oriented Design & Firmware Test

Using Plexim PLECS

- **What is PLECS?**
 - Behavioral circuit simulation, optimized for power electronics
 - Available as standalone software or as building block for MATLAB Simulink
- **Simulation Options**
- **Virtual Simulation**
 - System simulation using component models only
 - Additional coder and scripting allows state changes
- **Processor In the Loop (PIL)**
 - Virtual system circuit **while executing real code on real target device**
- **Real-Time Simulation using RT-Box**
 - Real time signal simulation stimulating real target device
 - Firmware now runs at full execution speed



PLECS PIL Firmware Test

Hardware Model

Control Loop Design

Optimized Code Generation

USB

MPLAB POWERSMART DEVELOPMENT SUITE

The image shows a workflow for testing PIL firmware. It starts with a hardware model of a power converter, which is used to generate a control loop design. The design is then optimized and code is generated, which is transferred via USB to a microcontroller board for testing. The background features various software windows from the MPLAB Powersmart Development Suite, including a Bode Plot, a Control Loop Design window, and a Code Generation window.

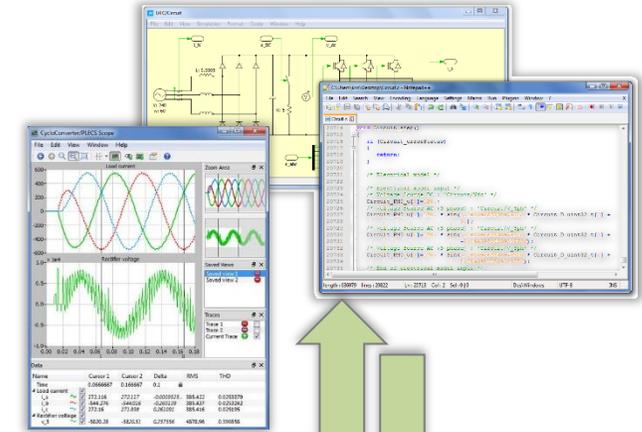
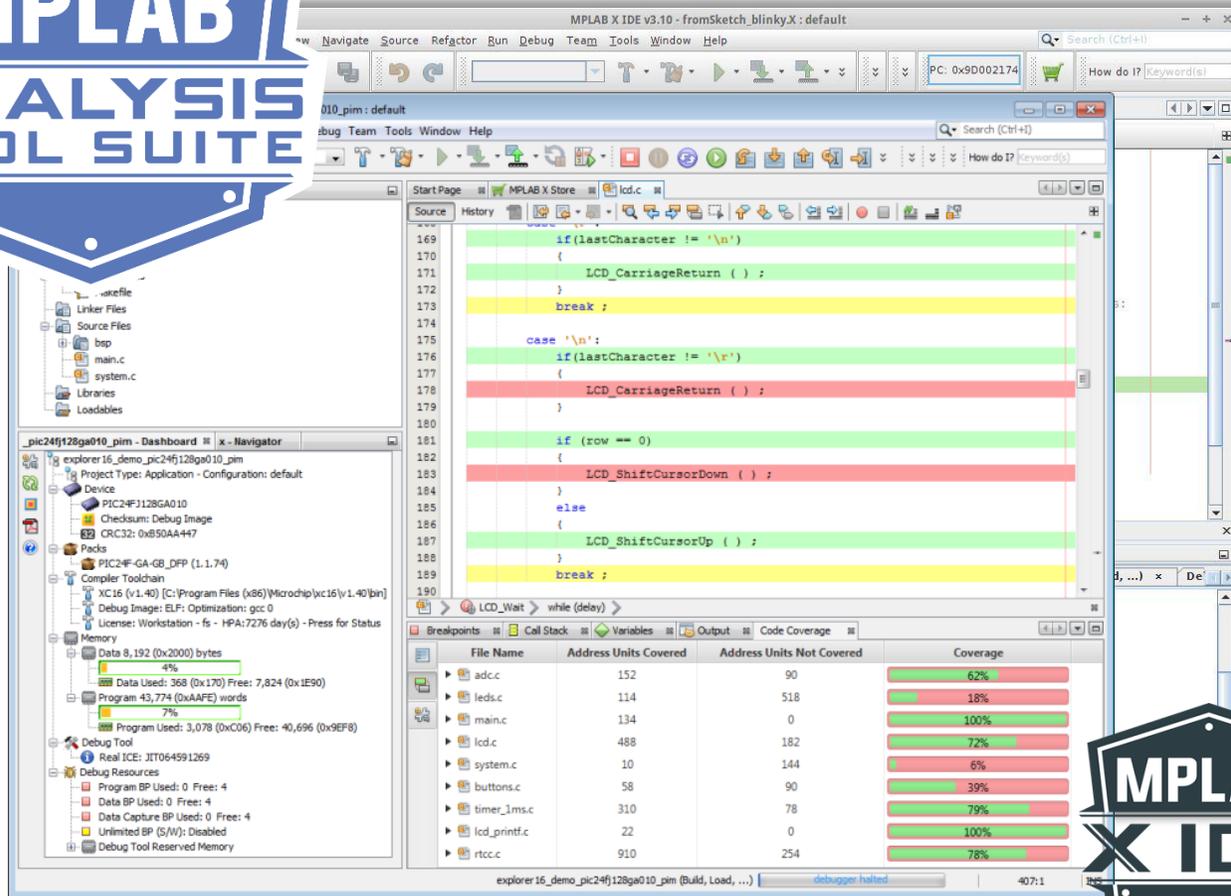
PIL Firmware Test

Using Plexim PLECS – PIL Simulation

- **PIL allows to include the vendor IDE**
 - Firmware can run in debugging session, allowing to debug and troubleshoot firmware issues and observe internal data
 - Integrated Development Environment (IDE) Extensions can be enabled, such as Code Coverage Measurement
 - Virtual hardware allows simulation of catastrophic fault cases, (e.g. shorted FETs)

Firmware Debugging & Test

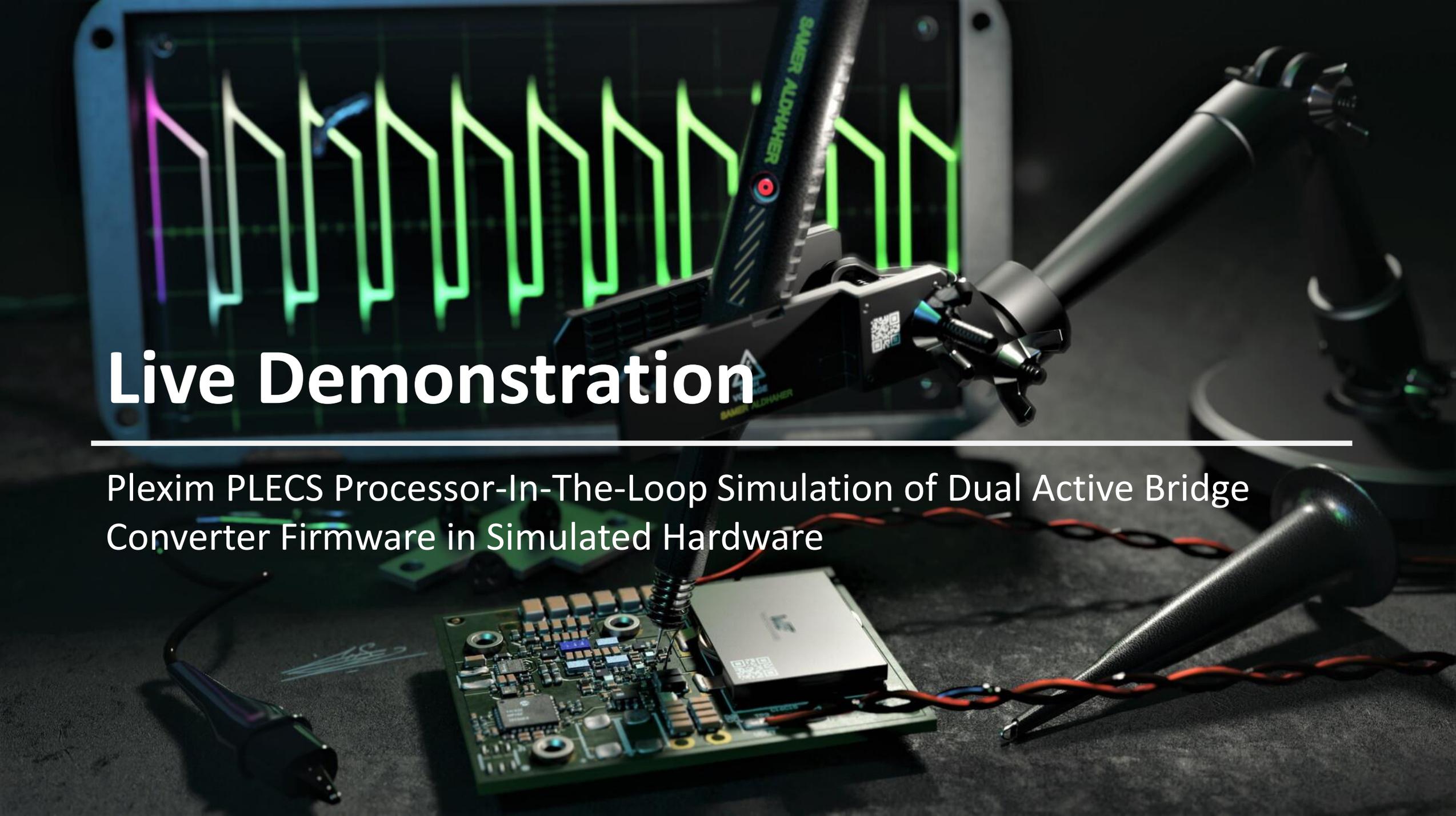
PLECS on Computer runs the simulation



Target firmware test during simulation



Target device runs the firmware

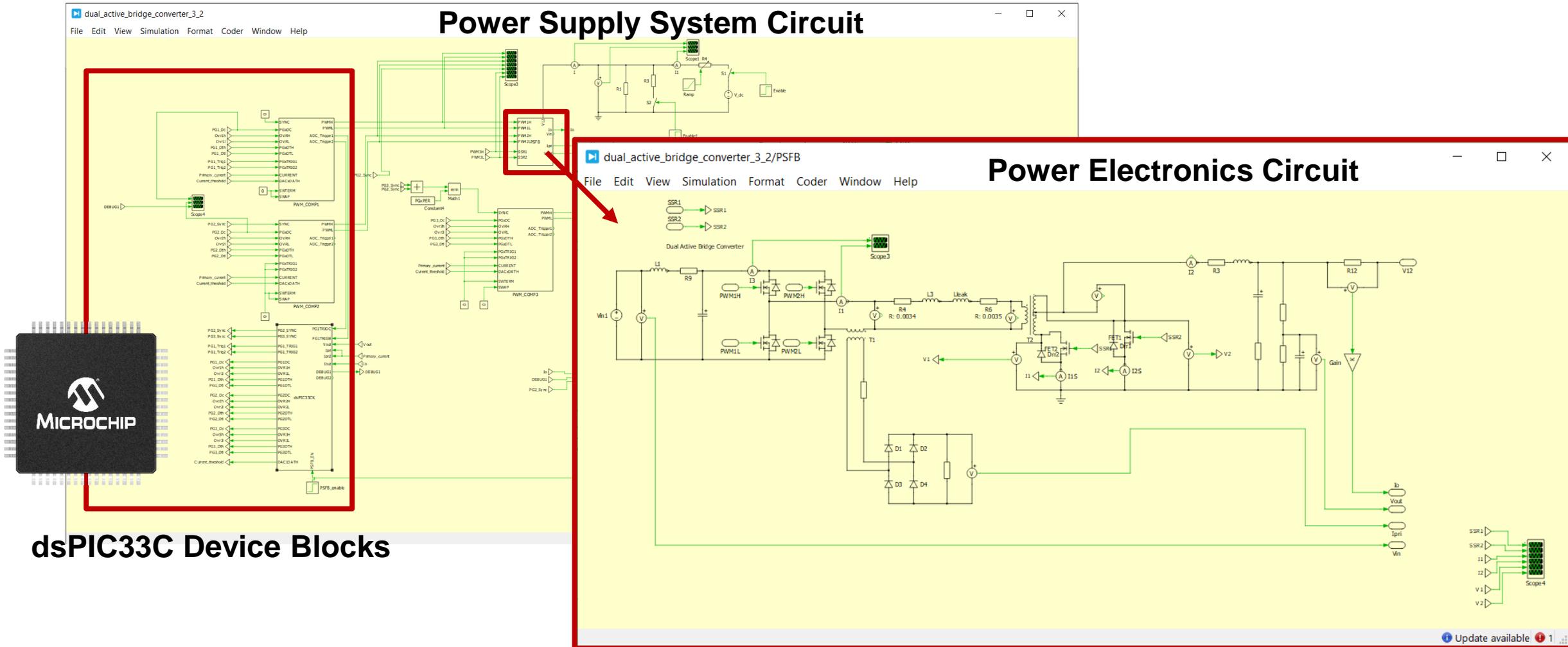
A robotic hand is shown in the foreground, holding a soldering iron and working on a green printed circuit board (PCB). The hand is positioned over a component on the board. In the background, a monitor displays a series of green and purple waveforms, likely representing the simulation results of a dual active bridge converter. The scene is set in a dark environment, possibly a laboratory or workshop, with a focus on the precision of the robotic assembly process.

Live Demonstration

Plexim PLECS Processor-In-The-Loop Simulation of Dual Active Bridge Converter Firmware in Simulated Hardware

PLECS PIL Firmware Test Demo

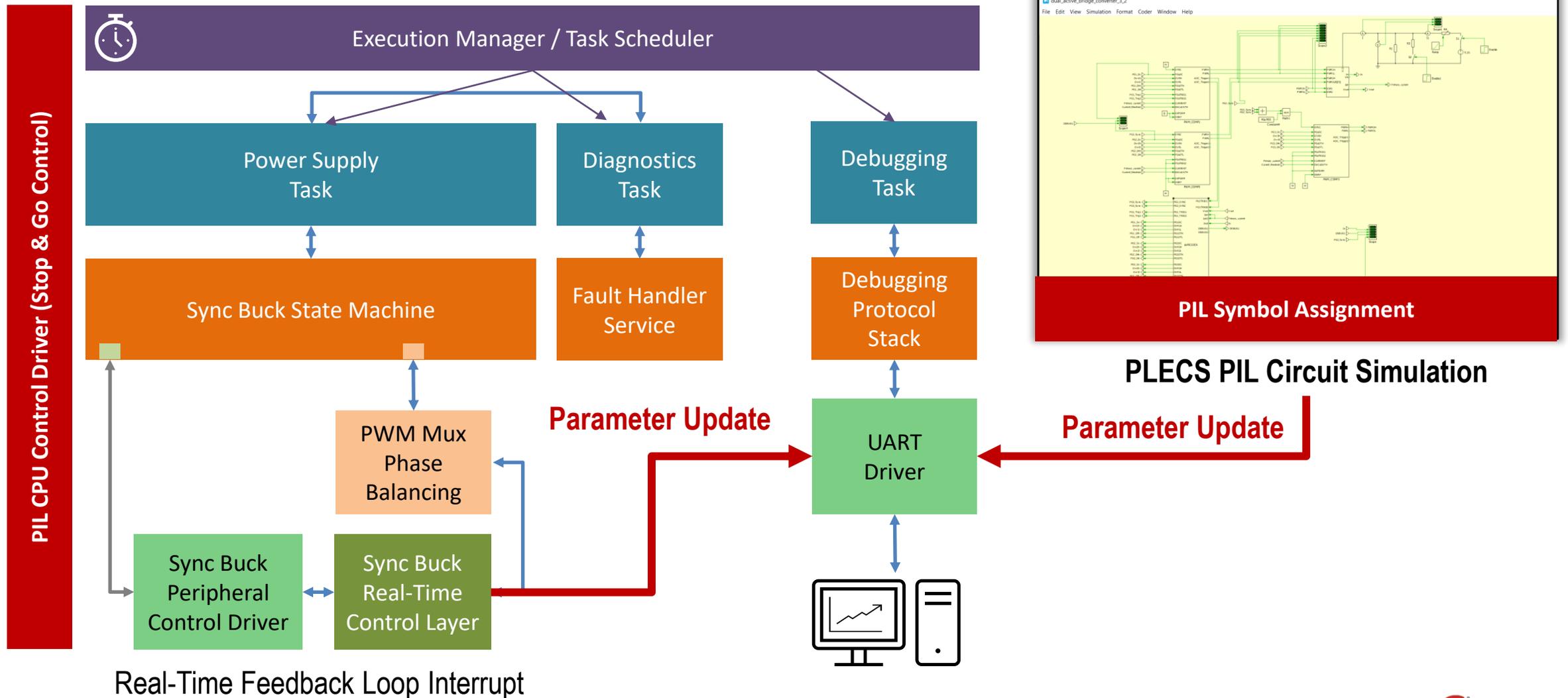
Firmware Test for Dual Active Bridge Converter



dsPIC33C Device Blocks

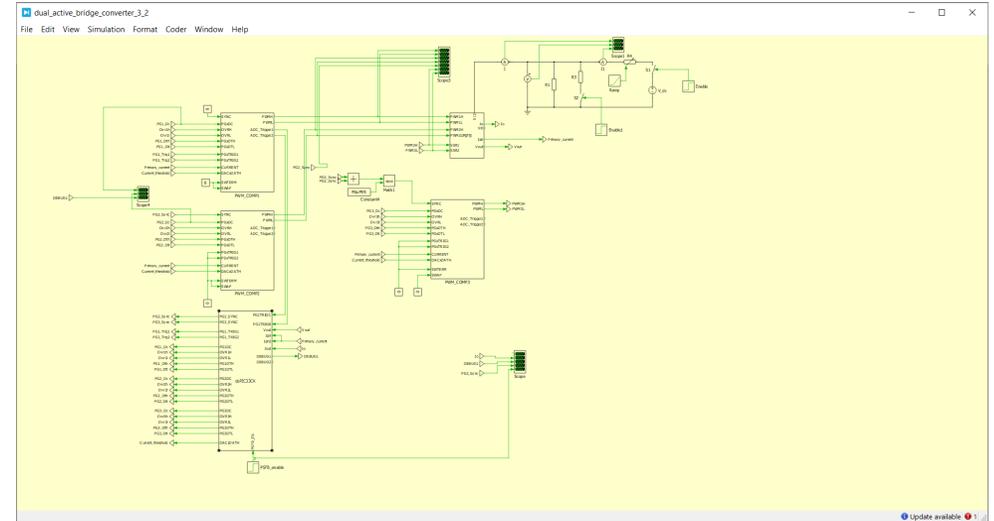
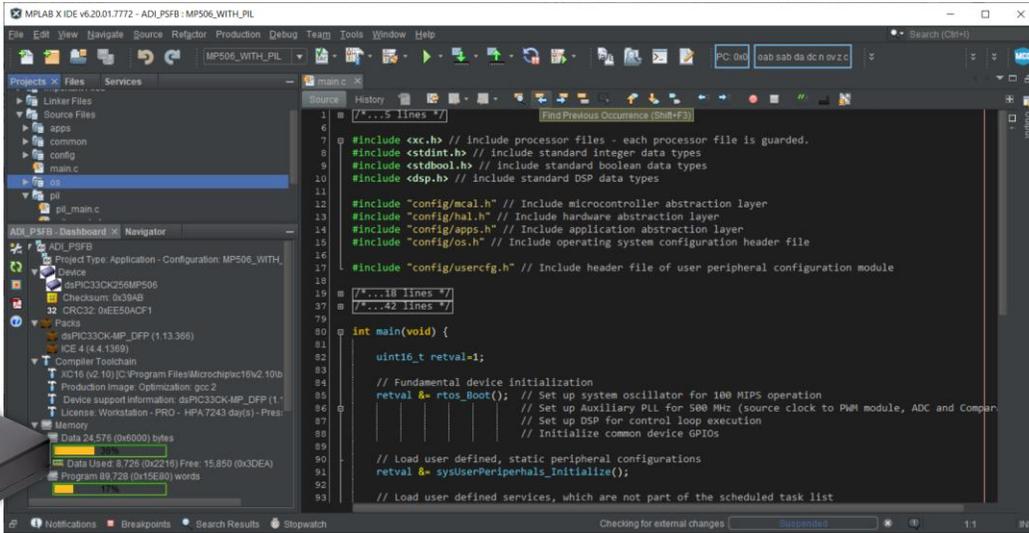
PLECS PIL Firmware Test Demo

Firmware Modification



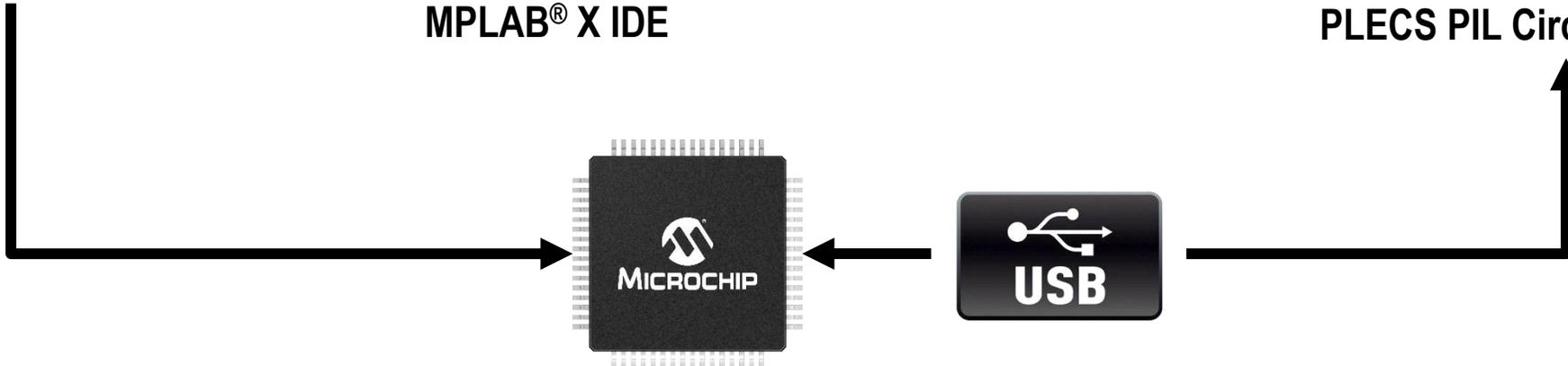
PLECS PIL Firmware Test Demo

Firmware Test for Dual Active Bridge Converter



MPLAB® X IDE

PLECS PIL Circuit Simulation



Agenda



Digital Power Supply Control Overview



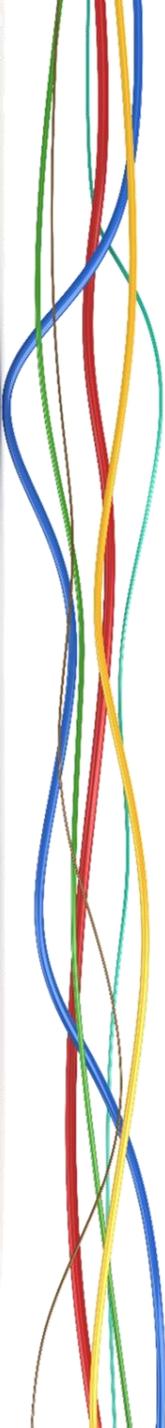
Rapid Prototyping



System Firmware Development & Test



Summary



Summary

- Digital Control of switch-mode power supplies enables new topologies, solves non-linear control challenges, eases product family management and customization and makes products more robust
- However, introducing control firmware into the design requires additional test, verification and quality management infrastructure and skills
- Wide range of various design tool eco systems and templates offer extensive design support and help to cut design cycles short

Digital Power Training

- **Getting Started in Digital Power**

- Intelligent Power Design Center:

<https://www.microchip.com/power>

- **How-2 Starter Kits**

- Digital Power Starter Kit 3 (Part-No. DM330017-3):

<https://www.microchip.com/dm330017-3>

- **Self-Paced Training:**

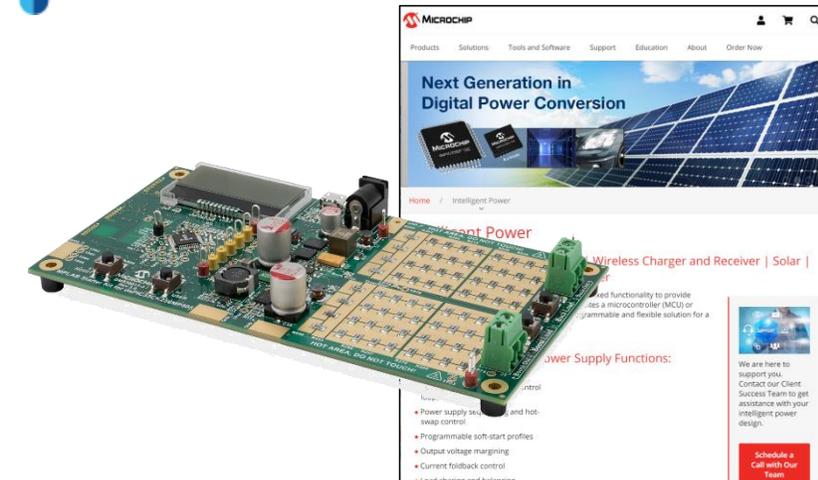
- Microchip University (Virtual Training Platform):

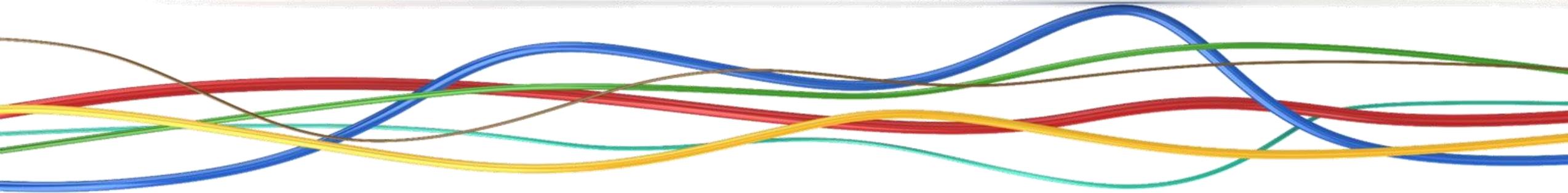
<https://secure.microchip.com/mu>

- **Face-2-Face Workshops:**

- Biricha Digital Power & PFC Workshop, **June 4th to 7th 2024**, Freiham near Munich

Register under <https://www.biricha.com/microchip.html>





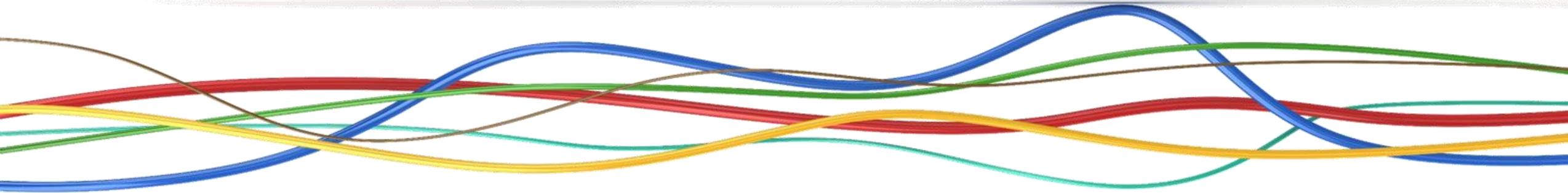
Q & A



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Thank You!

May the power be with you!



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Publication Information

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Duration: 60 min
Presenter: Andreas Reiter, Senior Application Engineer Digital Power, Microchip Technology Inc.



Short Bio:

Andreas Reiter is Senior Applications Engineer for Digital Power Applications at Microchip Technology. Andreas has been working in power electronics since 1997 and is focusing on digitally controlled power conversion since 2006. Andreas' experience and interest include future requirement identification research and respective solutions development. His field of work ranges from supporting chip design teams in defining future features of semiconductor products to developing reference designs, concept boards and digital control loop algorithms for next generation switch mode power supplies. Focus applications at Microchip Technology are nodes in power distribution networks in data center and telecom, renewable energies and automotive electrification applications.