YAGEO

Imagine low ESL

Developing Film Capacitor with Bode100 THE to T- ICh

2025-04-09

Agenda

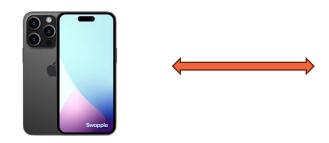


- Short introduction why
- The object the film capacitor
- The measurement setup
- Results
- Outlook

Electro Mobility and EMI aspects



- Broadcast cellphone 5G = 0.2W
- 87 Mio Inhabitents in Germany do a cell call at the same time = 16.4MW
- 60,7 Millionen vehicles (Jan 2024)
- Imagine all are BEVs and 10% driving at the same time
- operating up to 850 V / 450 A peak
- f = 5kHz ... 200kHz





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What is behind TESLA?

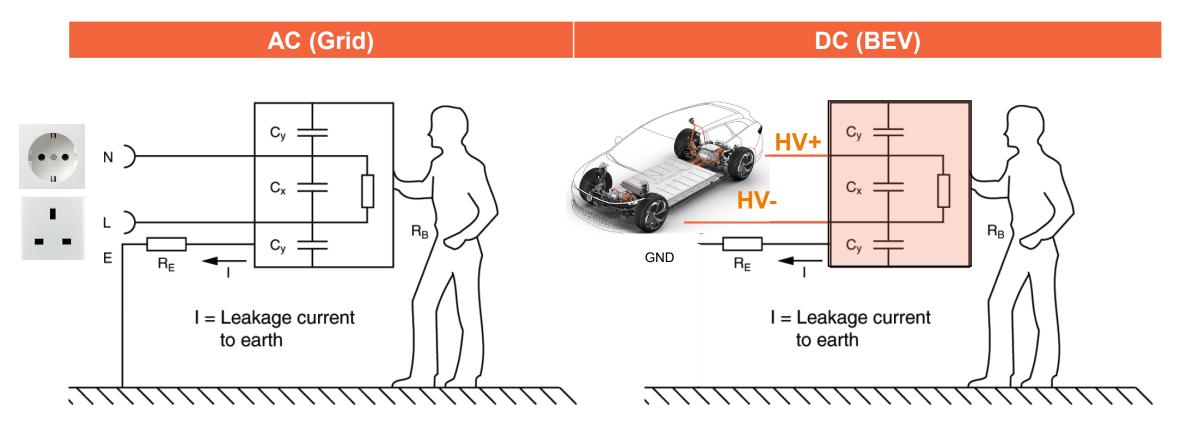




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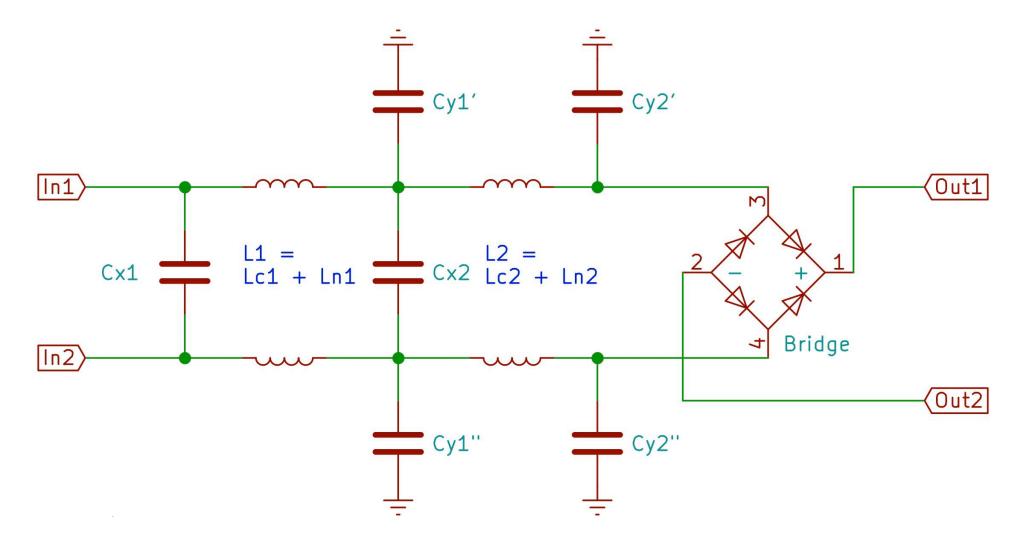
What is an EMI or X/Y capacitor ?

- aka "Funkentstörer", Safety capacitor, IEC60384-14, Y-Capacitor, X-Capacitor
- Use in grid applications (230VAC, 110VAC) and BEV (400V/800V)
- was originally developed catching transients not for DC



EMI Filter





Standards

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- Capacitance is defined 1kHz / 1Vrms no DC-bias
- DF is also defined at 1kHz
- ESR is determined at 100kHz
- There is <u>no</u> standard for ESL measurements
- Definition of inductance :

The area inside the current loop defines inductance The component is only a part of the whole loop

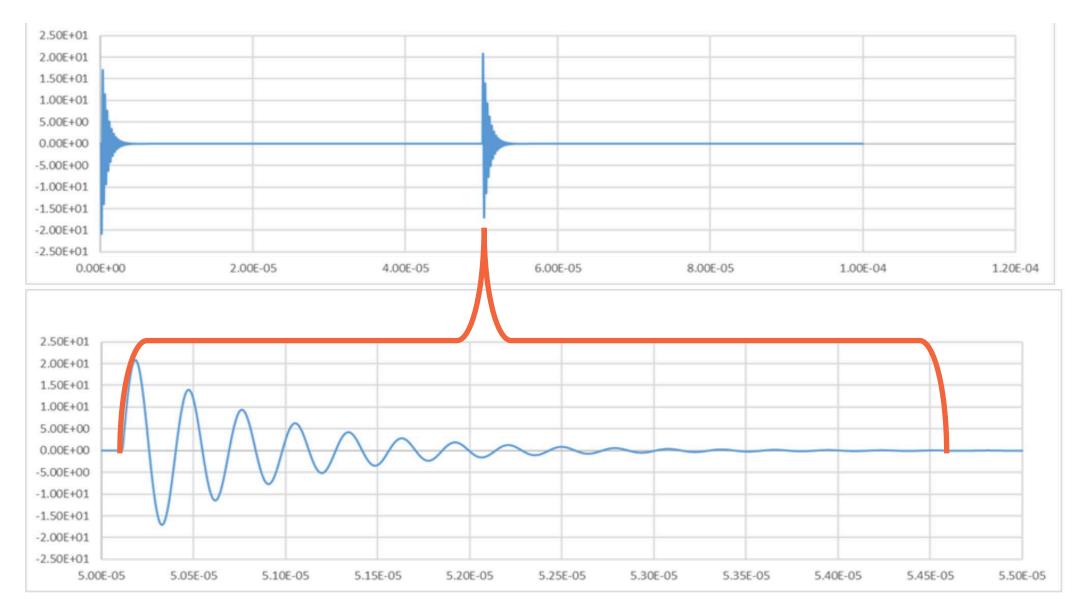
	Frequency	Trace 1	ESR	Trace 2	ESL	
🗄 🗹 Cursor 1	30 kHz	11,997 mΩ	12,142 mΩ	5,822 µH	5,813 µH 🚺	ÌÌ
🗄 🗹 Cursor 2	200 kHz	8,918 mΩ	5,75 mΩ	124,848 nH	125,358 nH 🧴	ມັ
🗄 🗹 Cursor 3	500 kHz	11,011 mΩ	10,381 mΩ	15,05 nH	15,353 nH 🚺	ມີ
🗄 🗹 Cursor 4	1 MHz	14,432 mΩ	14,253 mΩ	264,714 pH	72,002 pH 🚺	ÌÌ
						-

Why low ESL an

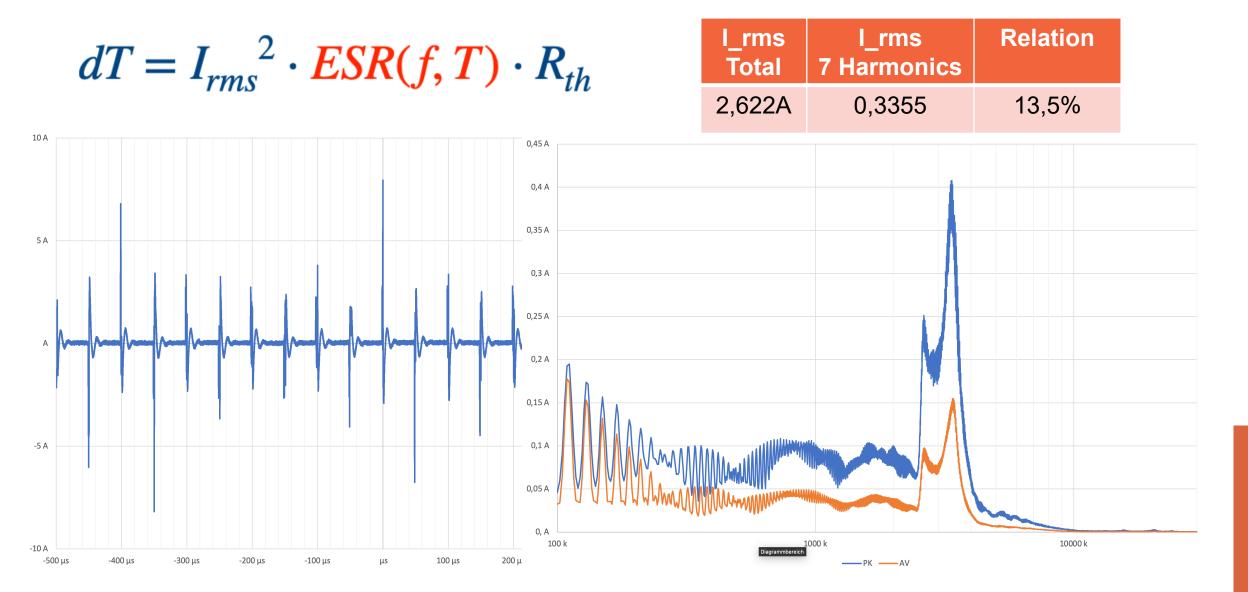


- Film capacitor widely used for DC-Link capacitors, Snubber and X/Y caps
- ESL cause
 - Impact filter performance due shift of resonance frequency
 - Ringing in switched application (Inverter, PFC)

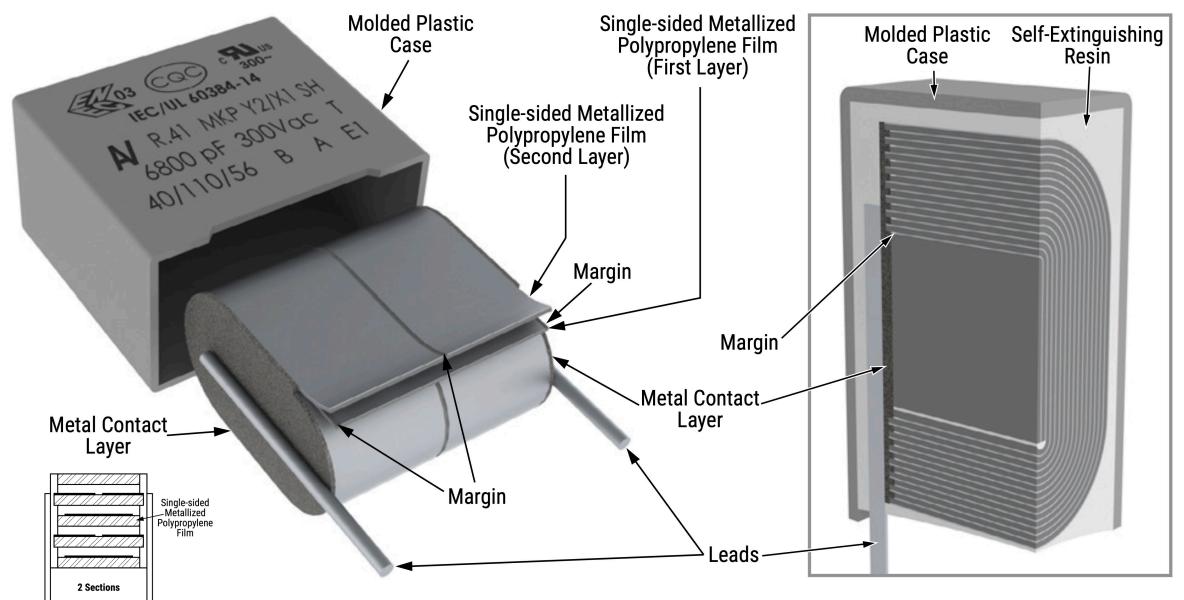
Ringing I = f(t)



Ripple current : time variant and frequency domain



Film Construction



Catalog material

Power and AC Film Capacitors – Printed Circuit Board Mount Power Film Capacitors C4AQ, Radial, 2 or 4 Leads, 500 - 1,500 VDC, for DC Link (Automotive Grade)

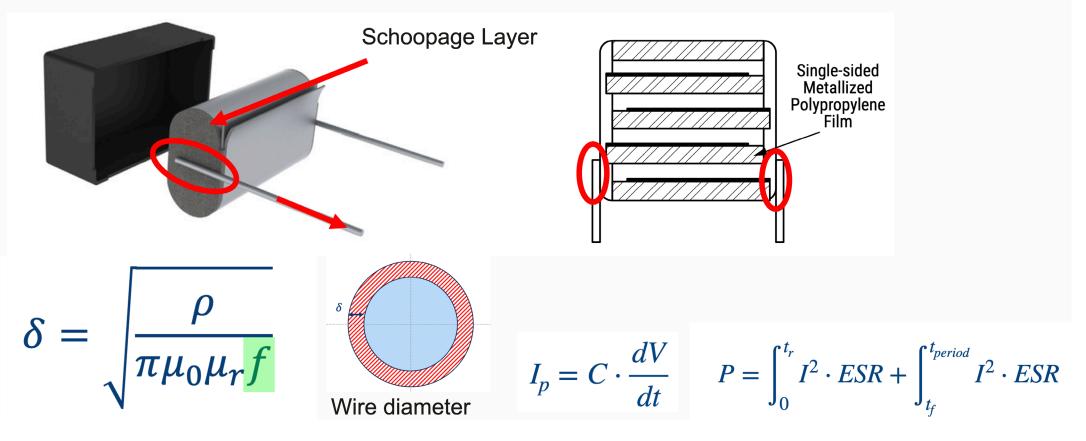


Table 1 – Ratings & Part Number Reference cont.

Cap Value	VDC	Dimensions (mm)		dV/dt	lpkr	ESL	ESR 70°C at 10 kHz	lrms* 70°C at 10 kHz	Rth (HS/Amb)	Packaging Quantity	PART NUMBER			
(µF)		Т	Η	L	S	S1	V/µs	Apk	nH	mΩ	Arms	(°C/W)		
	V _{NDC} at 70°C = 1,100 VDC; V _{OP85} at 85°C = 900 VDC; V _{OP105} at 105°C = 700 VDC													
1.5	1,100	11	20	31.5	27.5	۱	24	36	17	26.3	4.8	44	256	C4AQQBU4150A1WJ
2.7	1,100	13	25	31.5	27.5	١.	24	65	22	15.3	6.9	36	234	C4AQQBU4270A1XJ
3.3	1,100	14	28	31.5	27.5	١.	24	79	24	12.9	7.9	33	96	C4AQQBU4330A1YJ
5	1,100	19	29	31.5	27.5	۱	24	120	25	9.1	10.1	29	72	C4AQQBU4500A11J
8	1,100	22	37	31.5	27.5	١.	24	193	28	6.6	12.6	23	64	C4AQQBU4800A12J
12	1,100	20	40	42	37.5	10.2	16	190	12	6.3	14.4	20	58	C4AQQBW5120A3FJ
14	1,100	28	37	42	37.5	10.2	16	229	10	5.4	16.3	18	36	C4AQQBW5140A3JJ
I			·	I		.					- · -			

ESR impact by Wires – 0.8mm, 1.0mm and 1.2mm

- Loss in transition of Schoopage layer
- Additional loss due increasing resistance in lead wire due skin effect at higher frequencies



Skin effect on Cu wires

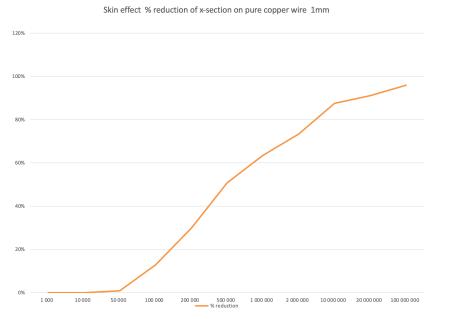


• At 500kHz the x-section is only a half

 $\delta = \sqrt{\frac{2 \cdot \rho}{\omega \mu}}$ $\delta = deepth \ of \ material$ $\rho = specific \ resistance$ $\omega = angular \ frequency = 2\pi \ freq$ $\mu = permeability$

$$A = \pi (D^2 - (D - \delta)^2)$$

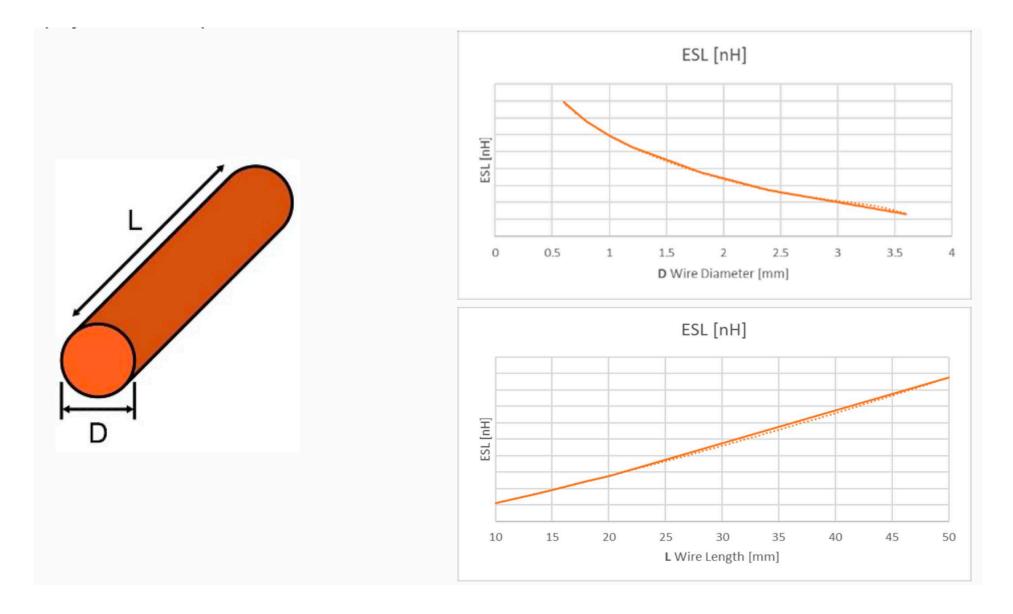
 $A = wire \ cross - section$ $D = wire \ diameter$ $\delta = deepth \ of \ material$



Frequency / kHz	Loss / %	Wire 1.0mm
10kHz	0%	1.0
50kHz	15%	0.85
100kHz	32%	0.68
200kHz	48%	0.52
500kHz	65%	0.45

ESL Value cersus Wire Ø and length

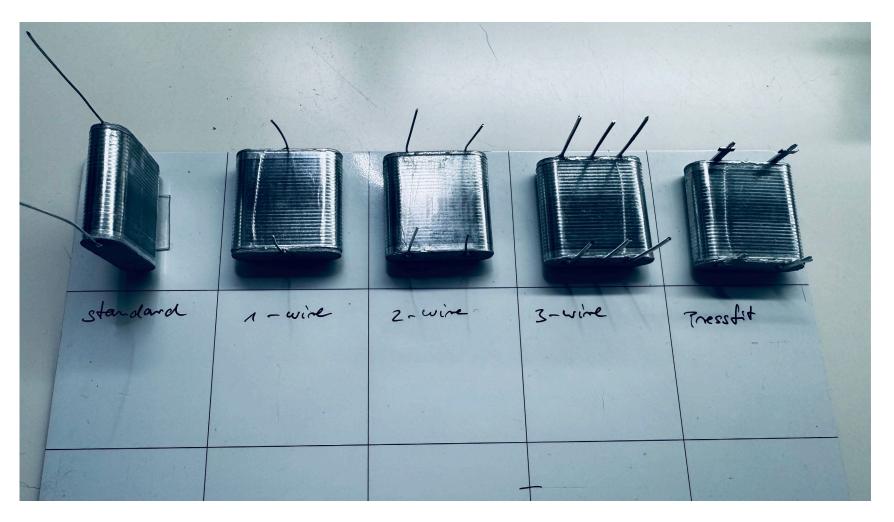




Specimen for our test



Wirethickness 0.8 1,0



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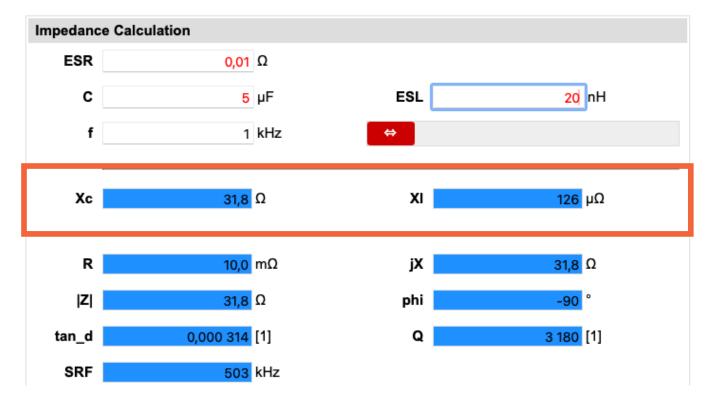
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Measurement Principle

 $\underline{Z} = \frac{\underline{U}}{\underline{I}}$ $\underline{Z} = |Z| e^{j\omega t + \varphi} \ \varphi = \arctan\left(\frac{X}{R}\right)$ $\underline{Z} = |Z| \left(\cos(\varphi) + j \sin(\varphi) \right)$ $Z = R + j(X_l + X_c)$ 3 variables R, X_l, X_c but only two equations $R = |Z| \cdot cos(\varphi)$ $X = |Z| \cdot sin(\varphi)$ with $X = X_1 + X_c$

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Does it matter? $C = 5\mu$ F, ESL = 20nH



	XI	Хс
1kHz	0.000126	31.8
10kHz	0.00126	3.18
100kHz	0.0126	0.318
1MHz	0.126	0.0318

What we all know ..



• Real capacitor has capacitance, resistance & inductance

$$|Z| = \sqrt{ESR^2 + j(2 * \pi * f * L) - \frac{1}{2 * \pi * f * C}}^2$$

- ESL depends on length and width of the chip size
- ESL impacts the Self Resonance Frequency

$$SRF = \frac{1}{2 * \pi * \sqrt{L * C}}$$

Where to start

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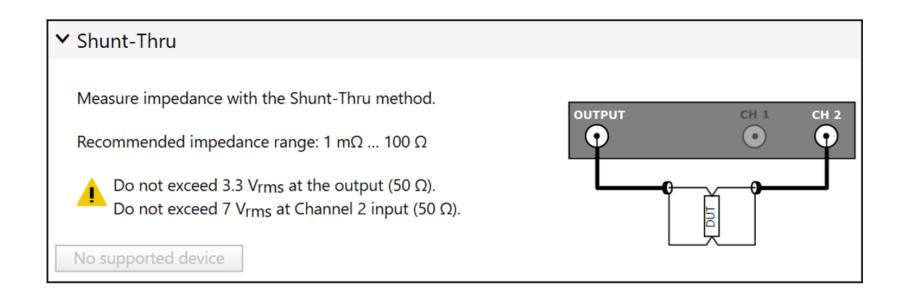


Frequency

Info	Legend	Toler	ance	Part Number	Cap.	V _{DC} *	Dielectric	Qty.	Bias (V)	Amb. (°C)	Add	Remove
	•			C4AUPBW4700M3FJ	7 uF	1200	PP	1	0	25	+	×
>	1			C4AUPBW4700M3FJ	7 uF	1200	PP	1	850	25		×
			8	C4AUPBW4700M3FJ	7 uF	1200	PP	1	850	90		×

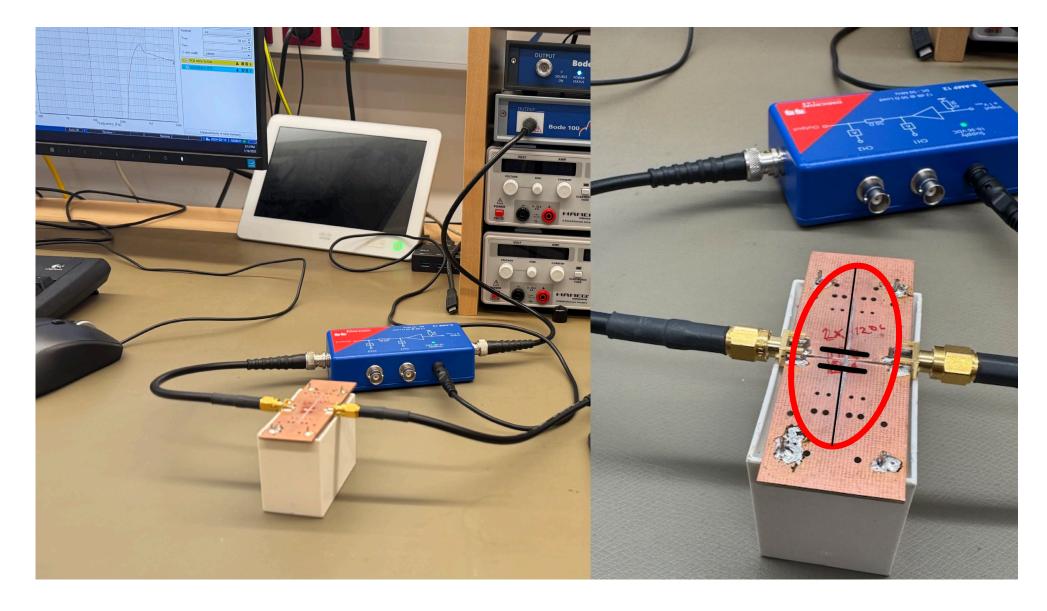
Measurement methode PCB – criteria

- Impedance is between $15m\Omega$. 300Ω
- ESR is between $6m\Omega$ and $100m\Omega$



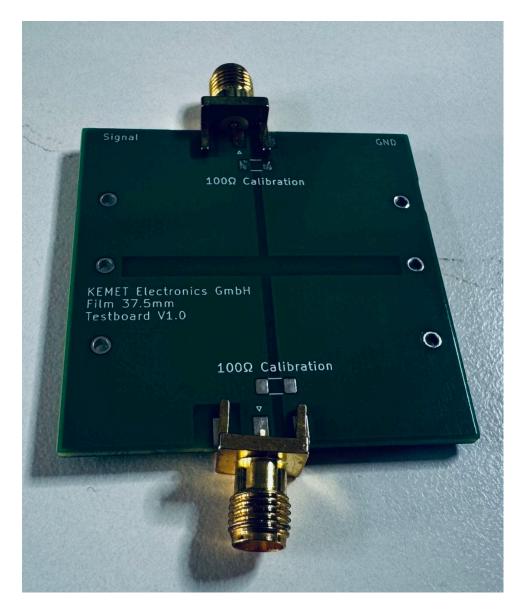
- $Z(226Hz) = 100\Omega$
- $Z(10MHz) = 680m\Omega$

First shot



The Testboard

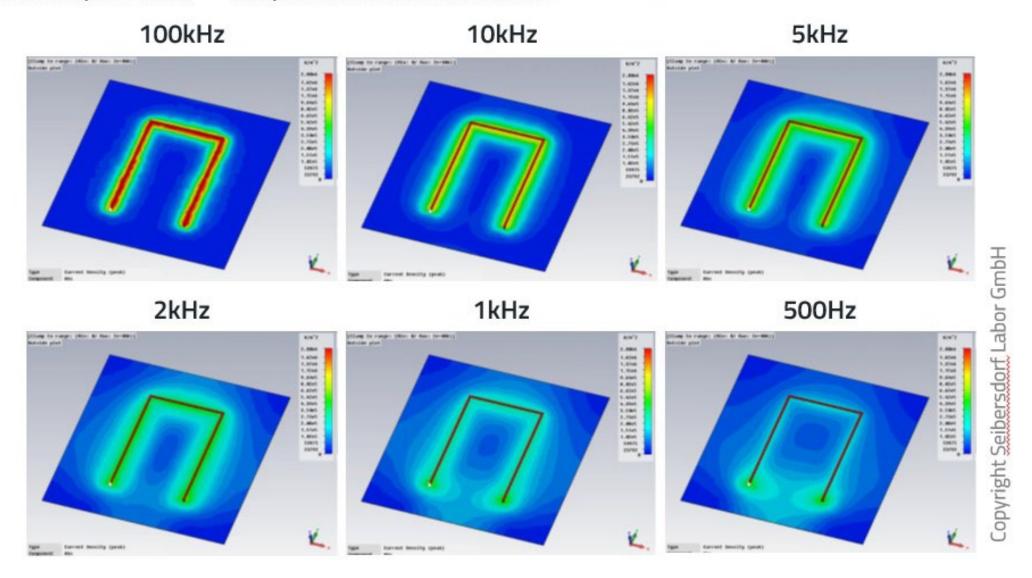
- Shunt-thru
- OSL (50Ω)
- Load is $2x \ 100\Omega$ in parallel
- SMA connector
- Symmetric layout



Coupling effects

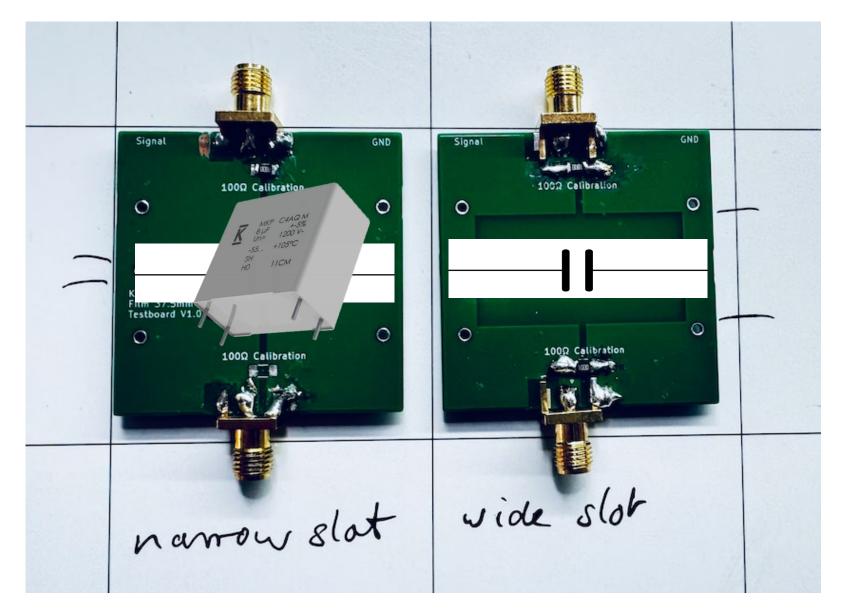


Current path with a u shaped conductor simulated in CST EMS

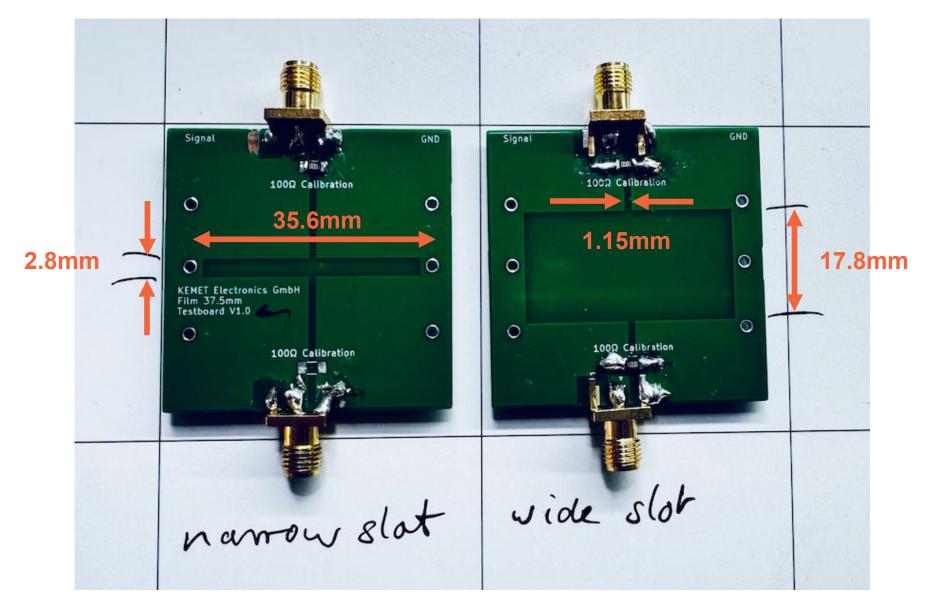


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Testboards

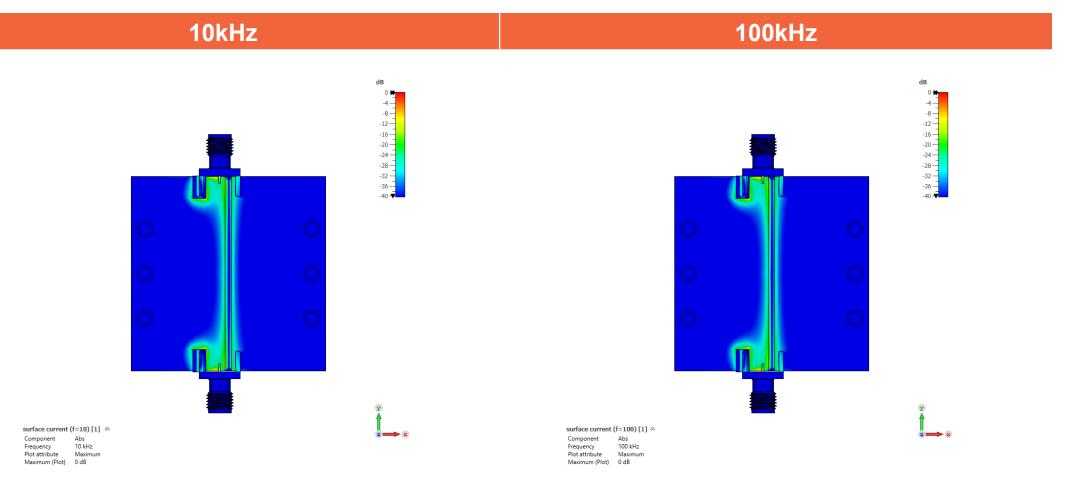


Testboards



The simulation of the Test PCB

- Slot is necessary to drive the current thru the component
- Because of the dimension of the PCB the frequency doesn't really matter



The simulation of the Test PCB (2)

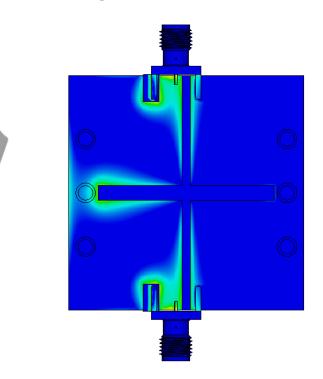
• The width of the gap controls the current flow

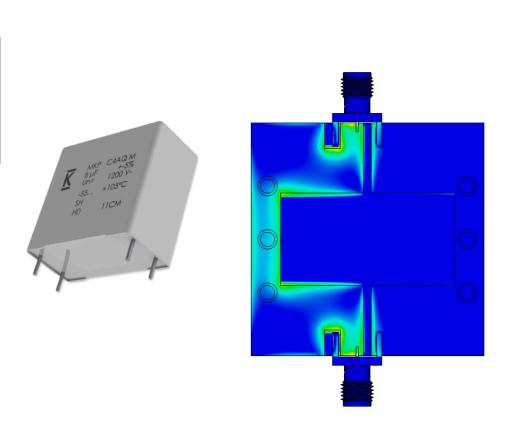
-16 -

-20 -

-24 --

- Adapt to the dimensional needs
- Error is in a range less than 10%





 surface current (f=100) [1]

 Component
 Abs

 Frequency
 100 kHz

 Plot attribute
 Maximum

 Maximum (Plot)
 0 dB

R76 MKF

5/125/THB A K8

surface current (f=100) [1] △ Component Abs Frequency 100 kHz Plot attribute Maximum Maximum (Plot) 0 dB **YAGEO**

dB

-16 —

-20 —

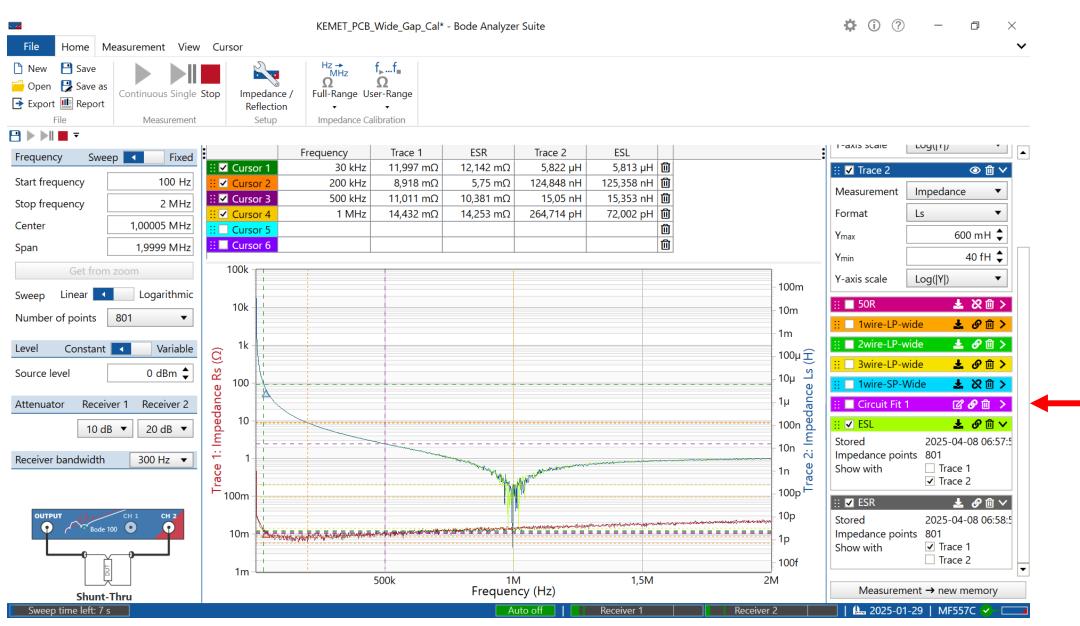
-24 —

-28 —

-32 — -36 —

28

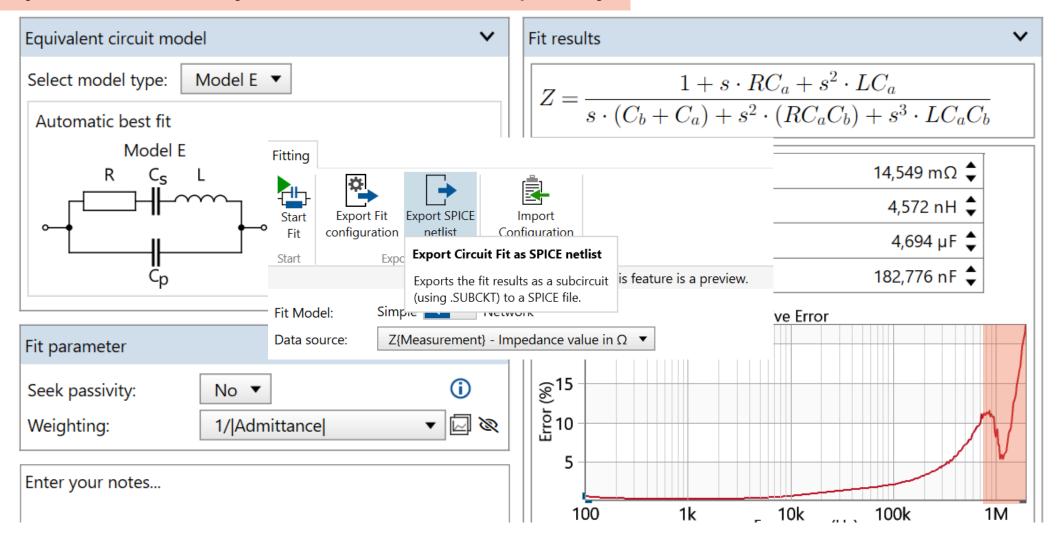
Measurement



Measurement



• Try not to use beyond resonance frequency



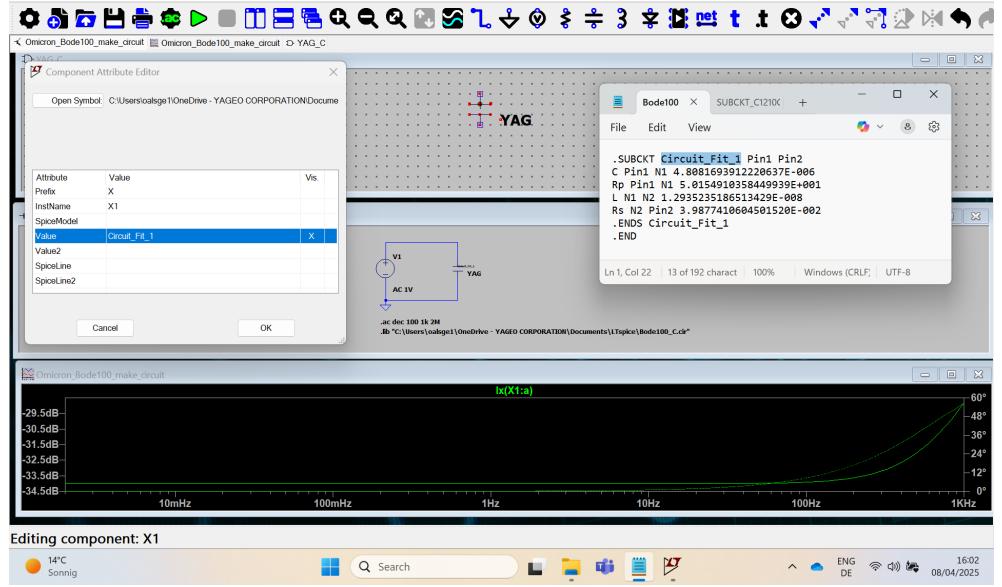
Use in other programs





LTspice - Omicron_Bode100_make_circuit

File Edit Hierarchy View Simulate Tools Window Help



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ESL reduction

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Capacitor Bobbin : 5uF 6,7um x 37,5 mm

	1 Wire/Standard Profile	1 Wire/Low Profile	
ESL [nH]	12.1	5.3	56% less
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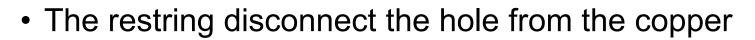
Specimen for our test



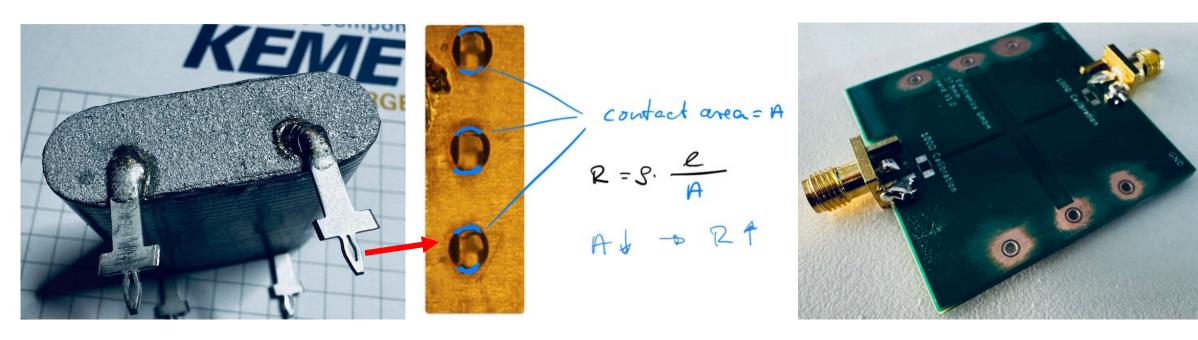
More wires reduce ESL and ESR

	1-wire SP			3-wire LP	
	T-wire SP	1-wire LP	2-wire LP	S-WIRE LP	2-PF LP
ESL/nH (2MHz)	12.1	5.3	4.7	3.1	./.
ESR/mΩ (100kHz)	7.8	4.2	3.1	2.4	./.
SRF/MHz	0.638	1.1	1.29 ¹⁾	1.27	./.

What about pressfit



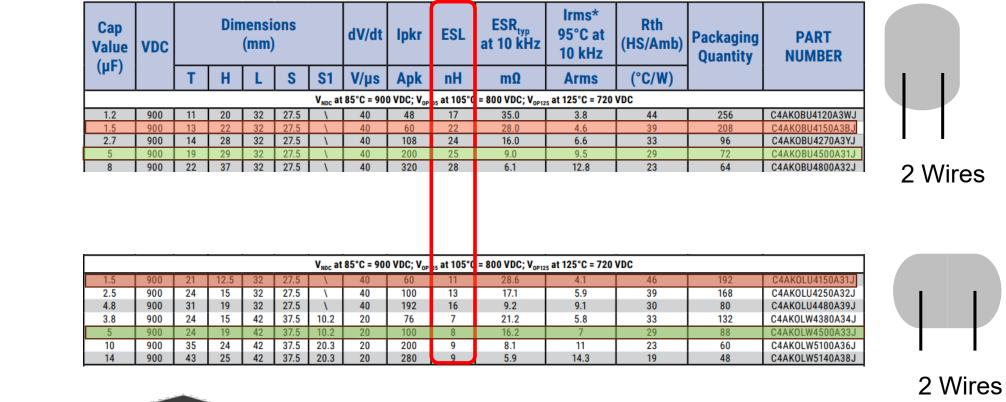
- For wire use lots of solder
- Wire Pressfit contacts I messed it up new PCB already ordered



Low ESL: Low profile 4 pins DC Link

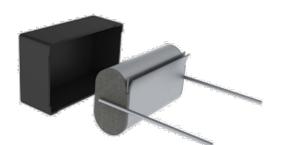


Table 1 – Ratings & Part Number Reference cont.





1 Wire



2 Wires Low Profile

Wrap up



- It was fun to work on my own first testboard
- Very helpful to have a community and contacts you can talk with
- The pressfit will be investigate when the new boards arrive
- There a lot more to do on the components characterization and ...

Enough material for future investigations





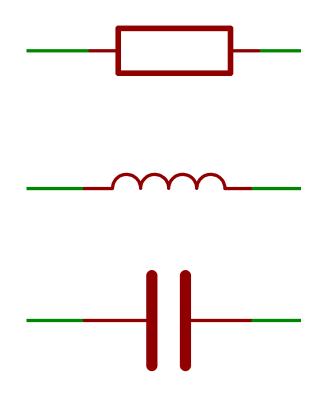
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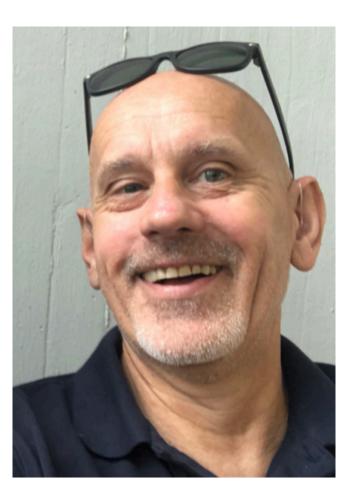
Acknowledgement



- Melanie Klenner, Korker for the excellent simulation of the PCB
- Florian Hämmerle, **OMICRON** for thehints and support for the investigation
- Federico Fantini and Robert Airi YAGEO for the insight and samples

Thank you!謝謝你!





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