FUTURE ELECTRONICS

A WT Microelectronics Company

Simulating Power Factor Correction Stages in Single- and Three-Phase Networks

Christophe Basso
Business Development Manager
IEEE Professional Member

OMICRON LAB

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Agenda

- Notions of Power Factor
- PFC Architectures
- Processing Power – Single Phase
- Processing Power – Three Phases

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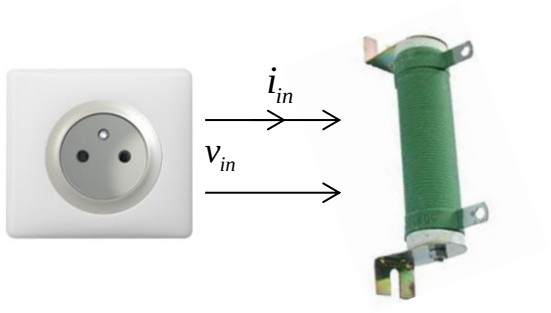
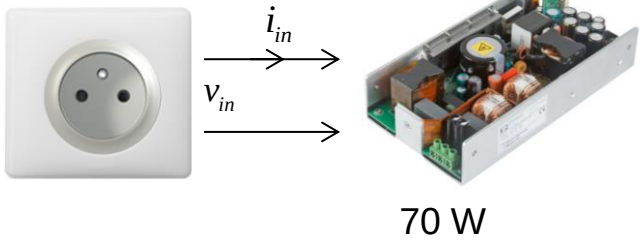
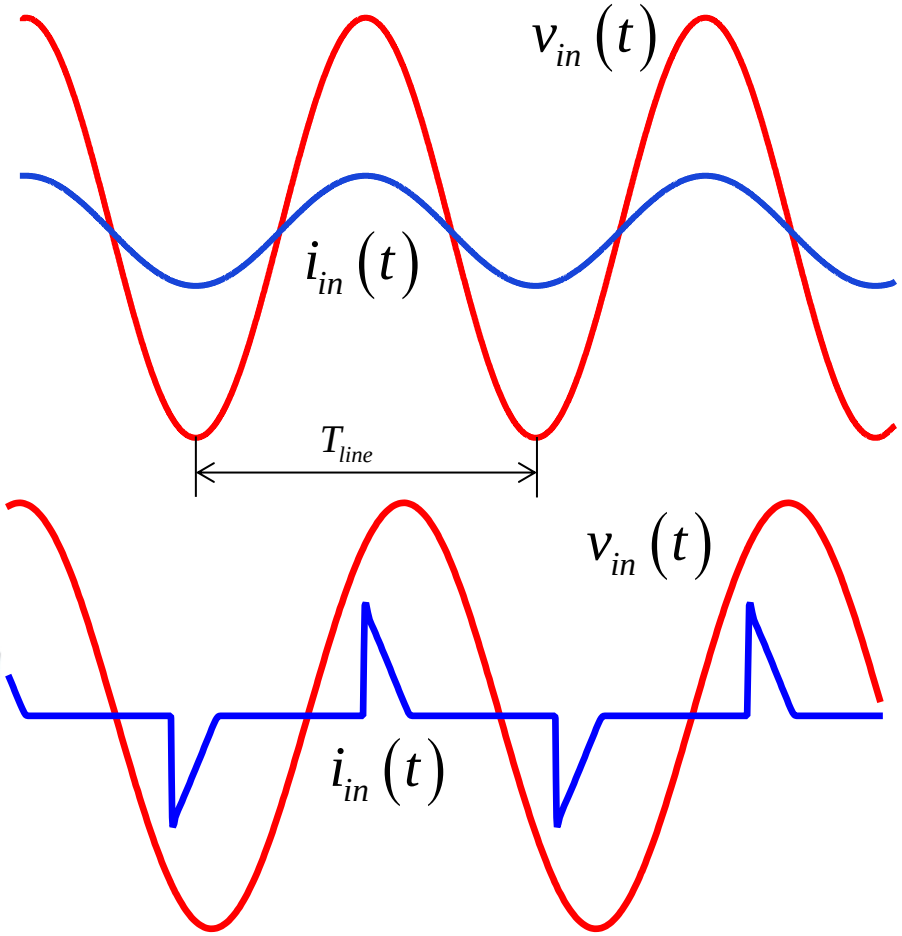
- Notions of Power Factor
- PFC Architectures
- Processing Power – Single Phase
- Processing Power – Three Phases

What is Power Factor?

- The goal of any power factor correction circuit is to emulate a resistance
  - ➢ The absorbed current must be sinusoidal and in phase with the input voltage







$$p_{in}(t) = i_{in}(t)v_{in}(t) = \frac{v_{in}(t)}{R}v_{in}(t)$$

$$P_{in,avg} = \frac{1}{T_{line}}\int_0^{T_{line}} p_{in}(t)\cdot dt = 70\ \text{W}$$

$$P_{in,app} = V_{in,rms}\cdot I_{in,rms} = 85\times 823m = 70\ \text{VA}$$

$$\text{PF} = \frac{\text{active power}}{\text{apparent power}} = \frac{[\text{W}]}{[\text{V}\cdot\text{A}]} = 1$$

$$P_{in,avg} = \frac{1}{T_{line}}\int_0^{T_{line}} p_{in}(t)\cdot dt = 70\ \text{W}$$

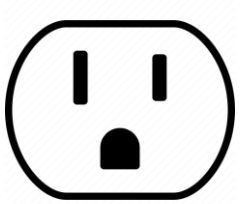
$$P_{in,app} = V_{in,rms}\cdot I_{in,rms} = 85\times 1.46 = 124\ \text{VA}$$

$$\text{PF} = \frac{\text{active power}}{\text{apparent power}} = \frac{[\text{W}]}{[\text{V}\cdot\text{A}]} = 0.56$$

What is the Impact of a Low PF?

- Assume a 250-W load absorbed by an equipment from a 110-V 15-A ac outlet
- With a PF of 0.56, the current is 250/110/0.56 ≈ 4 A rms

✓ You can safely connect a maximum of 3 devices (15/4 = 3.75)



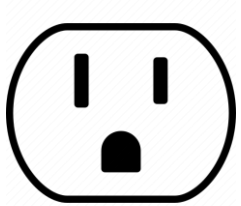
110 V – 15 A
P_{max} = 1.65 kVA

$I_{in,rms}$ = 4 A

x 3

250 W – PF = 0.56

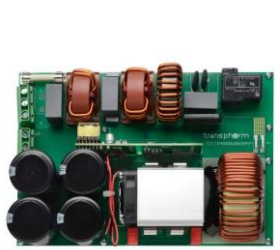
- Add a front-end power factor correction stage to bring PF close to unity



110 V – 15 A
P_{max} = 1.65 kVA

$I_{in,rms}$ = 2.3 A

x 6



PFC

250 W – PF = 0.99

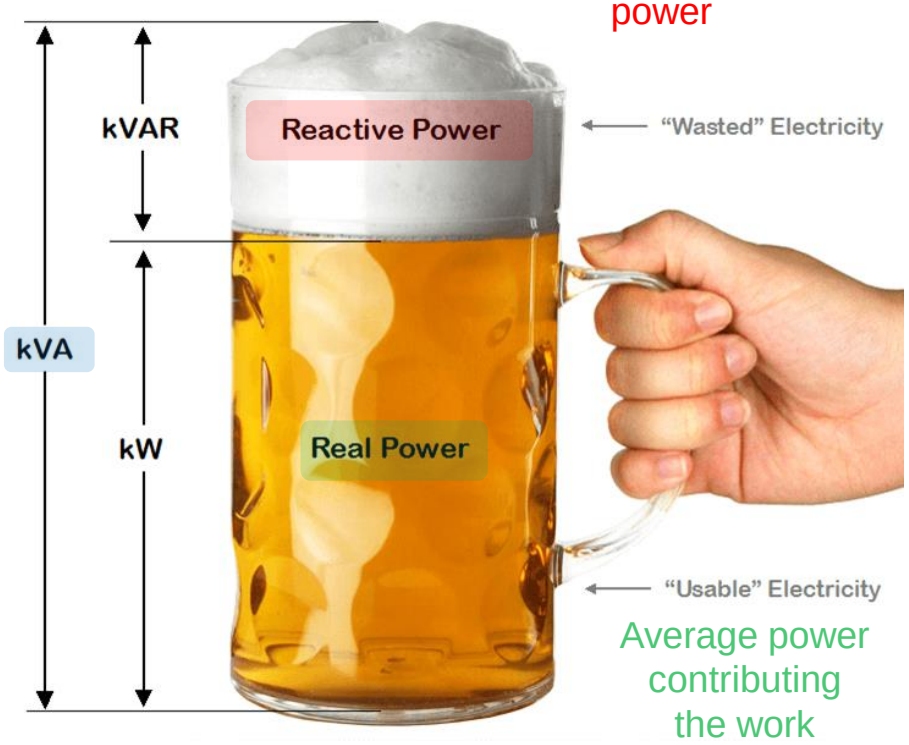
You can safely connect 6 workstations

Explaining Power Factor with Beer

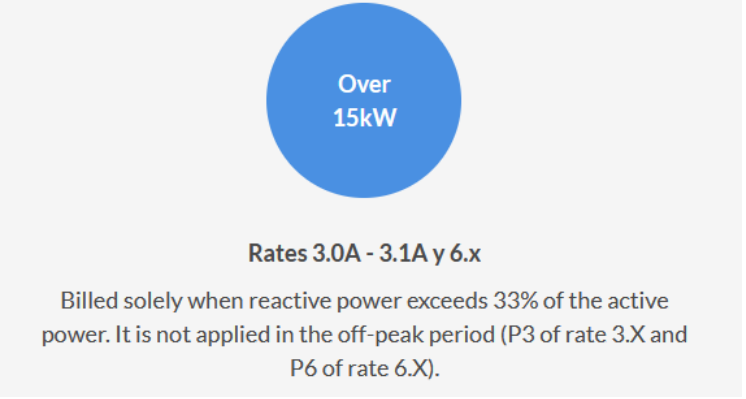
- A low power factor will force the production and circulation of a higher rms current
- Electric wires can overheat and utility companies push for power factor correction
- ✓ A glass of beer with an excessive foam can help understand the issue

Useless circulating power

Apparent power S supplied by the utility



Average power contributing the work



[VA] [W] [VAR]

$$S = P + jQ$$

$$\left|\frac{P}{PF}\right| = \sqrt{P^2 + Q^2}$$

$$Q = P\sqrt{\frac{1}{\mathrm{PF}^2} - 1}$$

If PF < 0.95

$$Q\,[\mathrm{VAR}] > 33\% \cdot P\,[\mathrm{W}]$$

https://www.iberdrola.es/en/homeowners-associations/information/reactive-power

Power Factor and Distortion

- Power factor depends on two parameters:

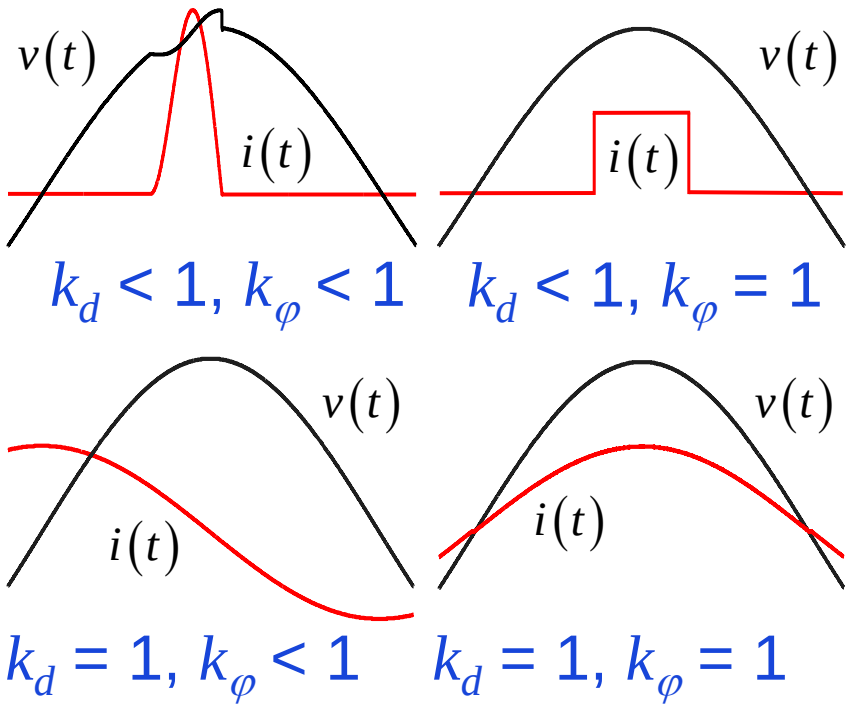
$$PF = \frac{I_{1,rms}}{I_{rms}} \cos\varphi = k_d k_\varphi$$

Fundamental rms current

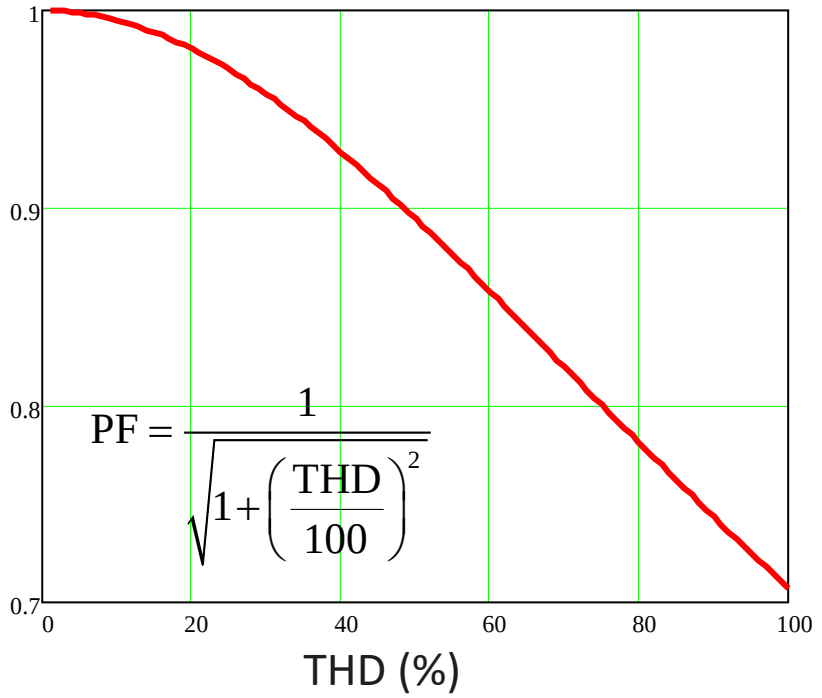
Total rms current

✓ k_d represents the distortion factor

✓ k_φ designates the displacement angle



For a displacement angle k_φ of 1:

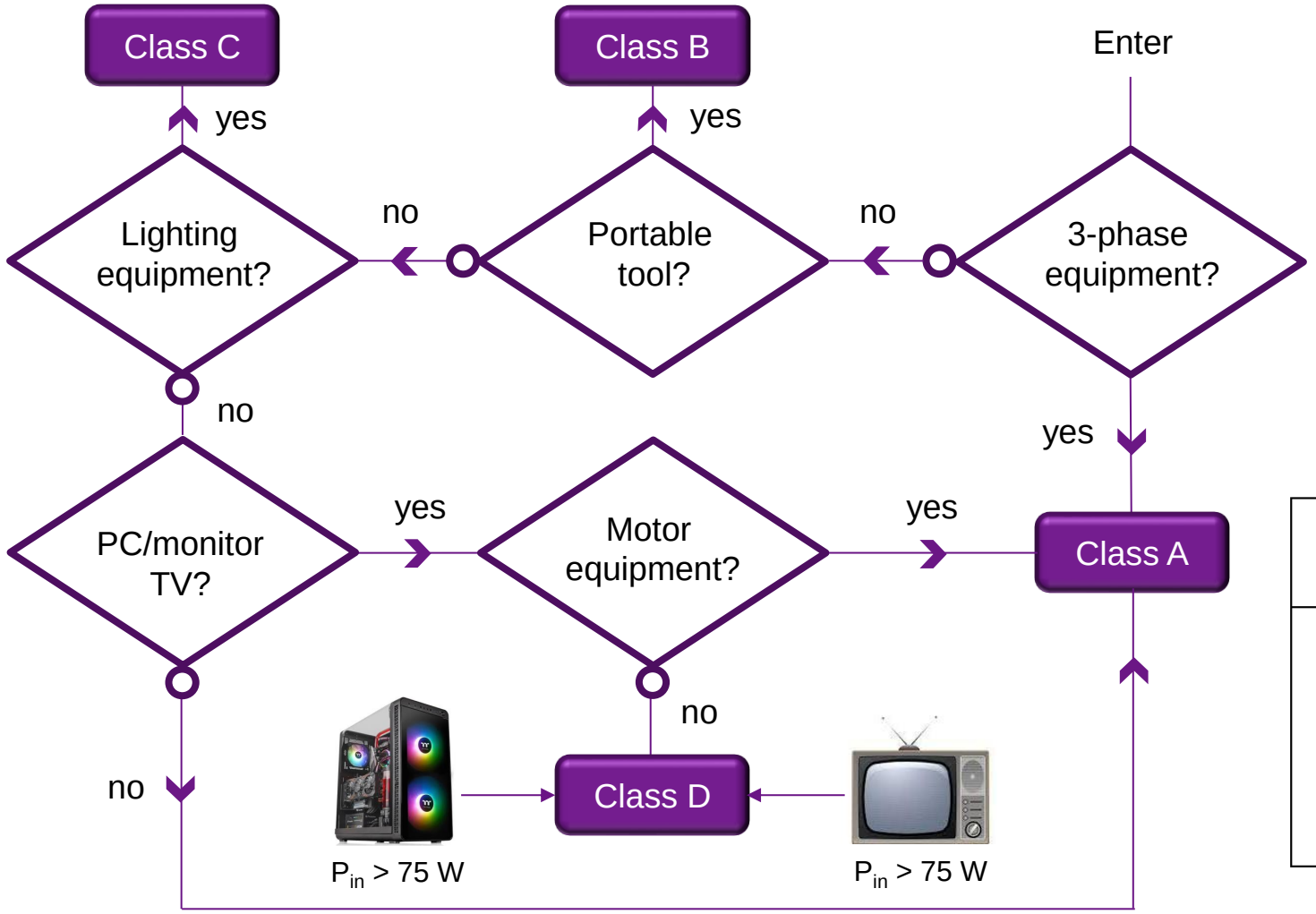


THD = 30%, PF = 0.958
THD = 10% PF = 0.995
THD = 5% PF = 0.999

Check harmonics limits according to IEC1000-3-2

Equipment Compliance

- The standard EN61000-3-2 defines the class of equipment and associated limits



NORME INTERNATIONALE
INTERNATIONAL STANDARD

CEI IEC 61000-3-2

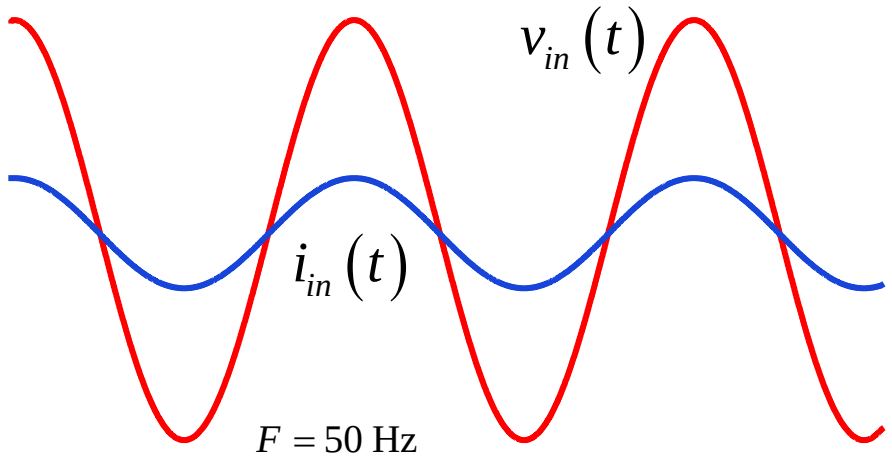
Deuxième édition
Second edition
2000-08

Class D limits

Rang harmonique n	Courant harmonique maximal autorisé par watt mA/W	Courant harmonique maximal autorisé A
3	3,4	2,30
5	1,9	1,14
7	1,0	0,77
9	0,5	0,40
11	0,35	0,33
$13 \leq n \leq 39$ (harmoniques impairs seulement)	$\frac{3,85}{n}$	Voir tableau 1

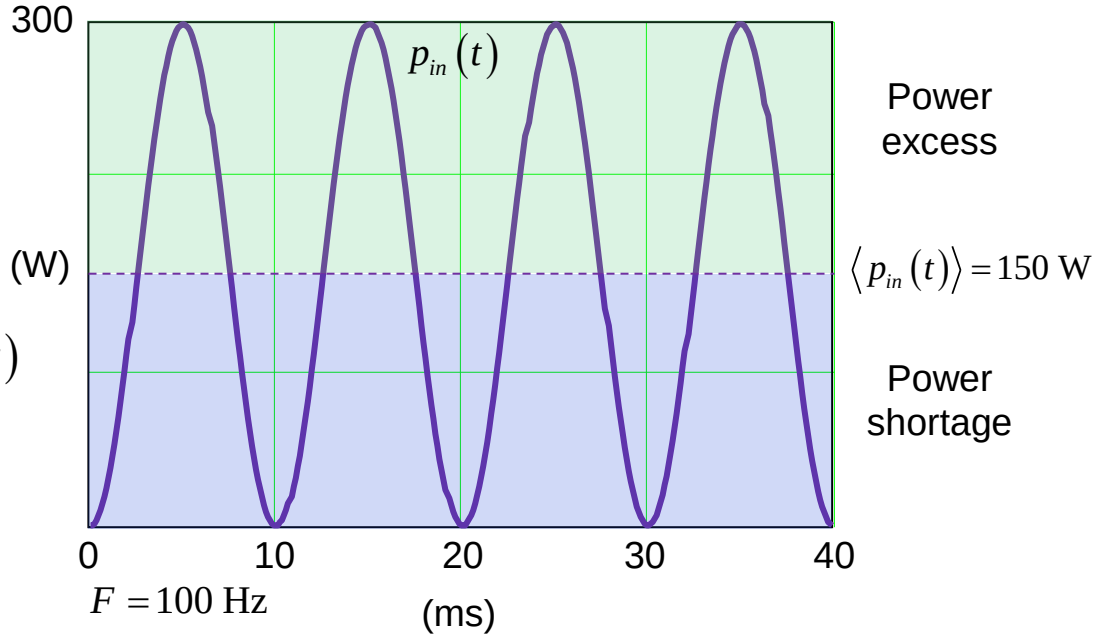
Storage Need in a Single-Phase Grid

- The goal of a PFC front-end converter is to emulate a resistive load
- The power of a single-phase ac source feeding a resistance involves a squared sinewave

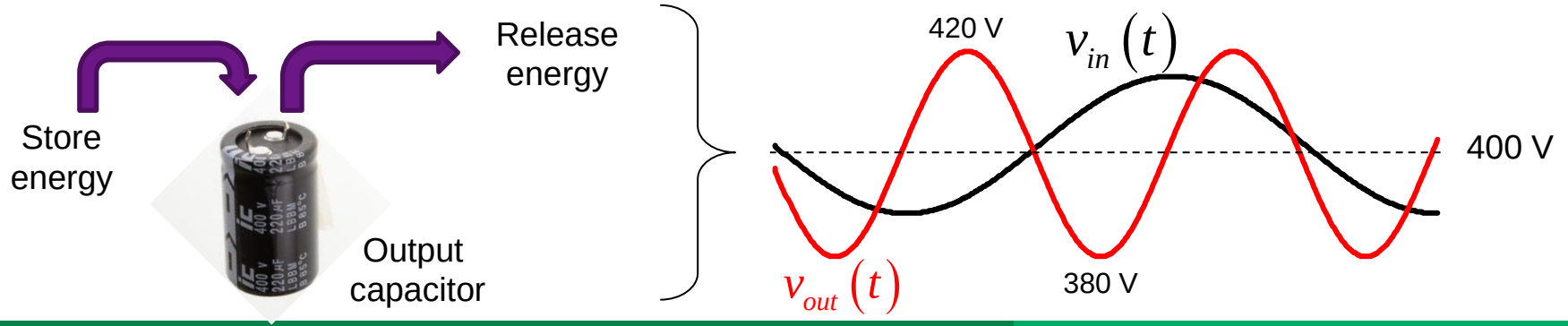


$P_{in} = 150$ W

$p_{in}(t) = v_{in}(t) \cdot i_{in}(t)$



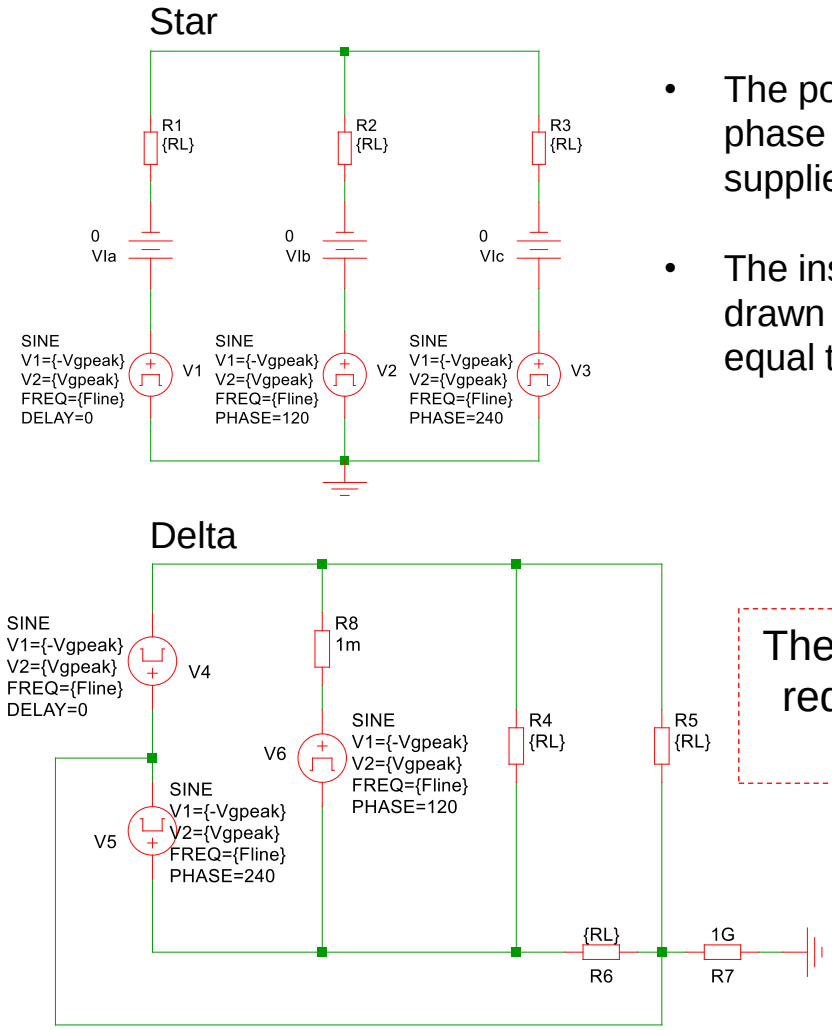
- Active power factor stores and release energy



✓ Output voltage ripple is twice the input frequency

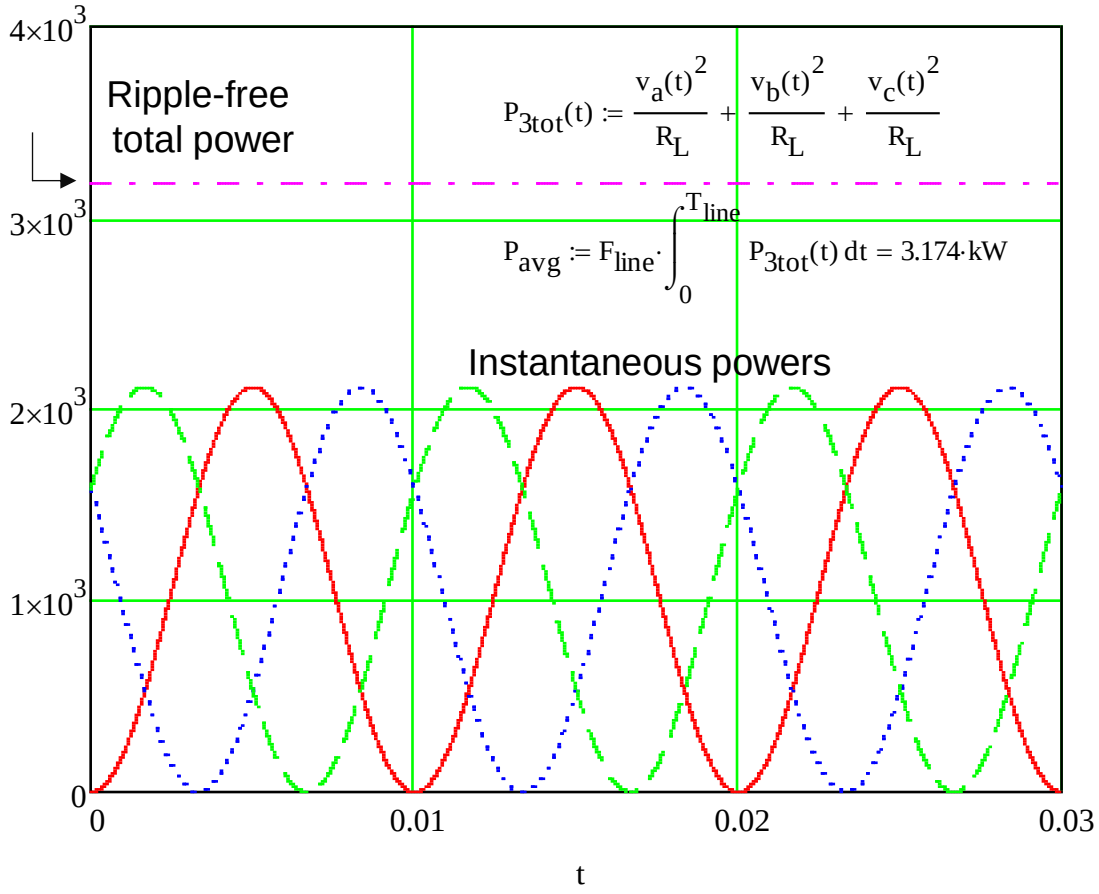
Instantaneous Power in a 3-Phase Grid

- The total power in a three-phase system is the sum of individual powers



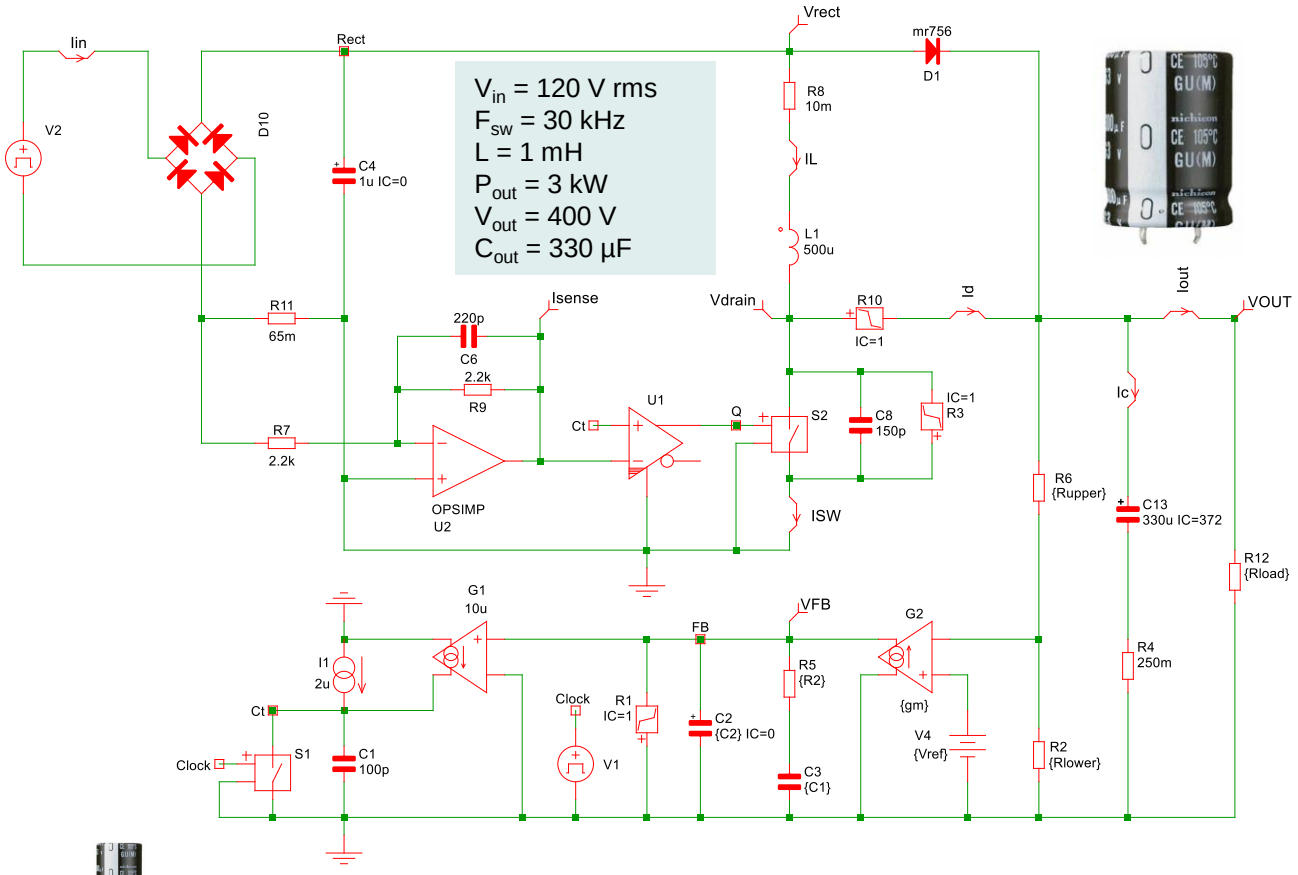
- The power drawn from the 3-phase grid is the sum of powers supplied by phases a, b and c
- The instantaneous power drawn from the grid is a flat line equal to 3 x 1.058k = 3.174 kW

The need for storage is reduced in a 3-phase PFC

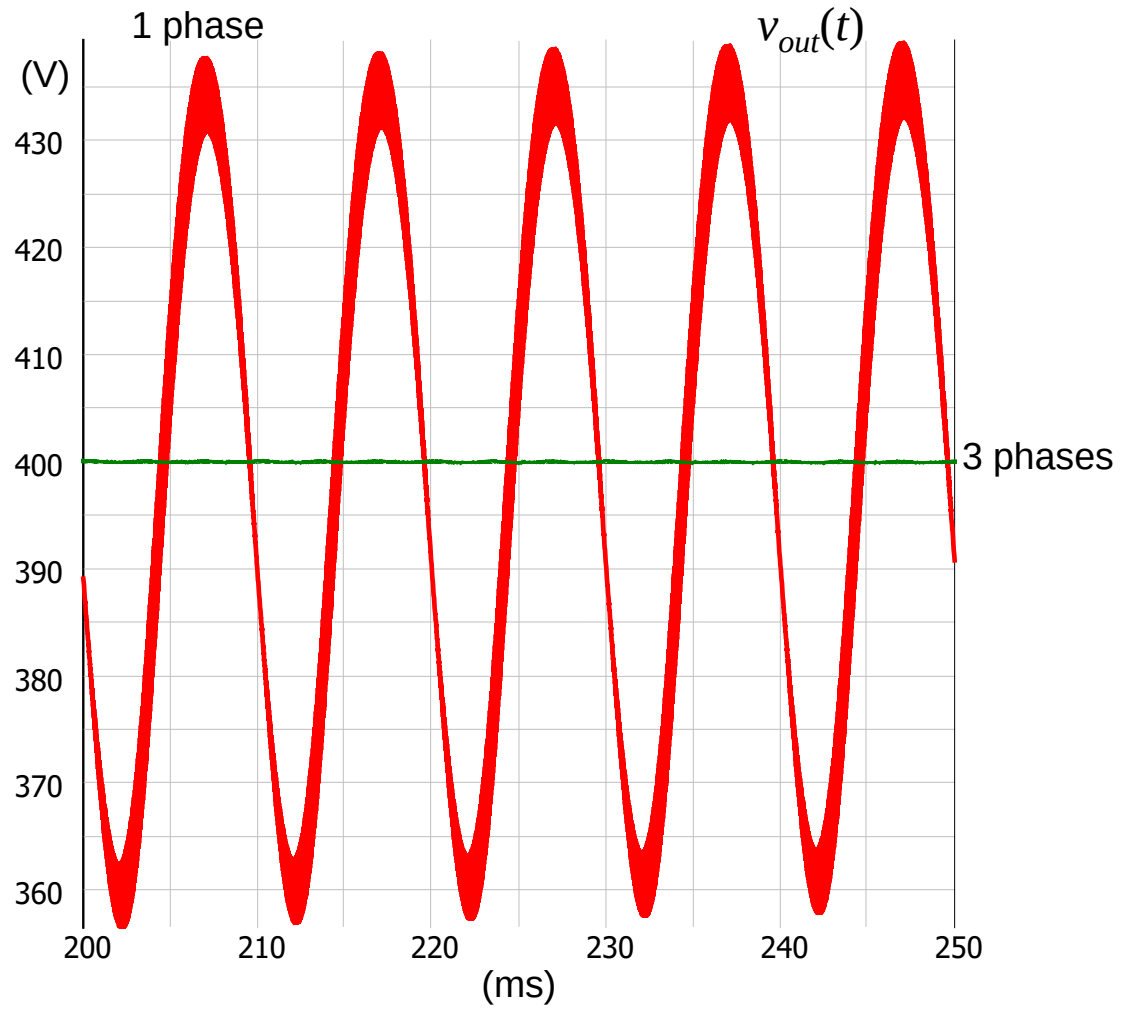


Output Ripple in 1- and 3-Phase PFCs

- Below is the comparison between a 3-kW PFC output ripple in a 1- or 3-phase grid

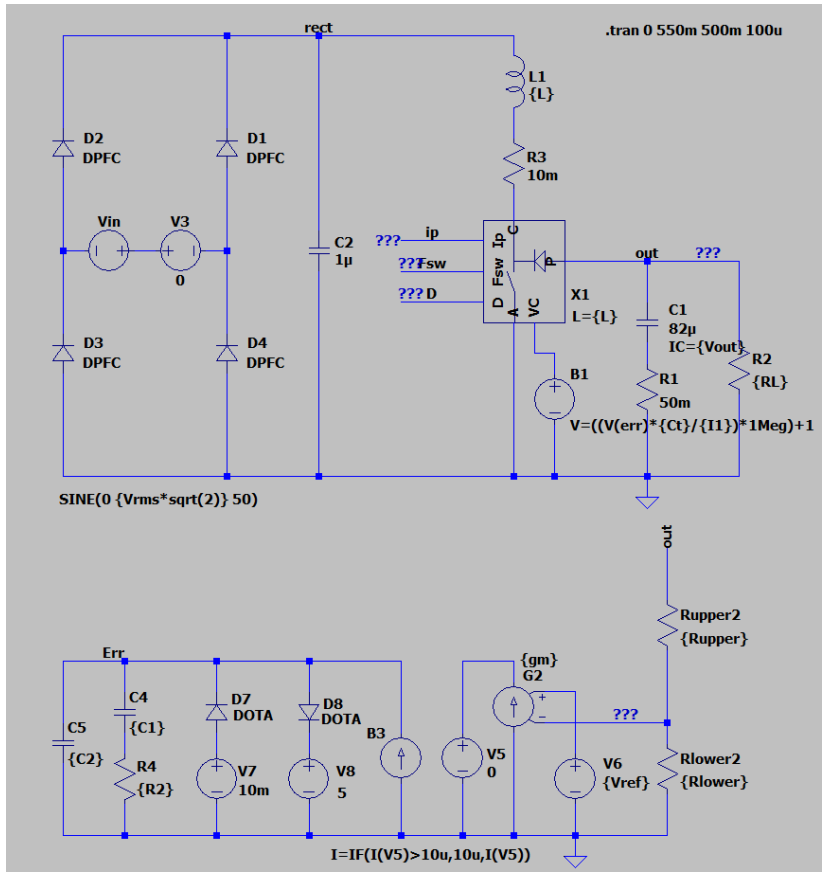


1 phase: strong low-frequency rms component
3 phases: no low-frequency component

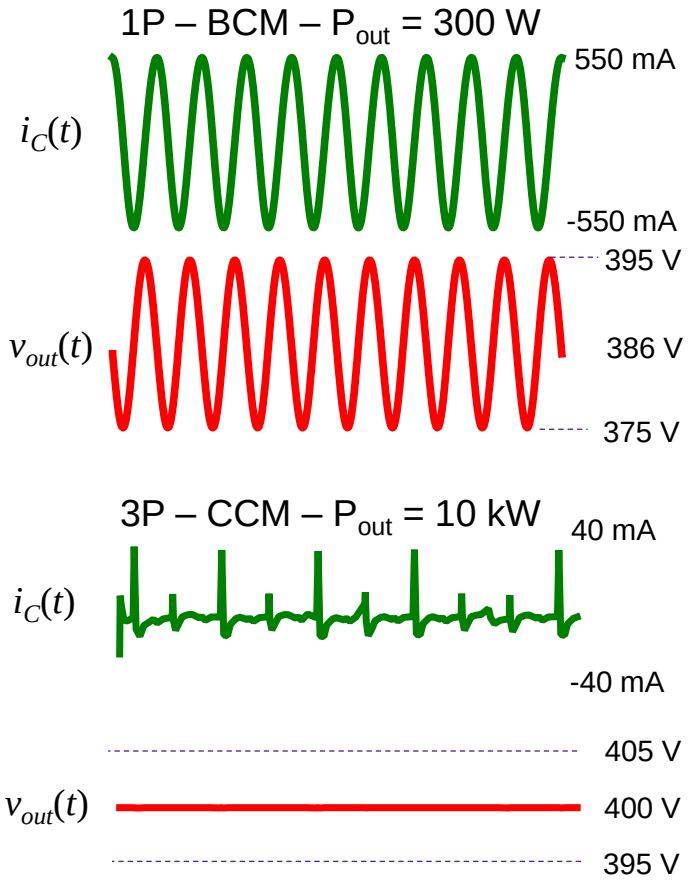


Averaged Simulations for the Ripple

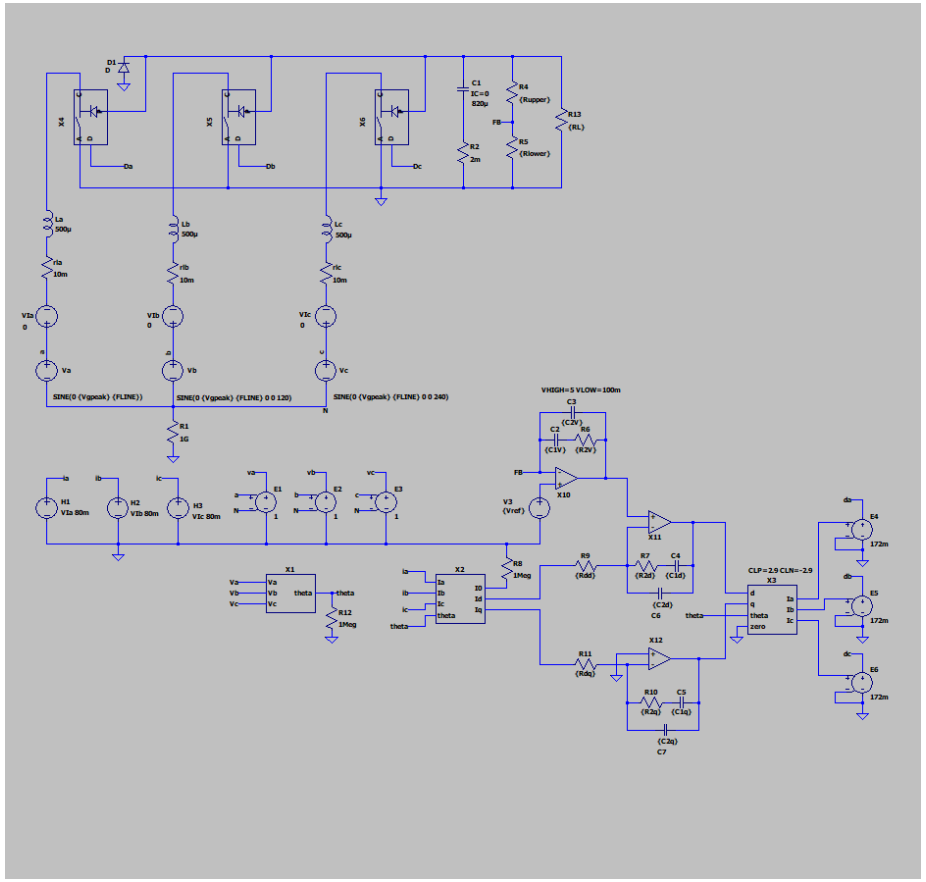
- Part of the output capacitor rms current depends on the low-frequency component
  - ➢ There is no low-frequency ripple in a balanced, 3-phase, active PFC



Single-phase BCM averaged model



No low-frequency ripple in 3-phase



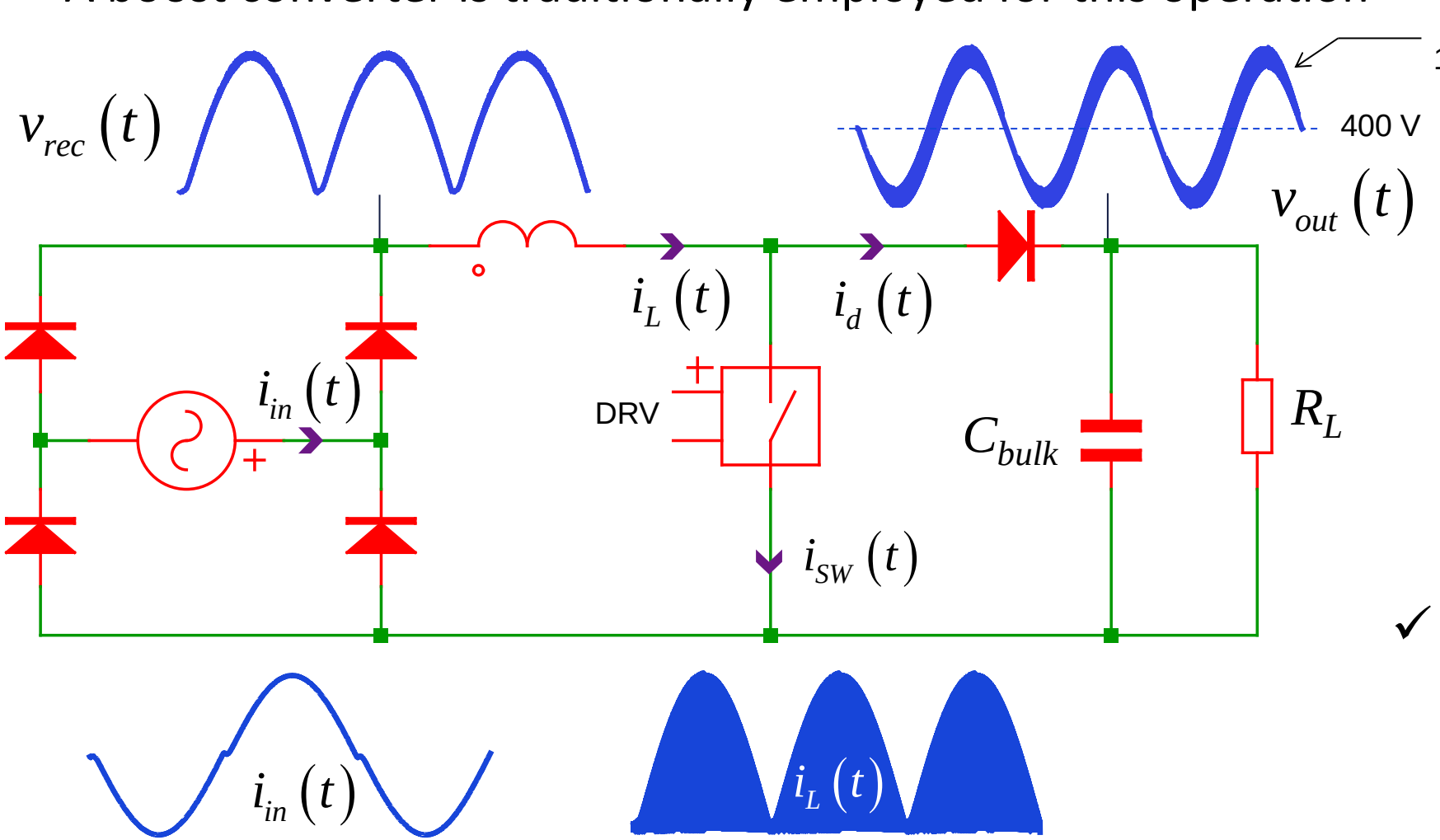
Three-phase BCM averaged model

Agenda

- Notions of Power Factor
- PFC Architectures
- Processing Power – Single Phase
- Processing Power – Three Phases

Power Factor Correction – One Phase

- An active PFC forces a sinusoidal current absorption in phase with the voltage
- A boost converter is traditionally employed for this operation



✓ The rectified input voltage sets the inductor current envelope

✓ The inductor current is adjusted to match power demand

No Diode Bridge with Totem-Pole PFCs

- The bridge hampers overall efficiency with two permanently-conducting diodes

$$P_d \approx 2V_f I_{d,avg}$$

$$I_{F,avg} = \frac{2}{\pi}\frac{\sqrt{2}P_{out}}{V_{ac,LL}\eta}$$

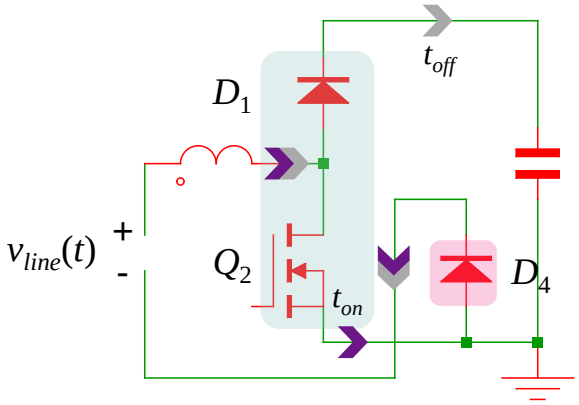
$$P = 300\ \text{W}$$
$$\eta = 100\%$$
$$V_{ac,LL} = 90\ \text{V rms}$$

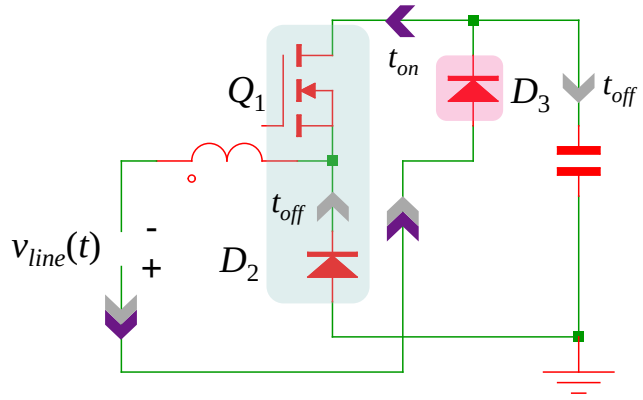
$$P_d \approx 5\ \text{W}$$
$$\text{Eff. loss} \approx 1.7\%$$

- The totem-pole PFC processes the positive and the negative input cycles

GaN
SiC

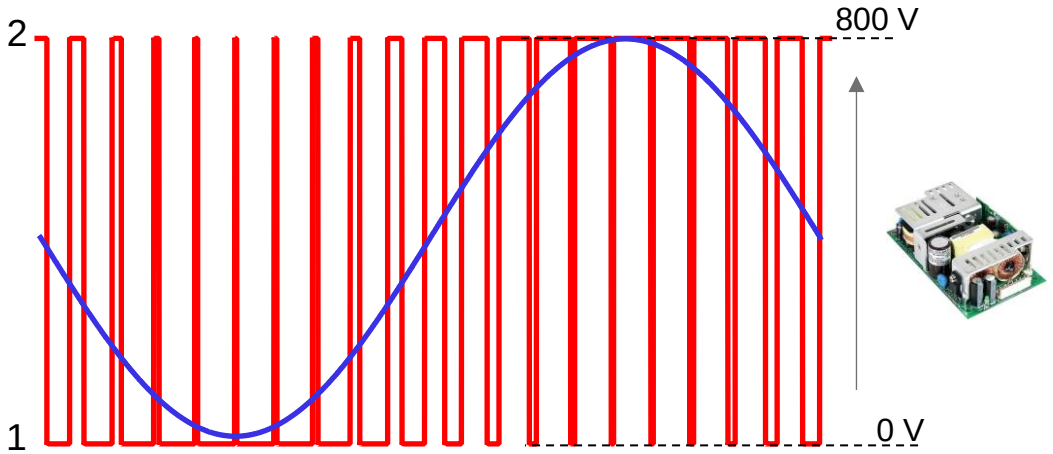
- ✓ Q_1/Q_2 swap roles between switches and diodes
  - They operate at high frequency: *fast leg*
- ✓ D_3/D_4 are active during half of the line cycle
  - This is the *slow leg* which can be sync-rectified



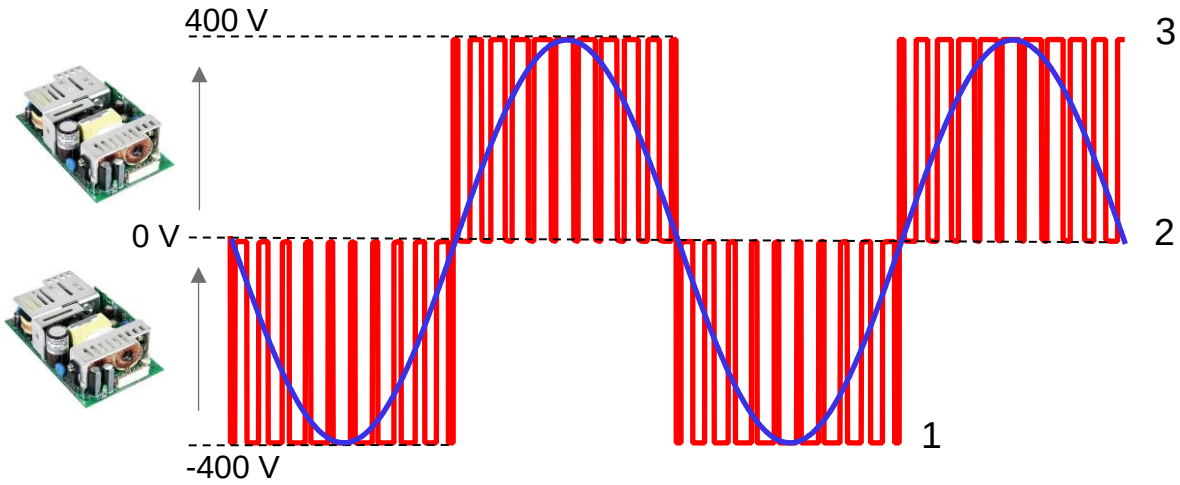


Multi-Level Converters

- The classical boost structure delivers a single output voltage of 800 V
- ✓ It is called a *two-level* inverter, meaning the switching pattern is unipolar
- An intermediate 0-V level can be added to form a *three-level* inverter
- ✓ The switching pattern becomes bipolar and transitions via a 0-V state



2-level switching pattern

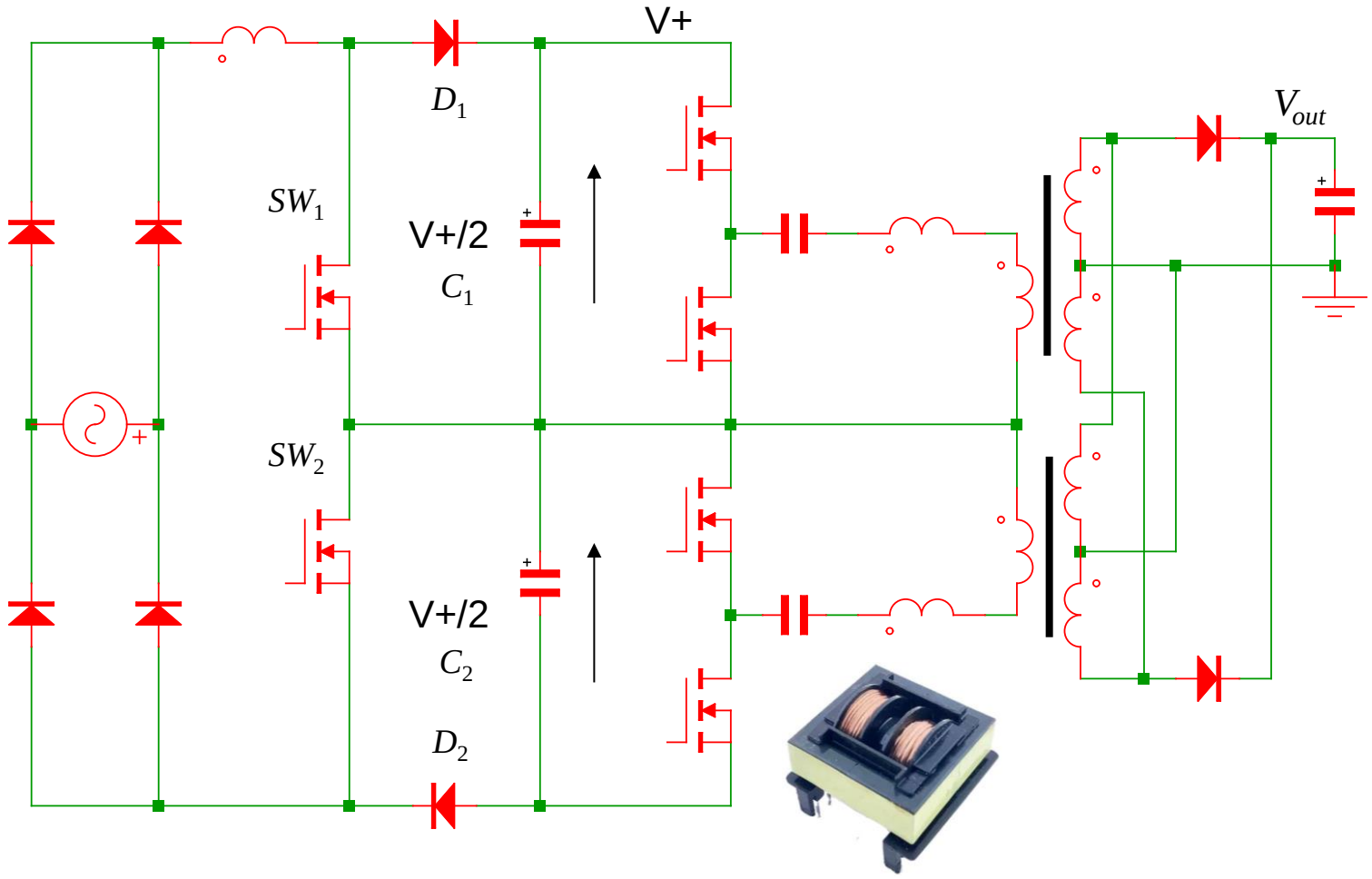


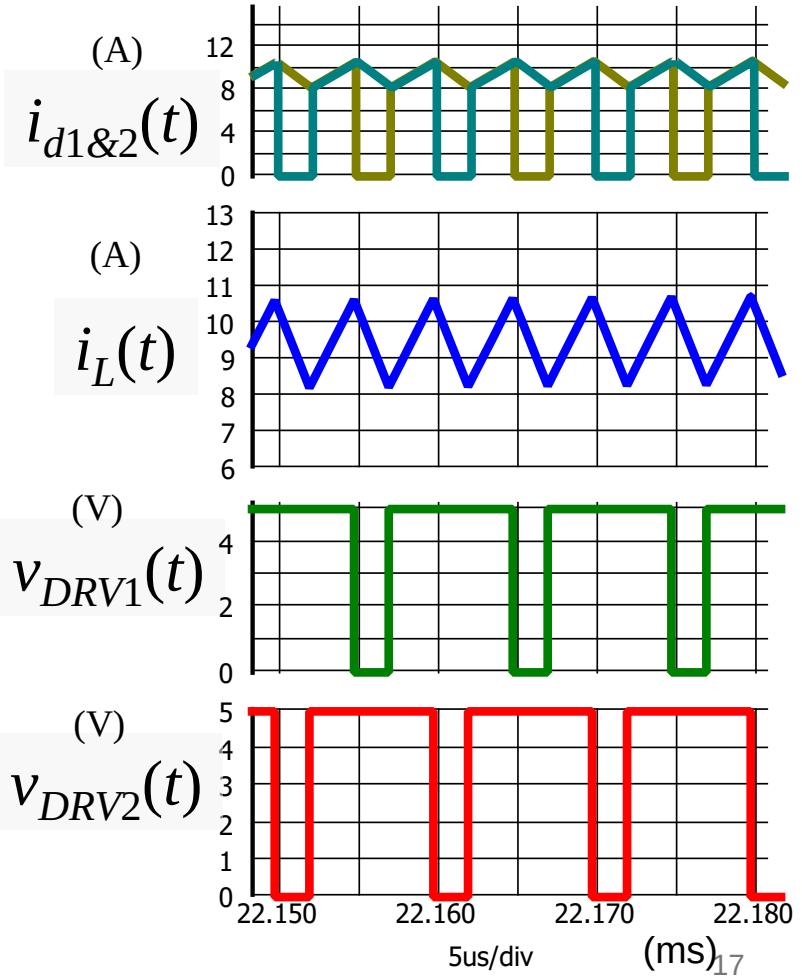
3-level switching pattern

Stack converters supplied by 400-V rails and reduce semiconductors stress

Stacking High-Power Converters

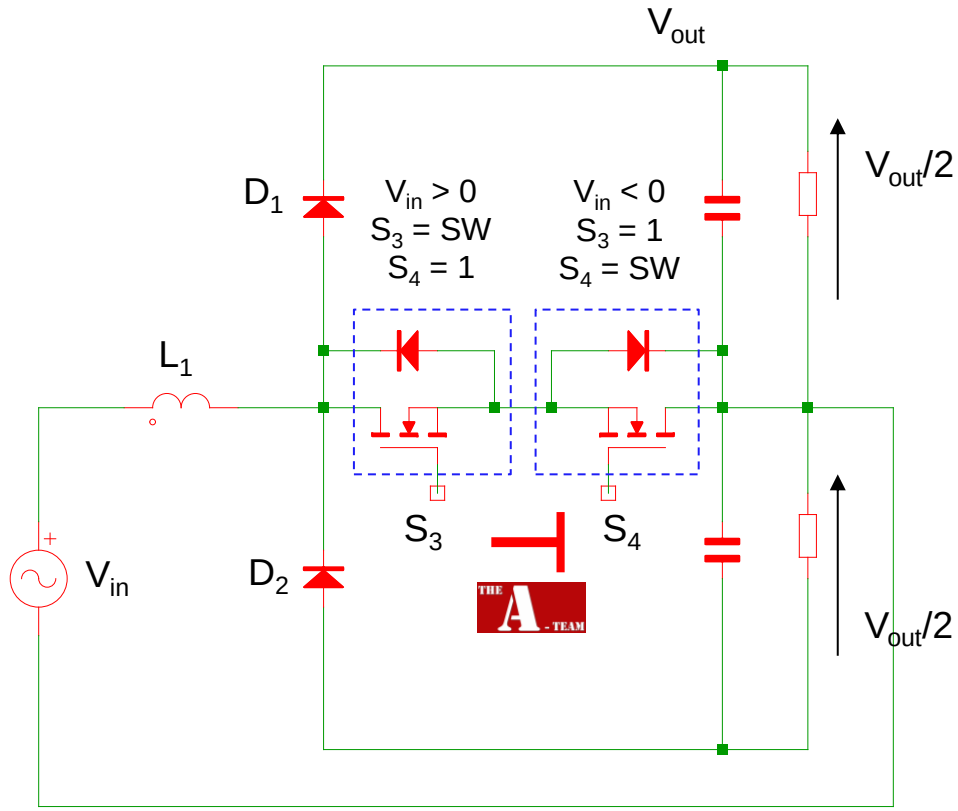
- The two dc rails of equal values let you use semiconductors of lower voltage
- The output transformers can then be serialized or paralleled for more power





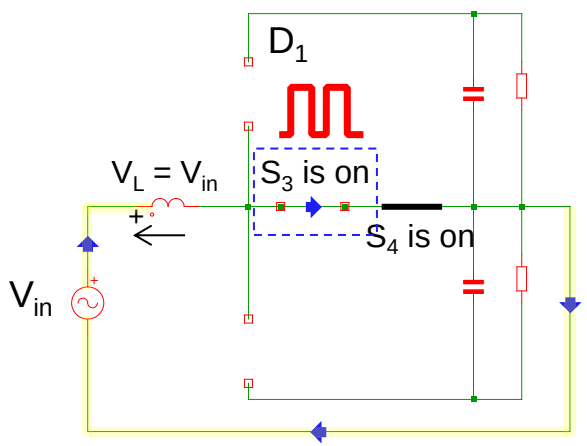
Three-Level T-Type PFC

- A simple 3-level PFC can be implemented by adding a bidirectional switch
- The two T switches operate at high frequency and block $V_{out}/2$

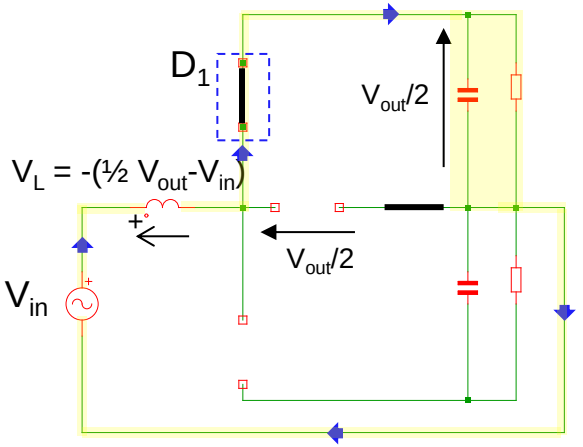


- The off-time voltage is half of the output voltage

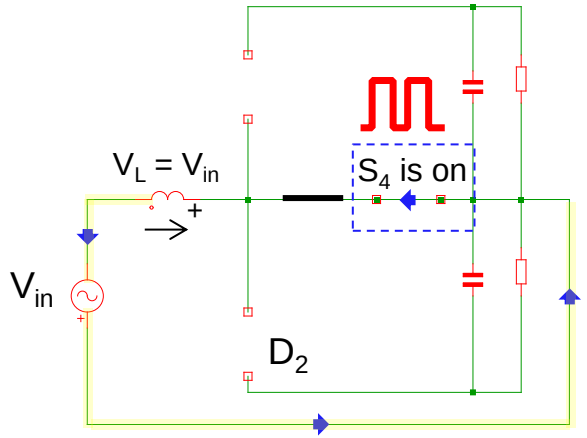
✓ Design with a smaller inductor for same ripple



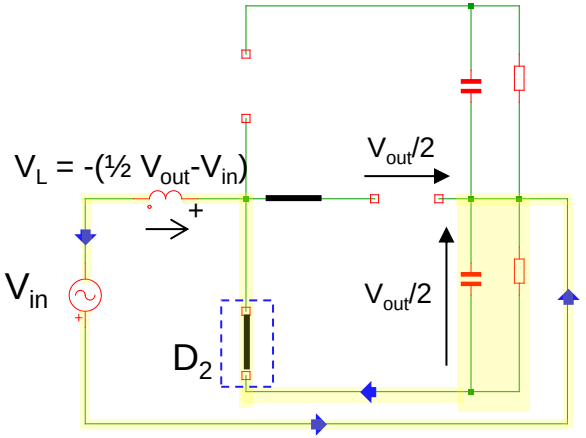
Positive ½ cycle – magnetization phase



Positive ½ cycle – demagnetization phase



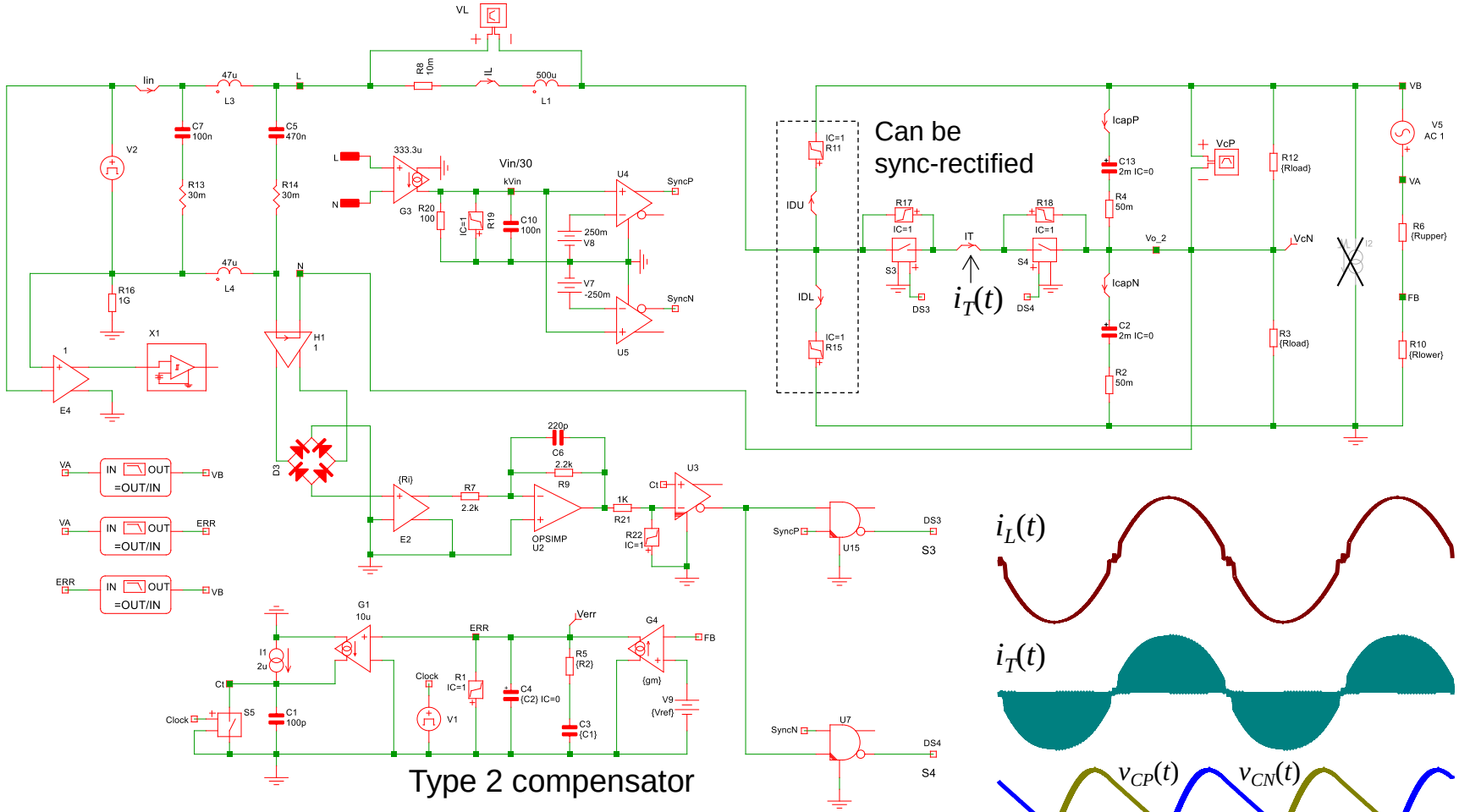
Negative ½ cycle – magnetization phase



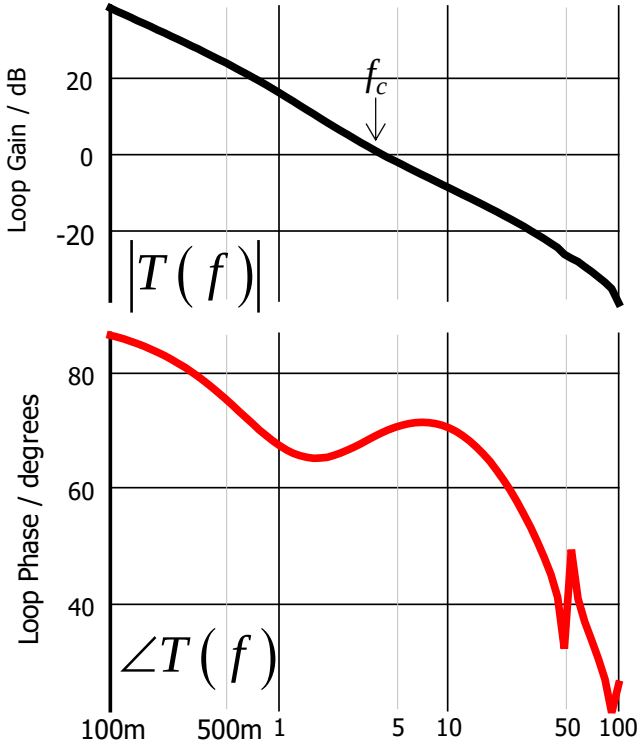
Negative ½ cycle – demagnetization phase

SIMPLIS Delivers the AC Response

- You can stabilize and test the transient response with the same circuit



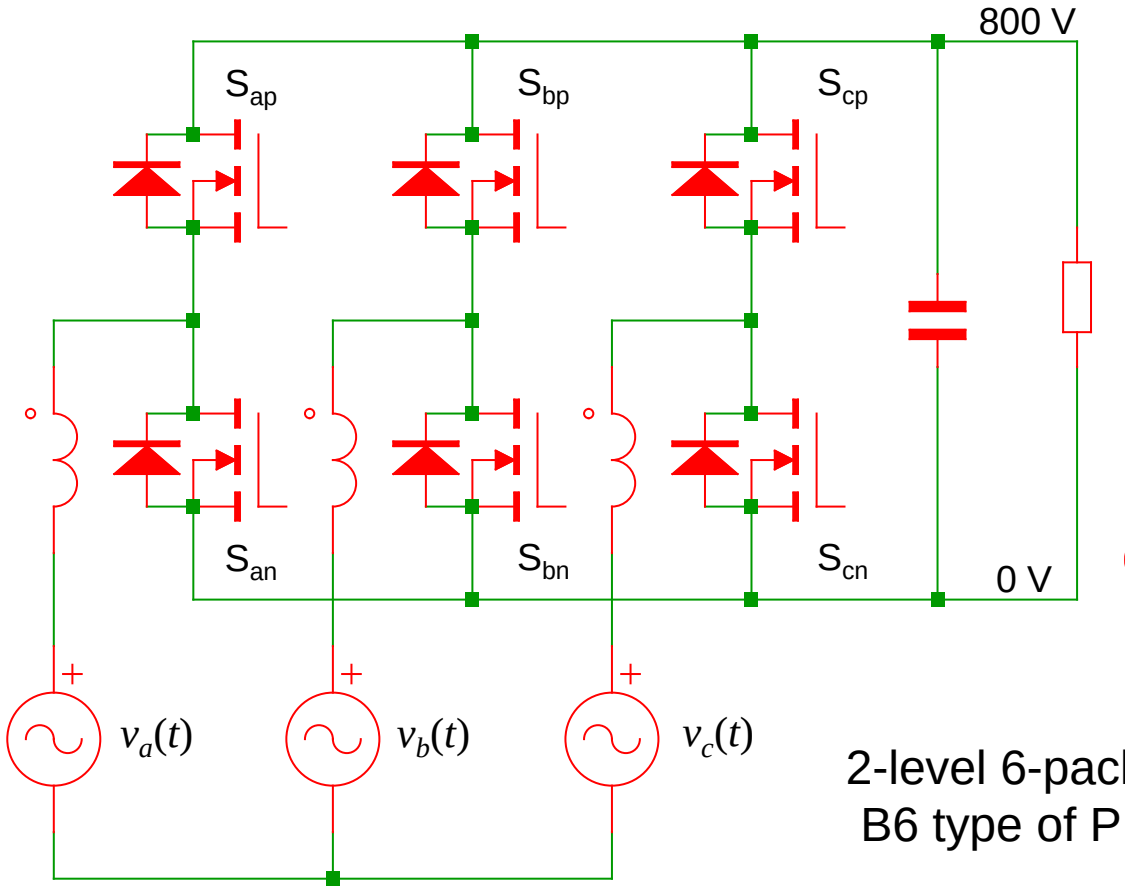
V_{in} = 230 V rms P_{out} = 1.5 kW



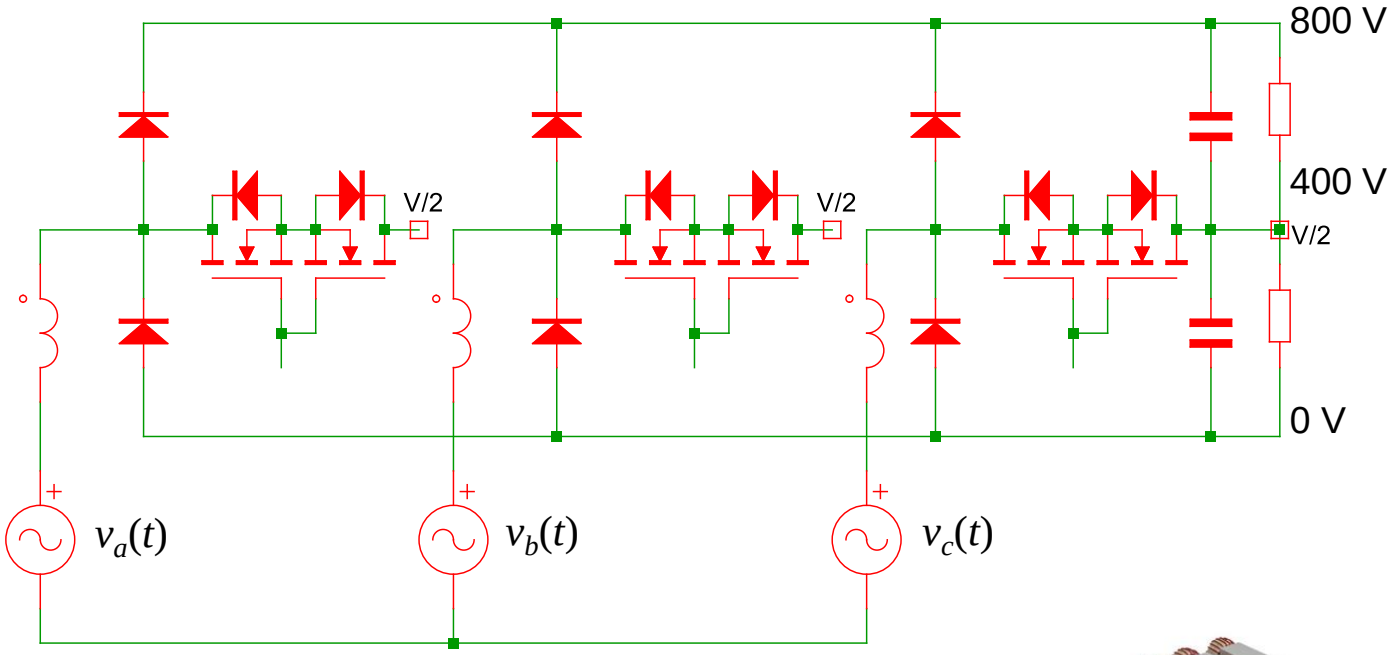
Loop Gain	Gain Crossover Frequency	4.1443925Hz
Loop Gain	Gain Margin	***ERROR***
Loop Phase	Phase Margin	69.969047degrees

Power Factor Correction – Three Phases

- There are three active branches, with or without synchronous rectification
- Different control techniques exist to maximize efficiency and minimize distortion



2-level 6-pack or
B6 type of PFC



3-level Vienna rectifier – T-type

30 kW

[Vienna 3-Phase PFC Reference Design](), Microchip

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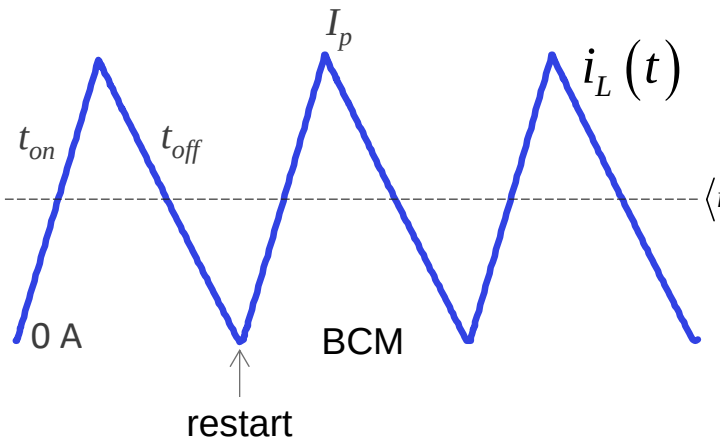
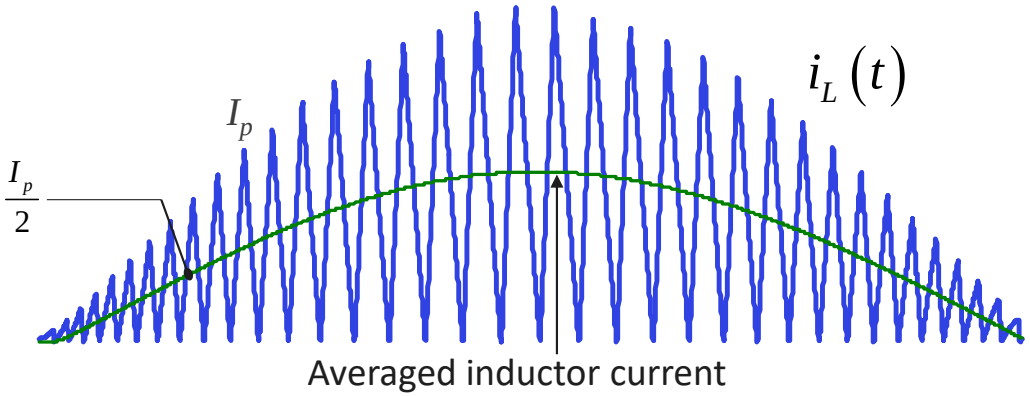
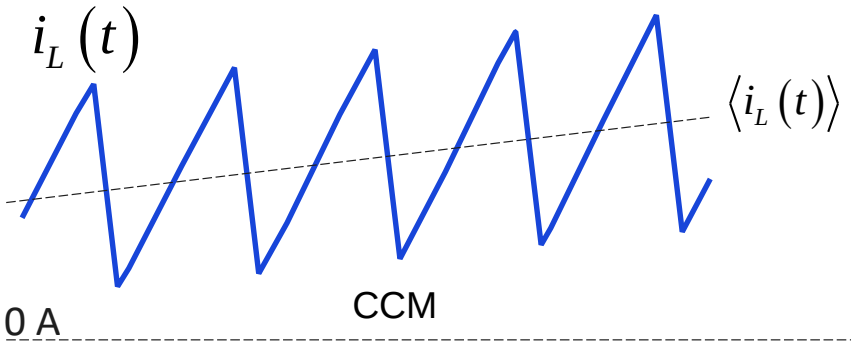
Borderline or Continuous Operation?

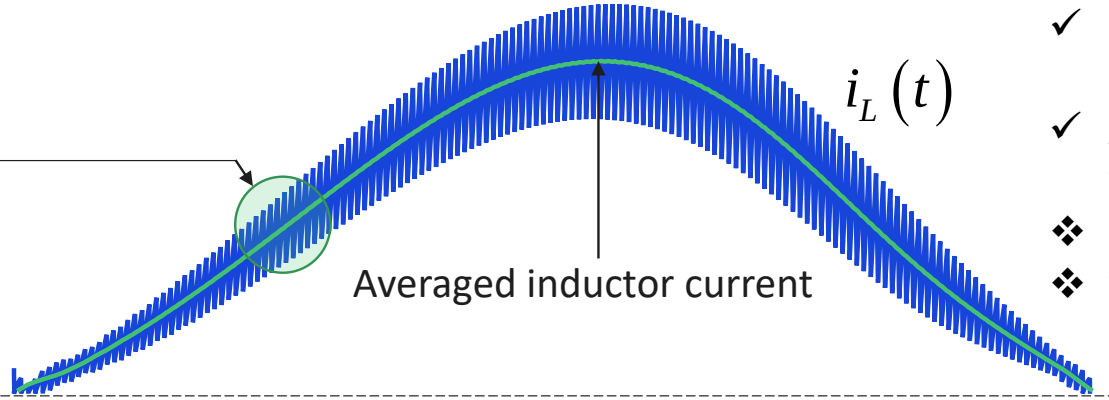
- A PFC can operate in discontinuous, borderline or continuous conduction modes
- Borderline or critical mode suits low to moderate output power levels, below 300 W
- Continuous conduction mode is adopted for high-power converters, above 500 W





- ✓ Near ZVS switching
- ✓ No t_{rr} loss on the diode
- ❖ Variable frequency
- ❖ Large rms currents



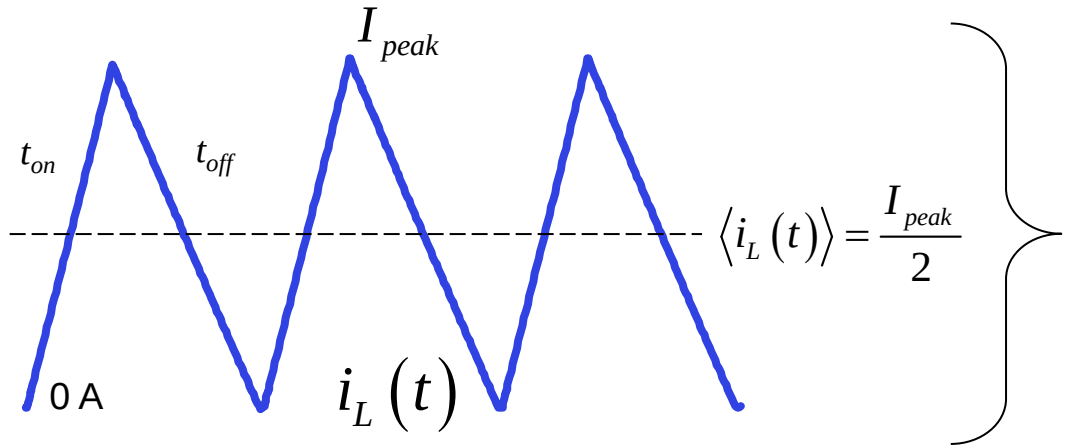


- ✓ Low ripple reduces core losses and rms currents
- ✓ Average current mode for best distortion figure
- ❖ Large inductance value
- ❖ t_{rr}-related losses due to diode – SiC is popular

Constant On-Time Control

- Voltage-mode control offers the easiest implementation for BCM PFCs

✓ Start with the inductor instantaneous current waveform:



$$p_{in}(t) = v_{in}(t)\, i_{in}(t) = v_{in}(t)\frac{i_{L,peak}(t)}{2}$$

$$i_{L,peak}(t) = \frac{v_{in}(t)}{L} t_{on}(t) \Rightarrow p_{in}(t) = \frac{v_{in}^{\,2}(t)}{2L} t_{on}(t)$$

$$\langle i_{in}(t)\rangle = \frac{v_{in}(t)}{2L} t_{on}(t) \Leftrightarrow \langle i_{in}(t)\rangle = \frac{v_{in}(t)}{R_{in}} = \frac{v_{in}(t)}{\frac{V_{ac}^{\,2}}{P_{in}}}$$

Resistive input

- The power sets the on-time value in relationship with the rms input voltage

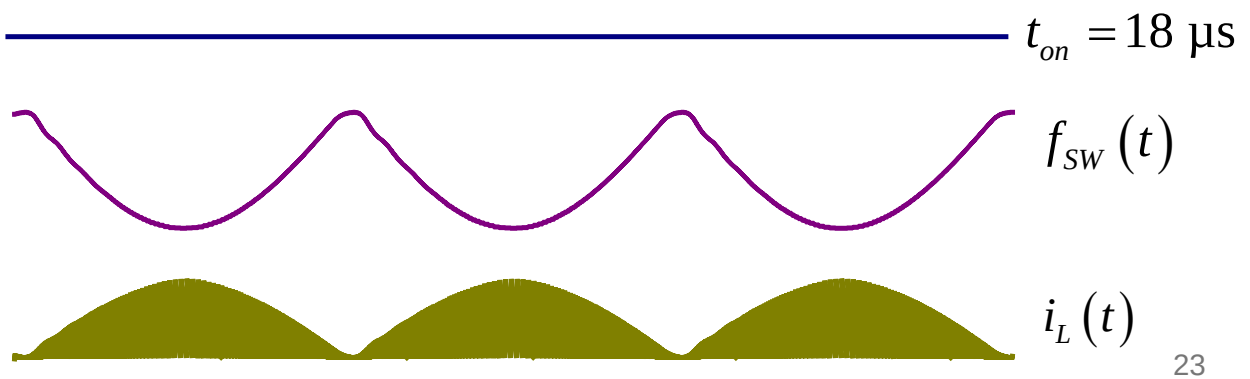
$$t_{on} = \frac{2LP_{in}}{V_{ac}^{\,2}}$$

$$\Rightarrow i_{in}(t) = \frac{V_{ac}\sqrt{2}t_{on}}{2L}\sin(\omega t)$$

constant

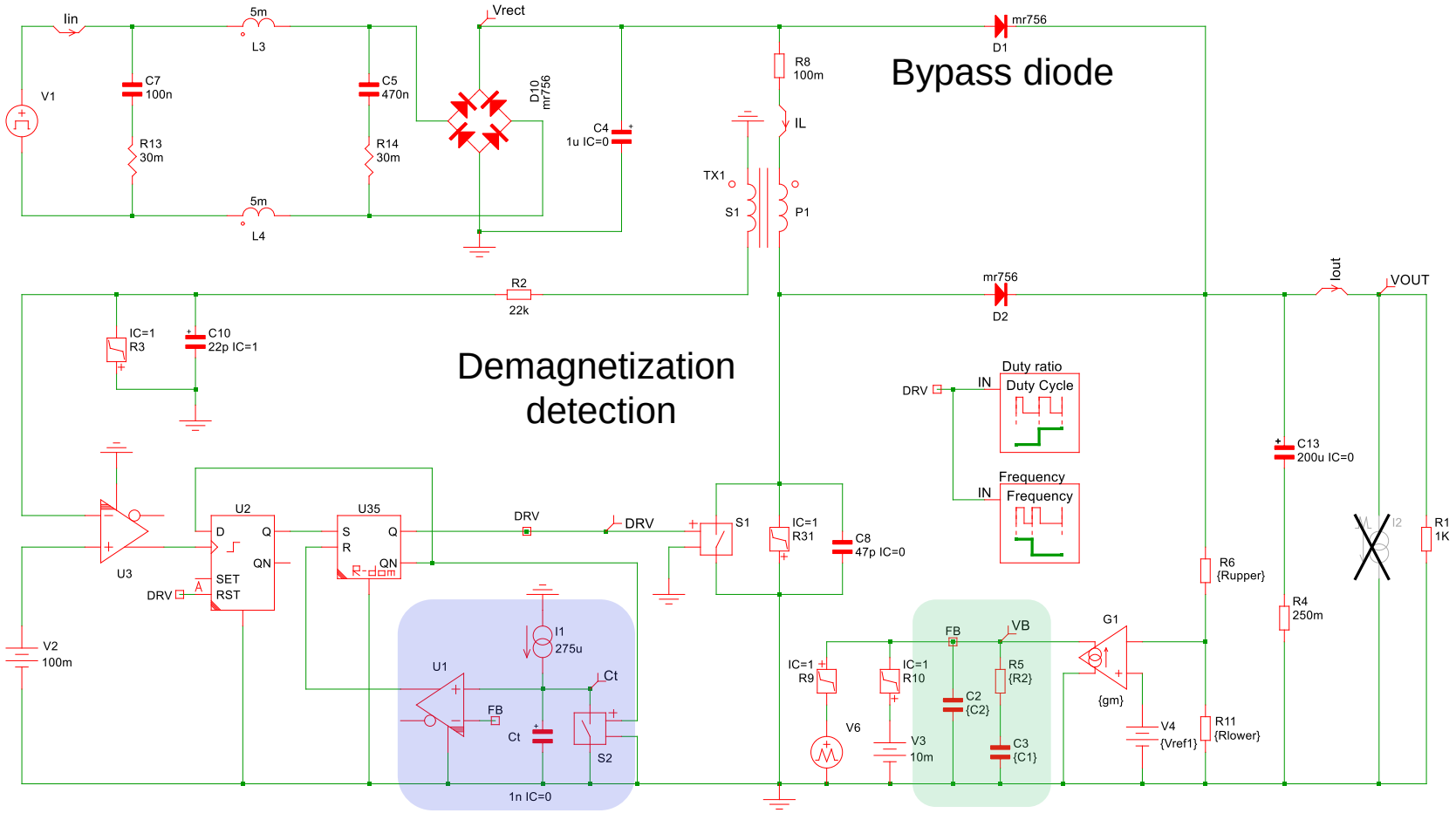
✓ On-time is constant

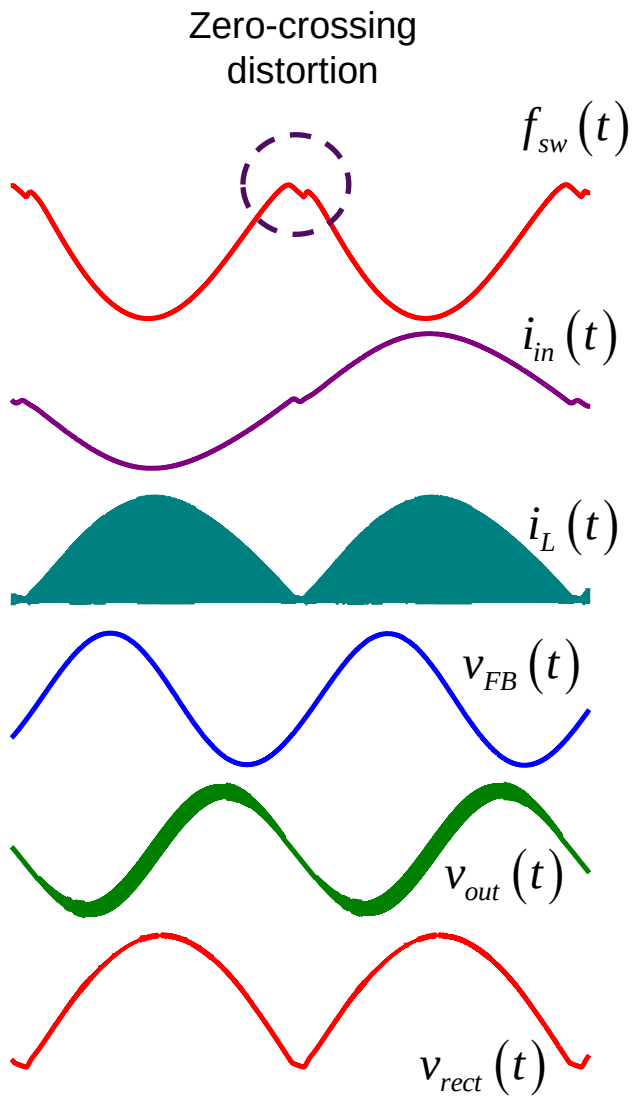
✓ Frequency is variable



Voltage-Mode Operation

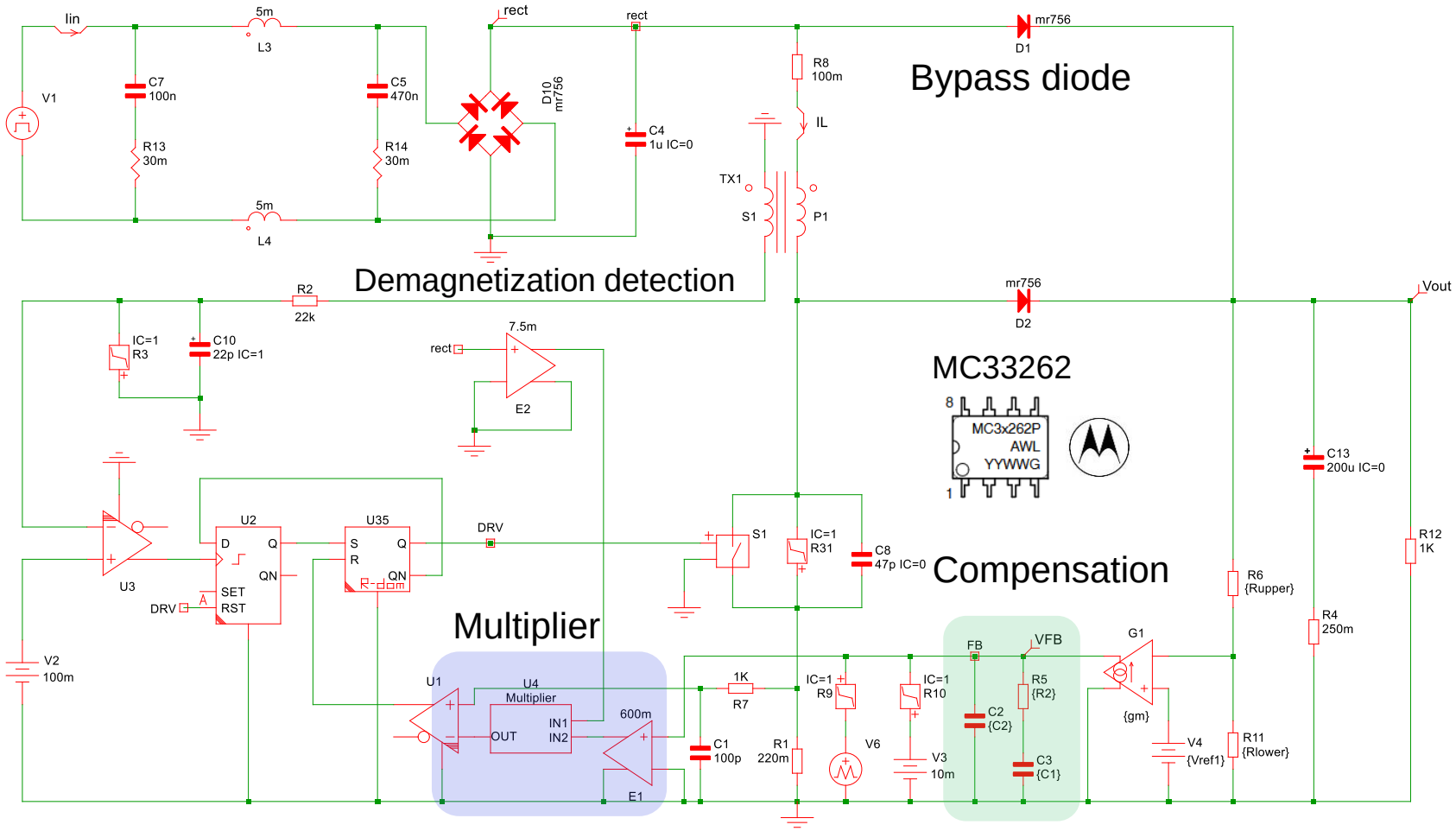
- Constant on-time can be implemented in voltage-mode control
- ✓ No need to sense the input voltage!

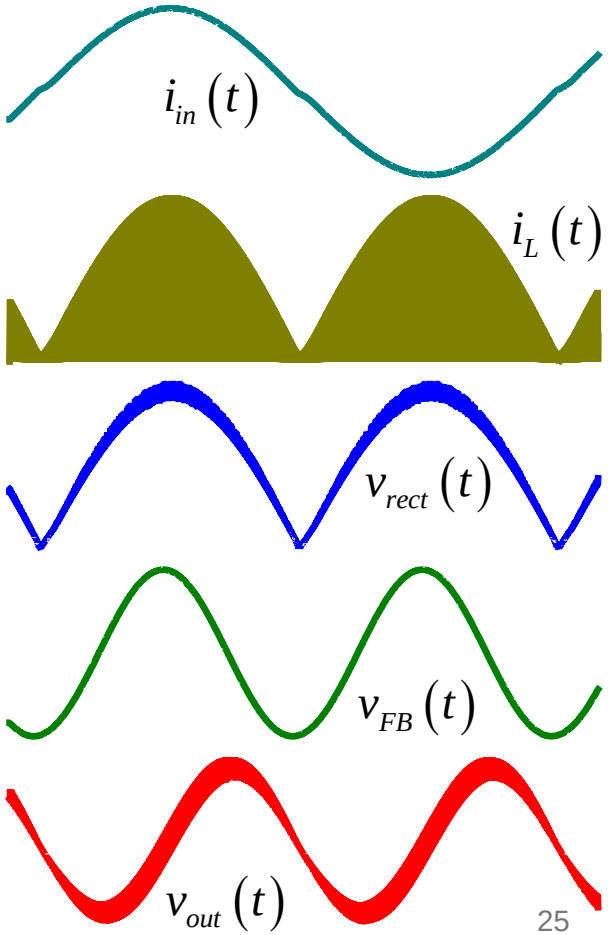




Peak-Current-Mode Operation

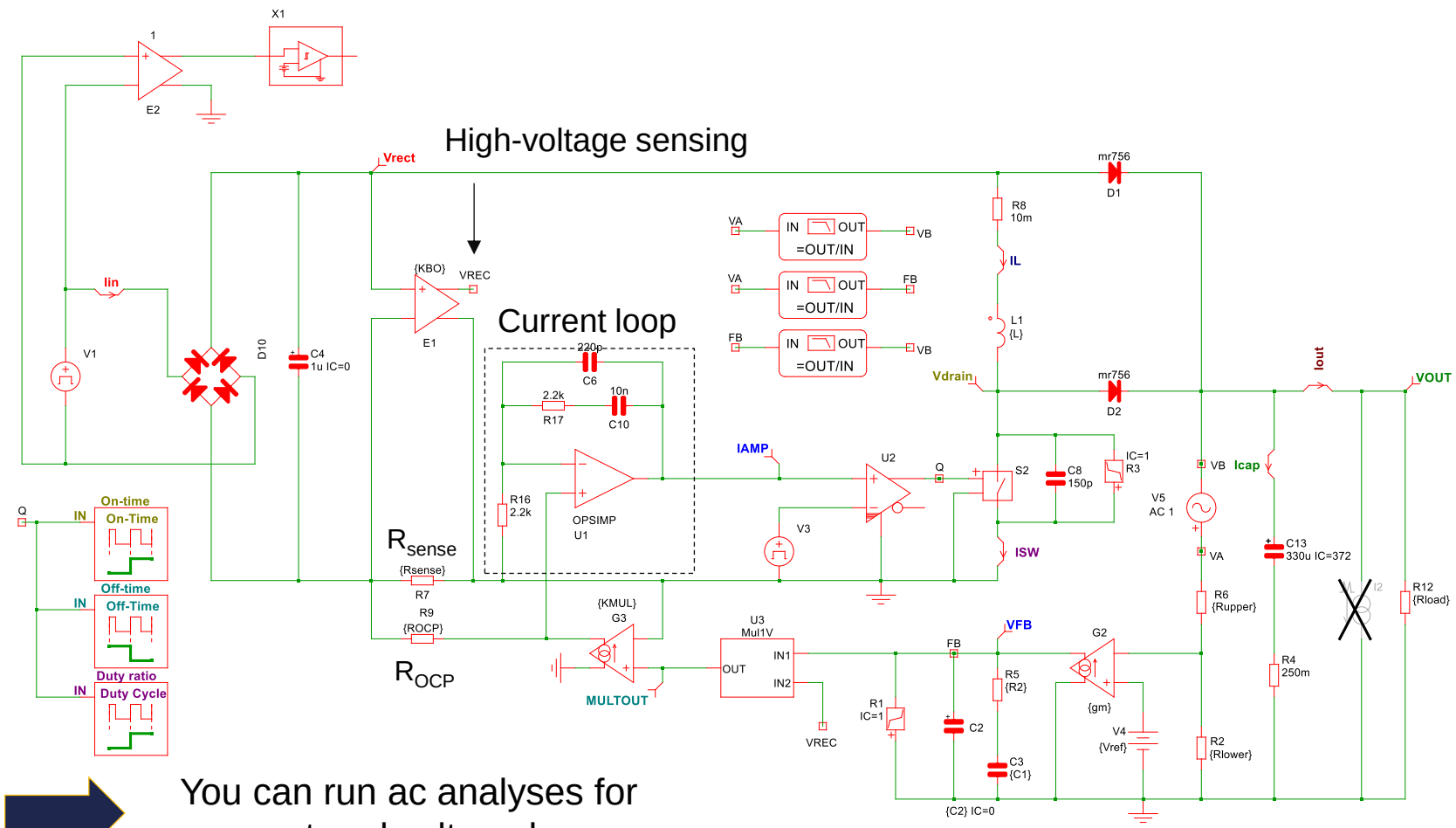
- The inductor *peak current* follows the rectified voltage for a sinusoidal envelope
  - A multiplier is needed to sense the input voltage: increased power consumption

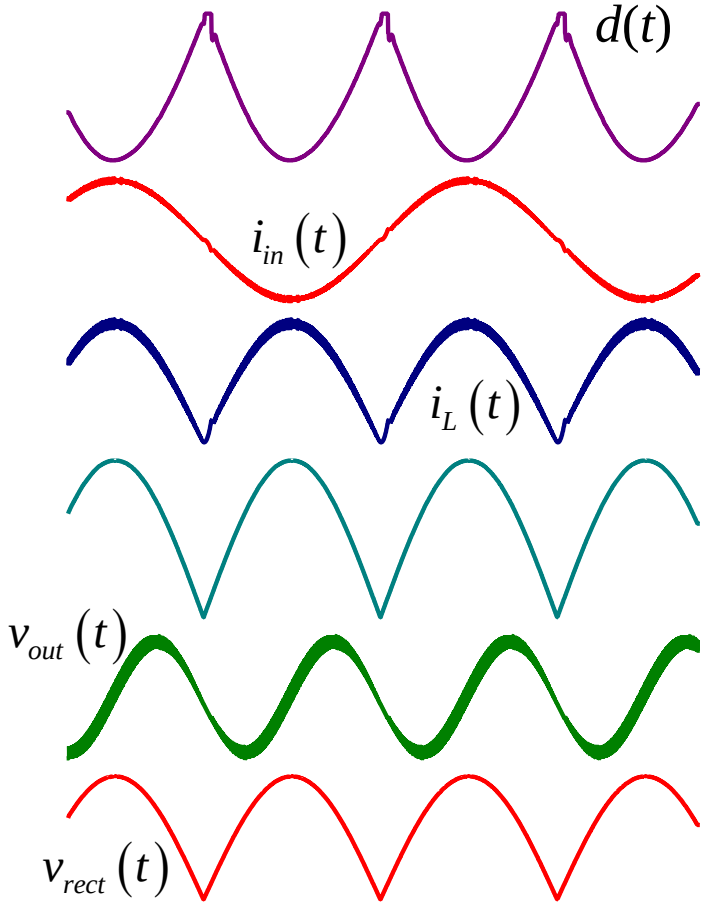




Average Current Mode Control – CCM

- A high-bandwidth loop monitors the inductor current to force sinusoidal waveshape
- A multiplier scales the current envelope to meet output power requirements





You can run ac analyses for current and voltage loops

Predictive Control Law – No Line Sensing

- It is possible to control the duty ratio without sensing the input voltage
- This elegant approach simplifies the implementation of the PFC engine

In a PFC

$$\langle i_L(t)\rangle = i_{in}(t) \propto v_{in}(t)$$

Dc transfer characteristic:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} = \frac{1}{D_{off}} \rightarrow R_{in} = \frac{V_{in}}{I_{in}} = \frac{D_{off} V_{out}}{\langle i_L(t)\rangle}$$

If D_{off} is shaped as:

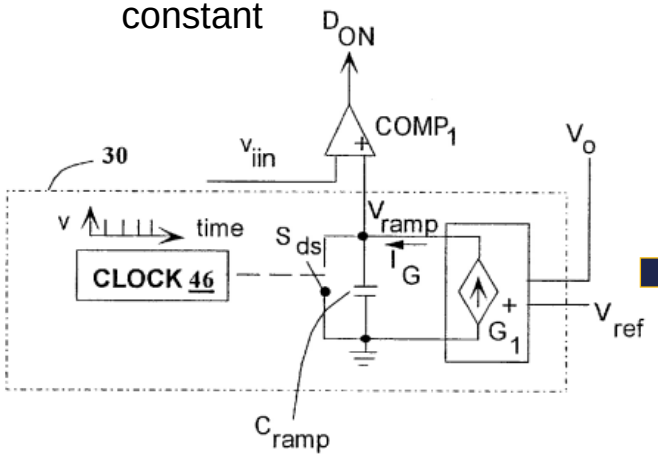
$$D_{off} = \frac{R_{in}}{V_{out}} \langle i_L(t)\rangle$$

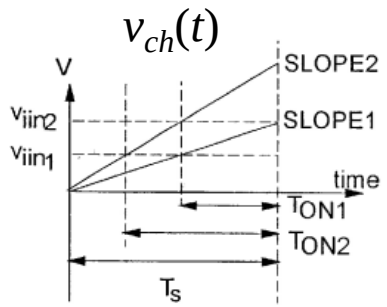
It ensures a sinusoidal absorption

That is, a resistive input will be observed if D_{off} is programmed according to the rule:

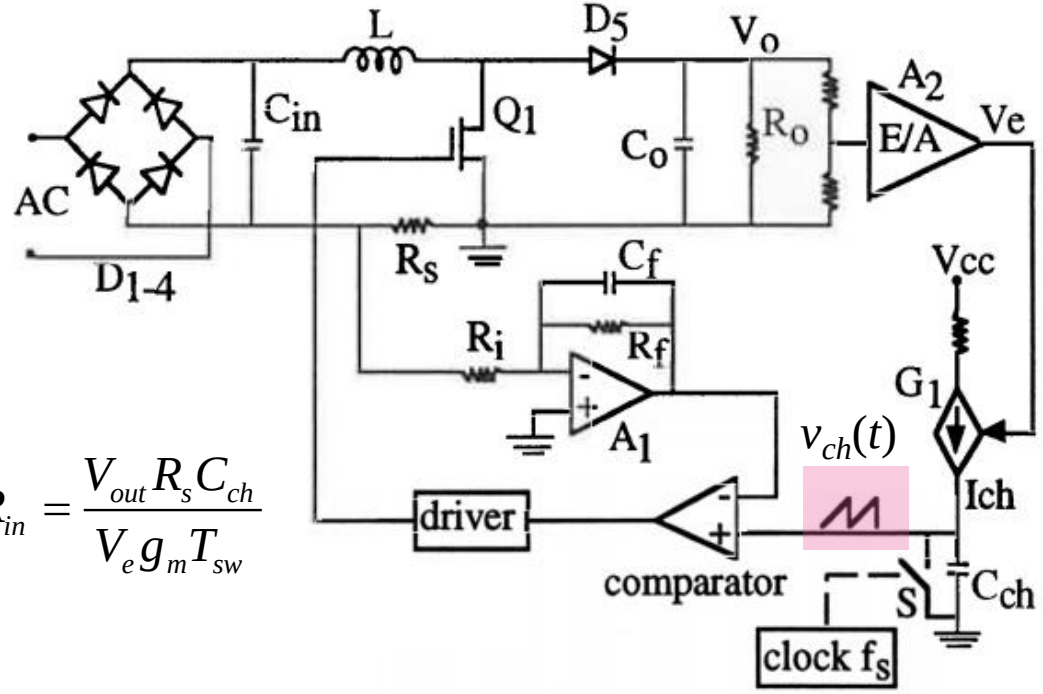
$$D_{off} = \left(\frac{R_e}{V_o(av)}\right) I_L(av) \quad , \quad 0 < D_{off} < 1 \qquad (4)$$

constant





$$R_{in} = \frac{V_{out} R_s C_{ch}}{V_e g_m T_{sw}}$$



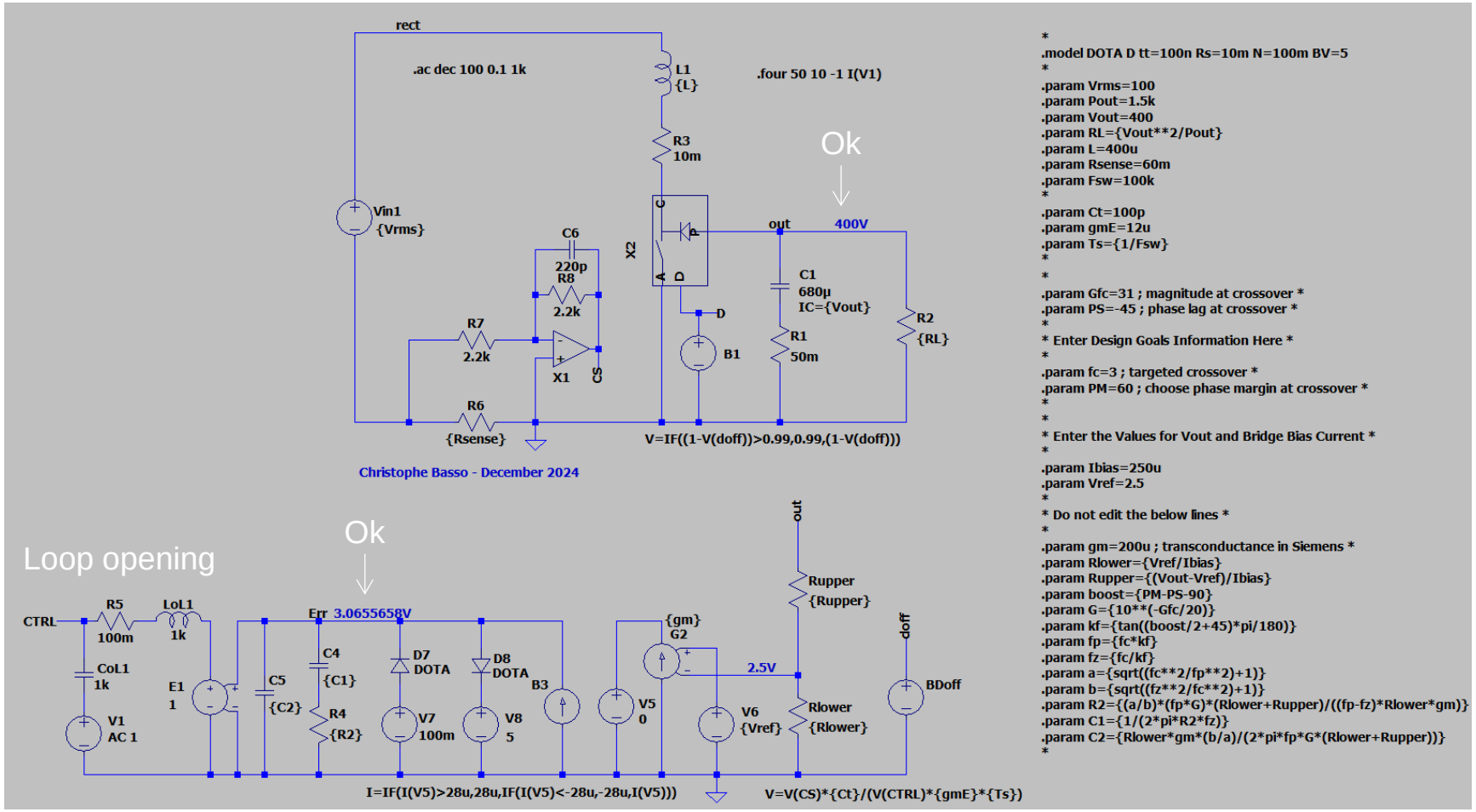
6,307,361 (Oct 2001) and 6,728,121 (April2004)

S. Ben-Yaakov, I. Zehser, *PWM Converters with resistive input*, *IEEE Transactions on Industrial Electronics*, vol. 45, June 1998

An Averaged Model to Stabilize the Loop

- An average model can be built and offers many advantages for the PFC study

✓ It simulates fast (no switching component) and it works for ac analyses

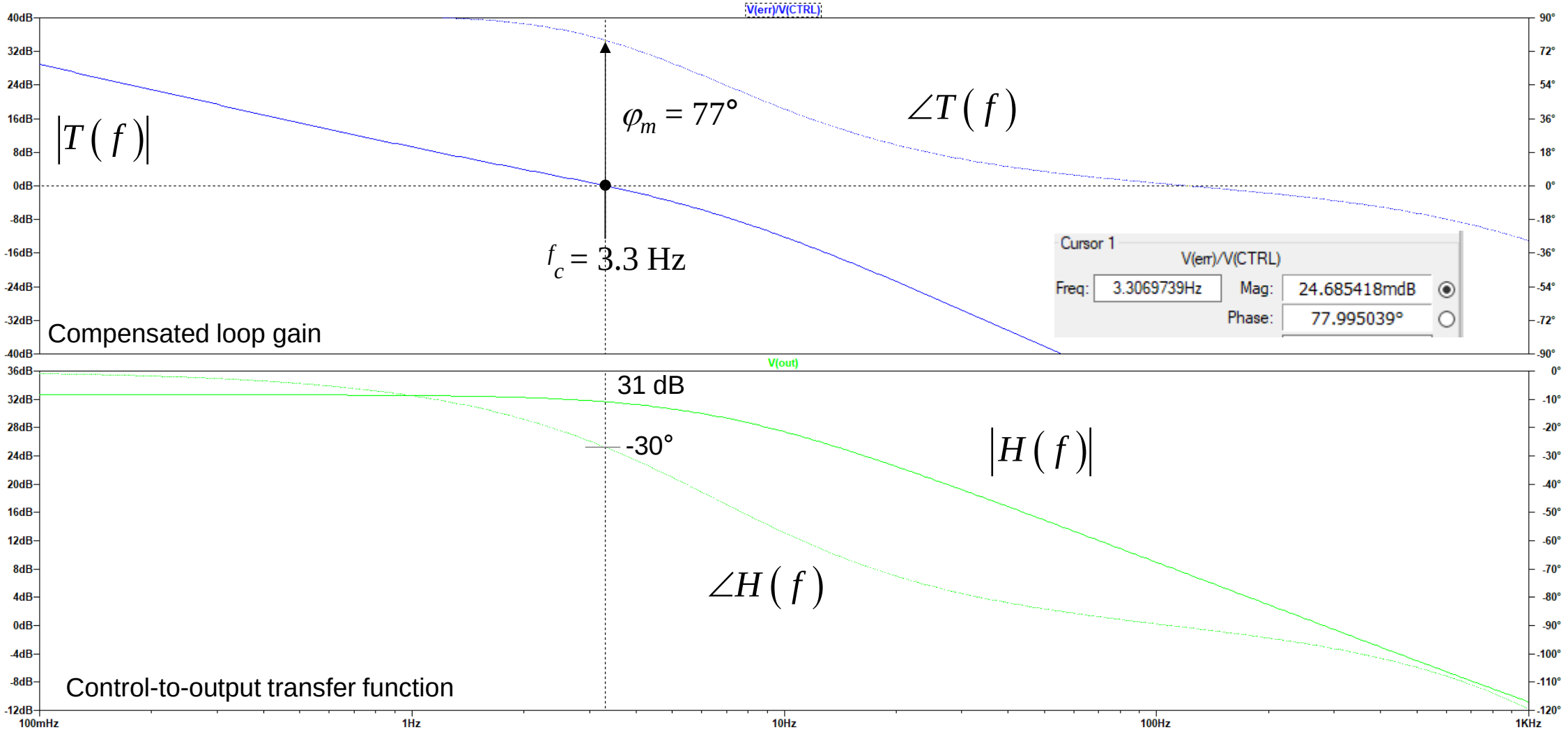



```
*
.model DOTA D tt=100n Rs=10m N=100m BV=5
*
.param Vrms=100
.param Pout=1.5k
.param Vout=400
.param RL={Vout**2/Pout}
.param L=400u
.param Rsense=60m
.param Fsw=100k
*
.param Ct=100p
.param gmE=12u
.param Ts={1/Fsw}
*
*
.param Gfc=31 ; magnitude at crossover *
.param PS=-45 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fc=3 ; targeted crossover *
.param PM=60 ; choose phase margin at crossover *
*
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Ibias=250u
.param Vref=2.5
*
* Do not edit the below lines *
*
.param gm=200u ; transconductance in Siemens *
.param Rlower={Vref/Ibias}
.param Rupper={(Vout-Vref)/Ibias}
.param boost={PM-PS-90}
.param G={10**(-Gfc/20)}
.param kf={tan((boost/2+45)*pi/180)}
.param fp={fc*kf}
.param fz={fc/kf}
.param a={sqrt((fc**2/fp**2)+1)}
.param b={sqrt((fz**2/fc**2)+1)}
.param R2={(a/b)*(fp*G)*(Rlower+Rupper)/((fp-fz)*Rlower*gm)}
.param C1={1/(2*pi*R2*fz)}
.param C2={Rlower*gm*(b/a)/(2*pi*fp*G*(Rlower+Rupper))}
*
```

- The right-side macro automates the compensation components values for the type 2 OTA
- Always check the operating points are correct before considering the ac plots
- This is the voltage-loop ac analysis, but the current loop can also be swept

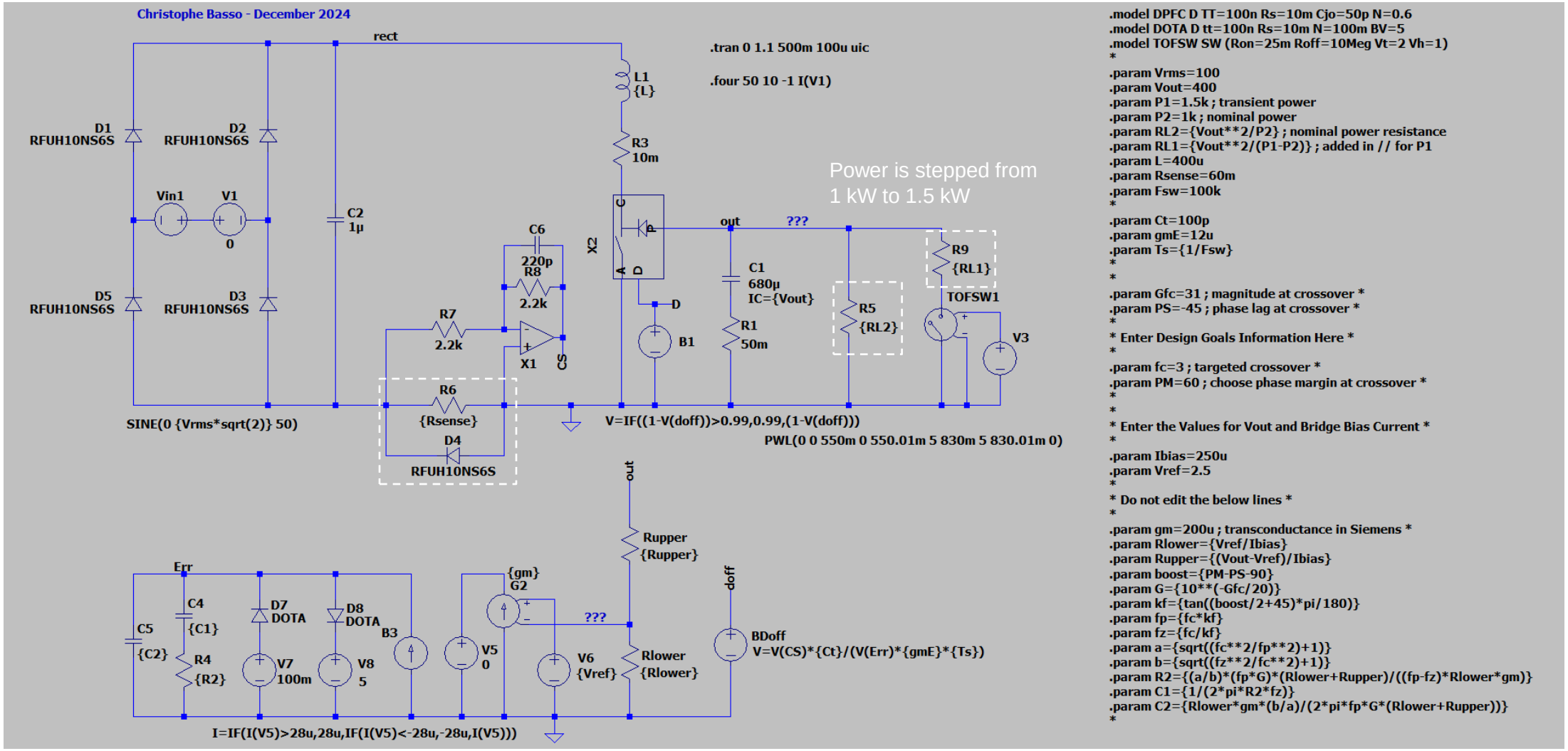
Check Crossover and Margins are Ok

- SPICE linearizes the large-signal PWM switch model and delivers ac results in a second



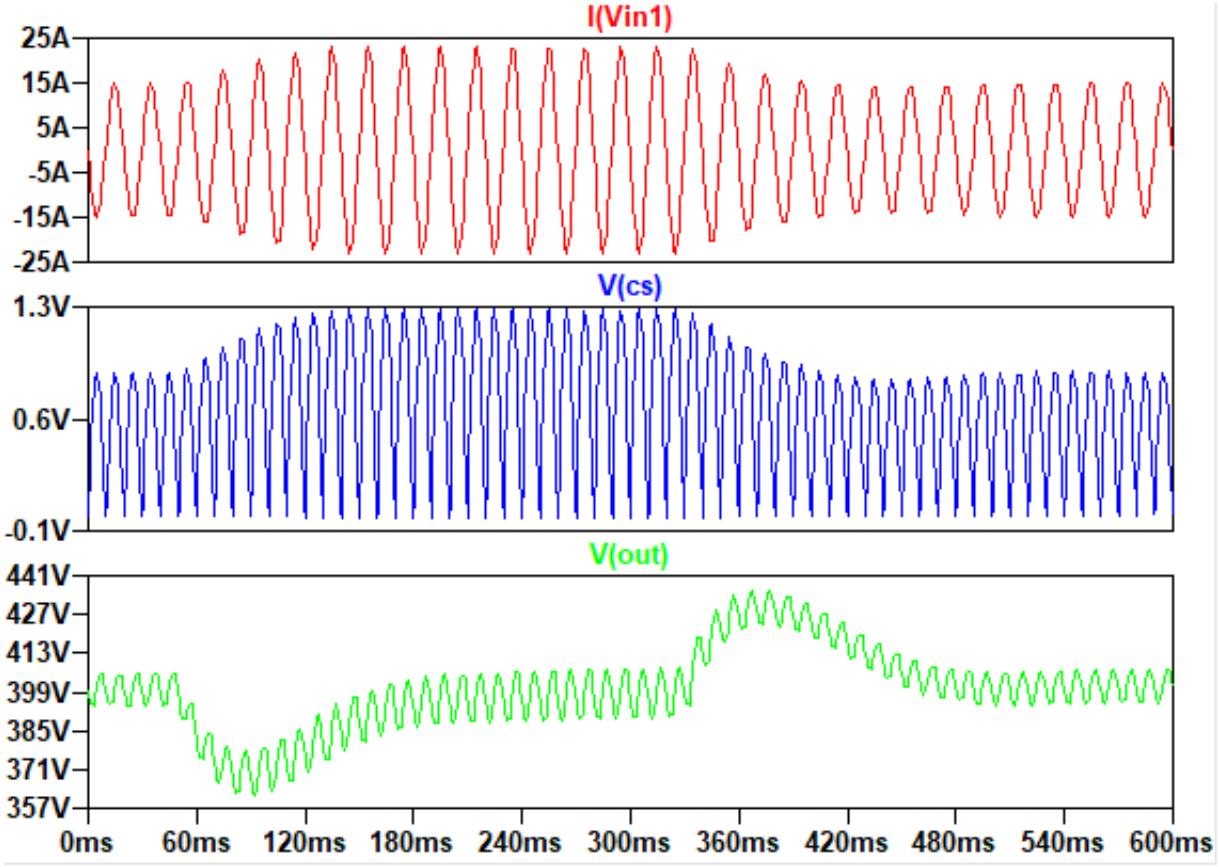
Averaged Model and Transient Analyses

- Transient analyses are extremely fast and let you test the compensation strategy

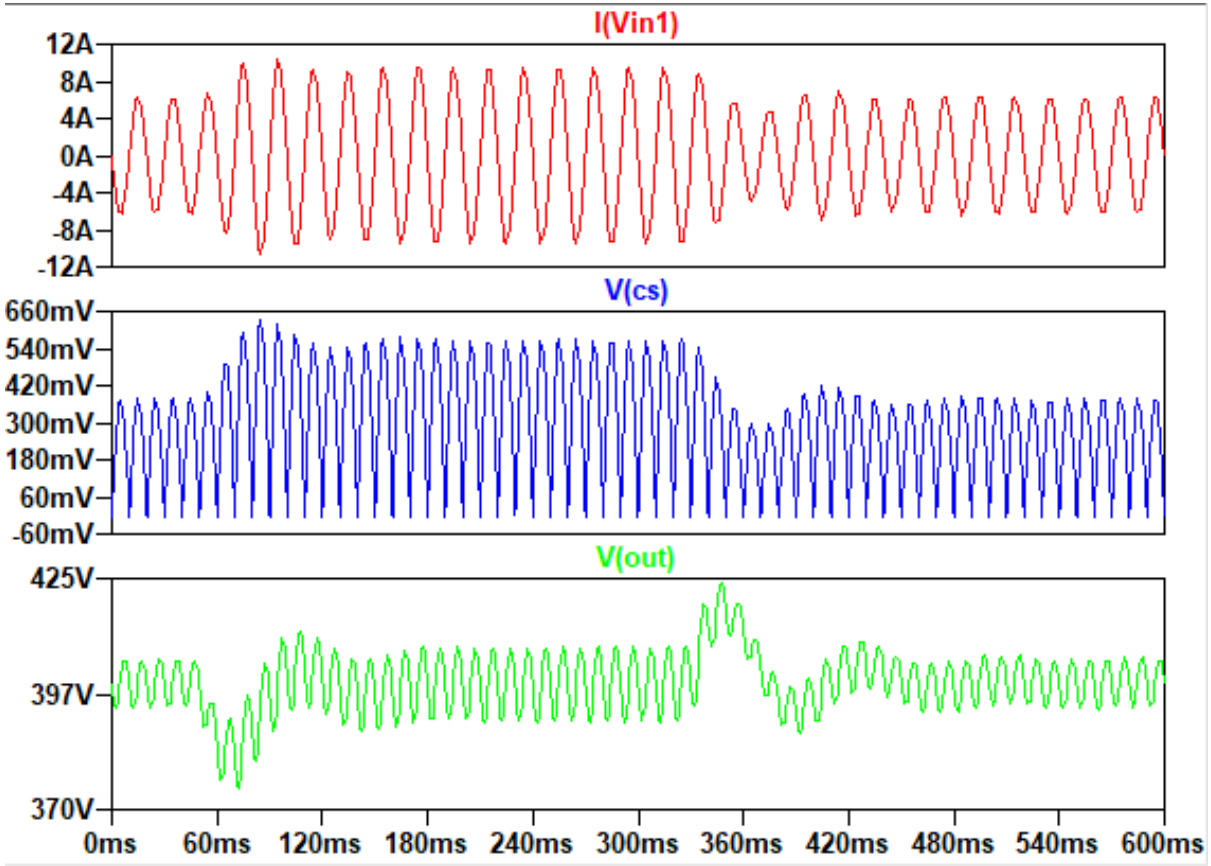


Testing the Step Load Response

- The output voltage is stable at low line but shows a bit of ringing at high line
- ➢ The transient response is better in high line as the crossover frequency increases



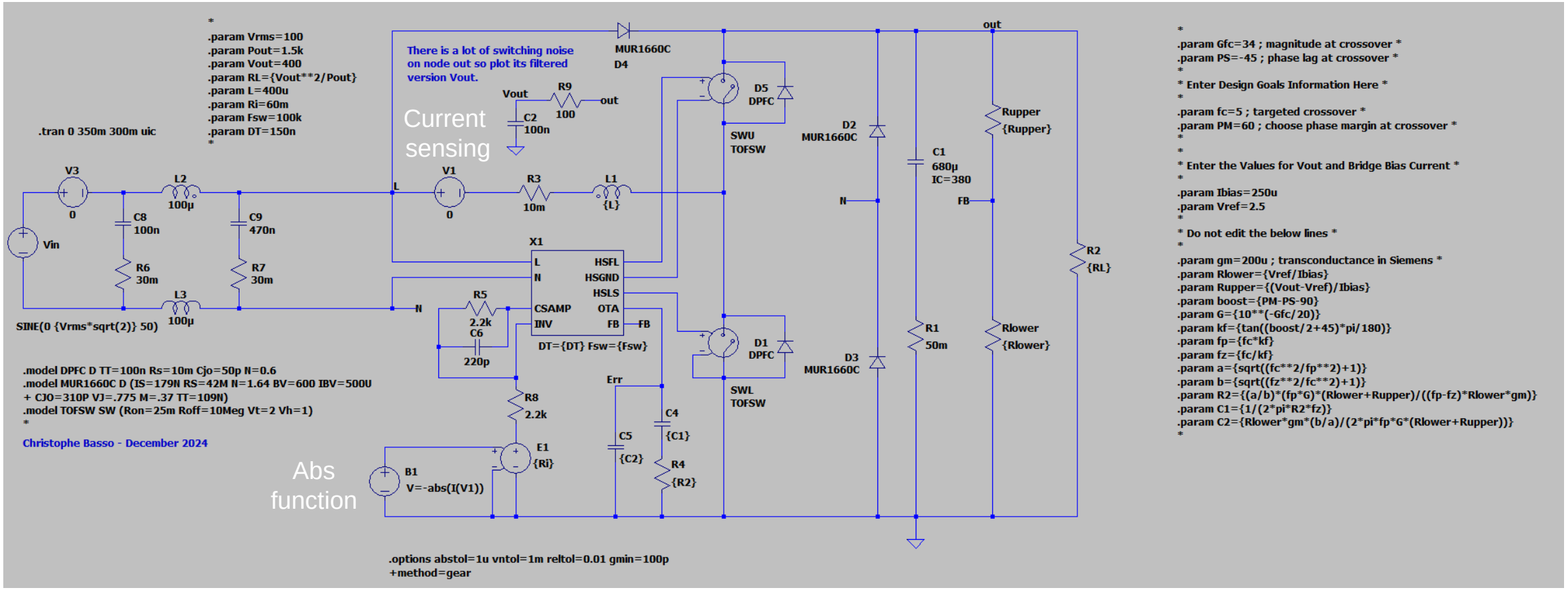
P_{out} stepped from 1 kW to 1.5 kW, V_{in} = 100 V rms



P_{out} stepped from 1 kW to 1.5 kW, V_{in} = 230 V rms

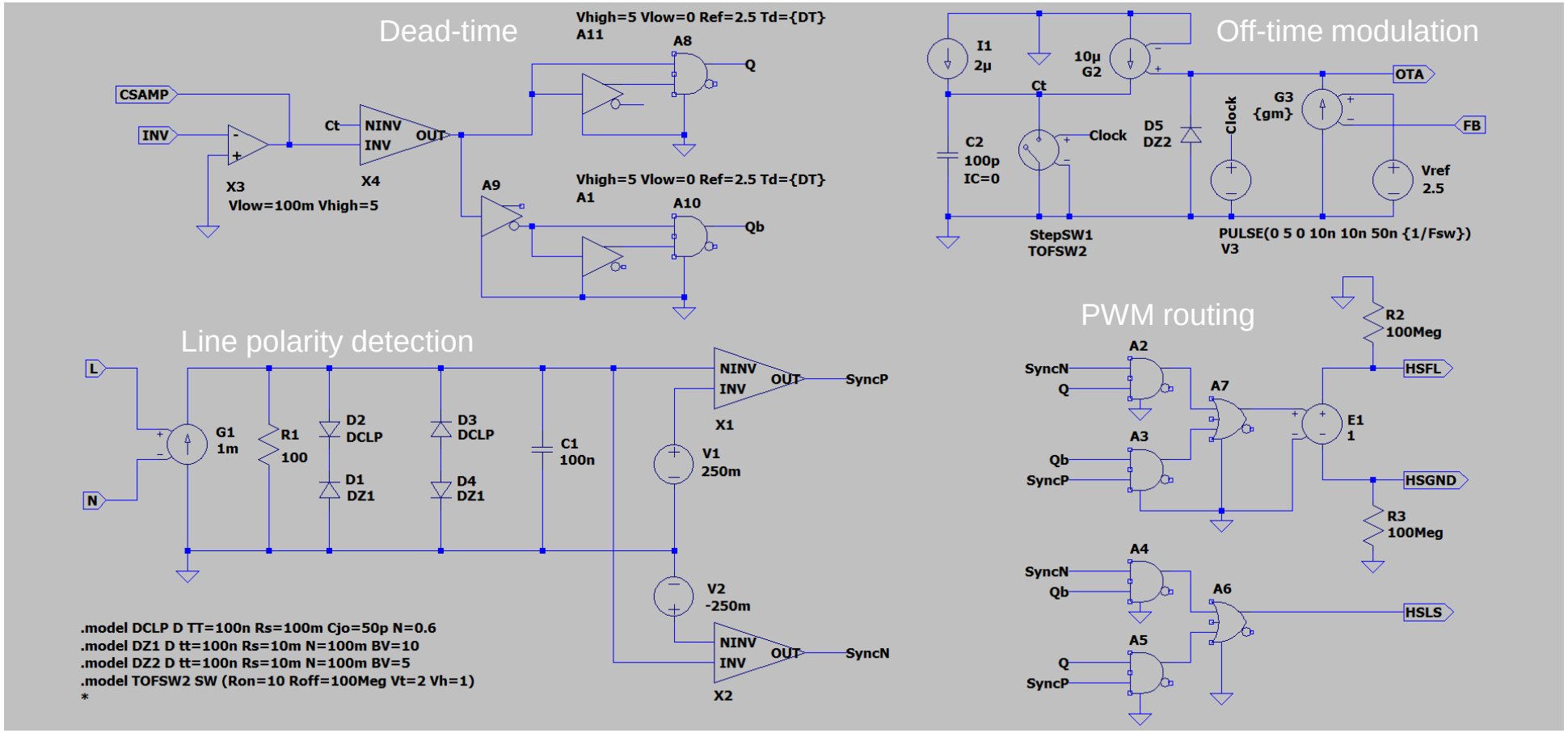
A TPPFC in a Cycle-by-Cycle Application

- The variable-t_{off} technique is well suited for a TPPFC implementation
- An internal circuitry detects the line polarity and routes timings to the switches



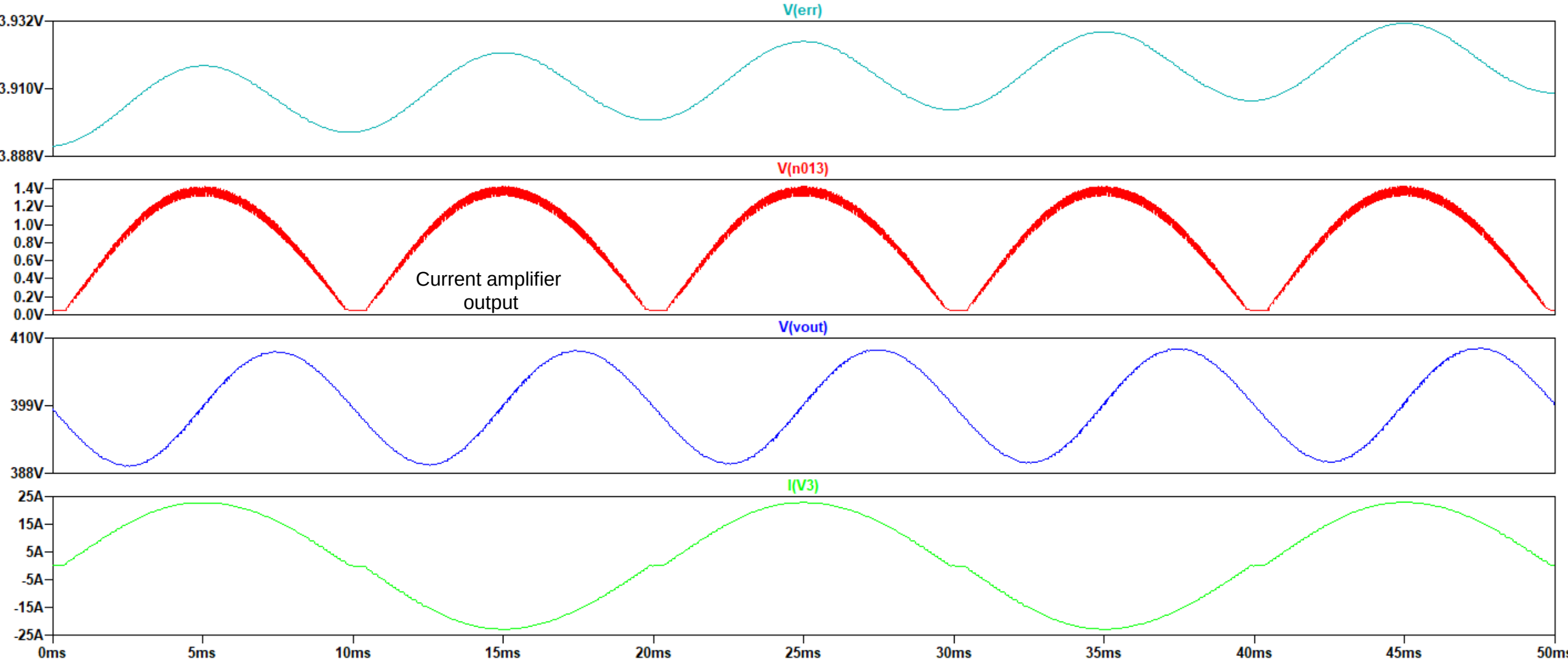
Inside the TPPFC Subcircuit

- You need to determine the input line polarity to route the PWM signals
- Dead-time is inserted to provide smooth handover between switch and sync rectifier



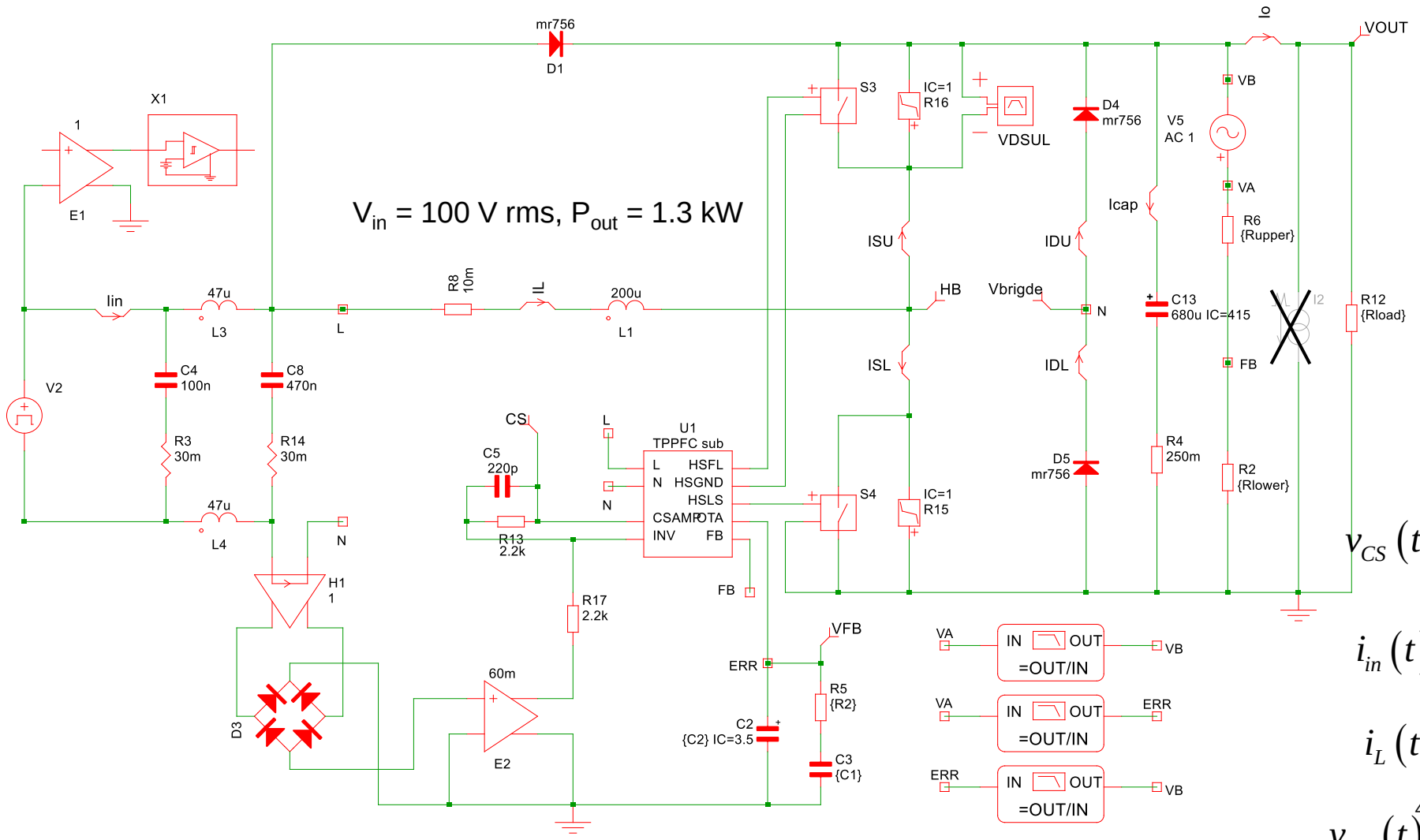
Operating Waveforms

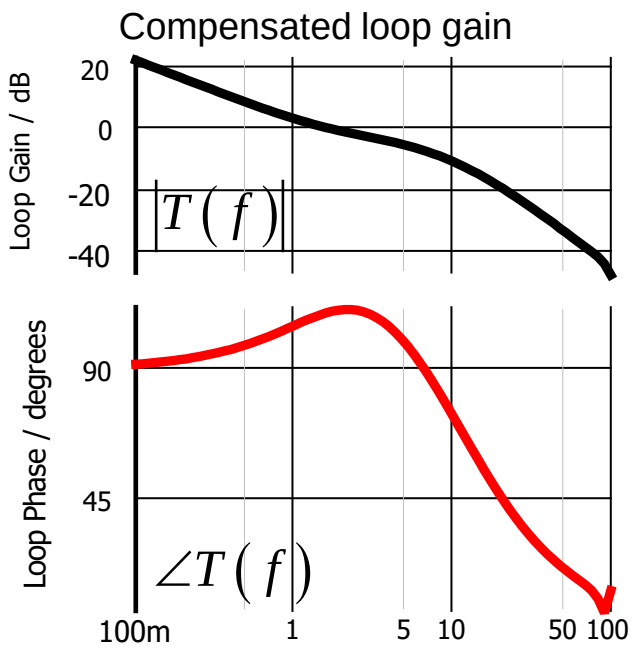
- The simulation time is 183 s on my machine which is acceptable

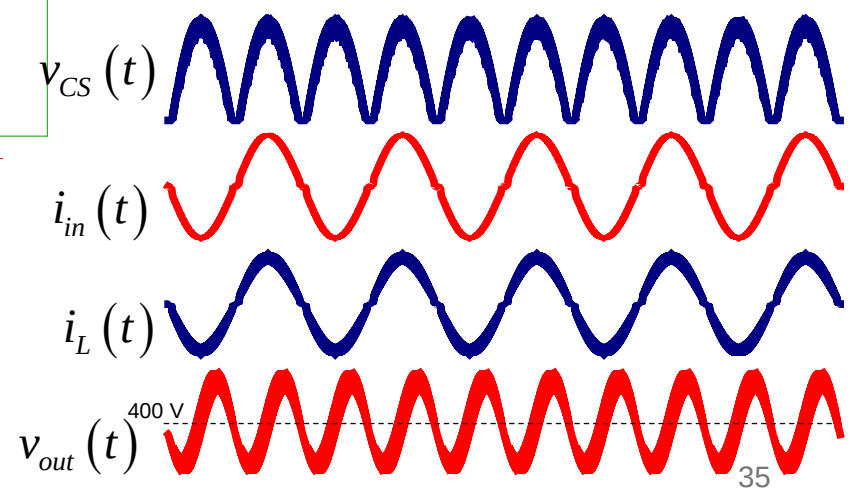


SIMPLIS for AC and TRAN Responses

- There is no need to resort to an averaged model with SIMPLIS

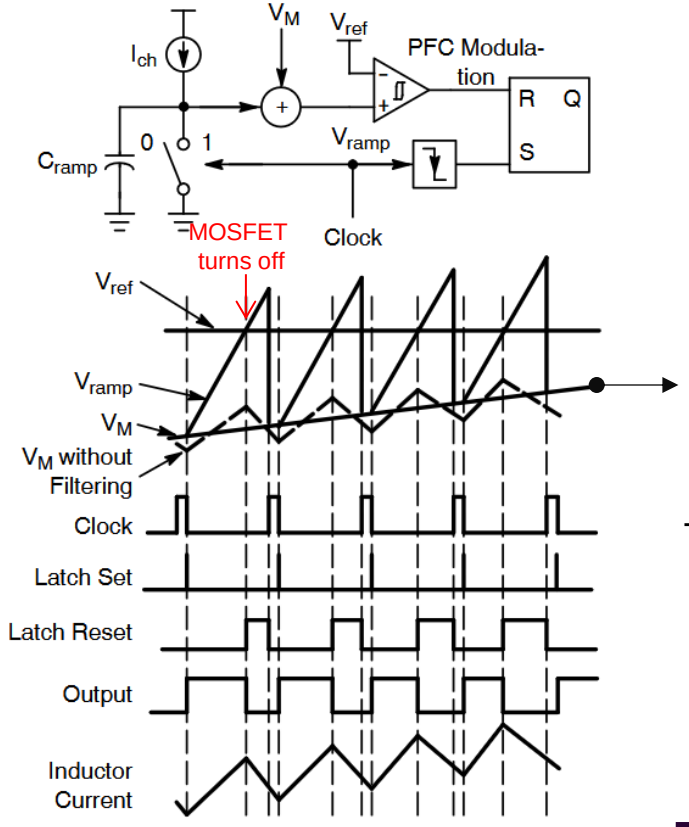






NCP1654 – a Different Approach

- The NCP1654 from *onsemi* uses a slightly different technique to produce 1-$d(t)$
- The static input voltage is used to scale the control voltage envelope

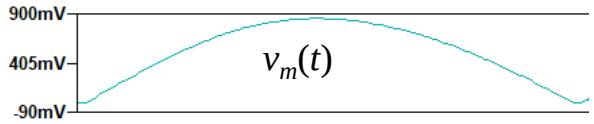


This is the internal modulator of the NCP1653/54

Boost dc transfer characteristic $\frac{V_{out}}{V_{in}} = \frac{1}{1-d}$ ➡ $V_{in} = V_{out}(1-d)$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{\langle i_L(t)\rangle} = \frac{V_{out}}{\langle i_L(t)\rangle}(1-d)$$

R_{in} has to be constant if we want to emulate a resistance



The transition occurs when $V_{ramp} = V_{ref}$ or: $V_m + \frac{I_{ch} dT_{sw}}{C_{ramp}} = V_{ref}$

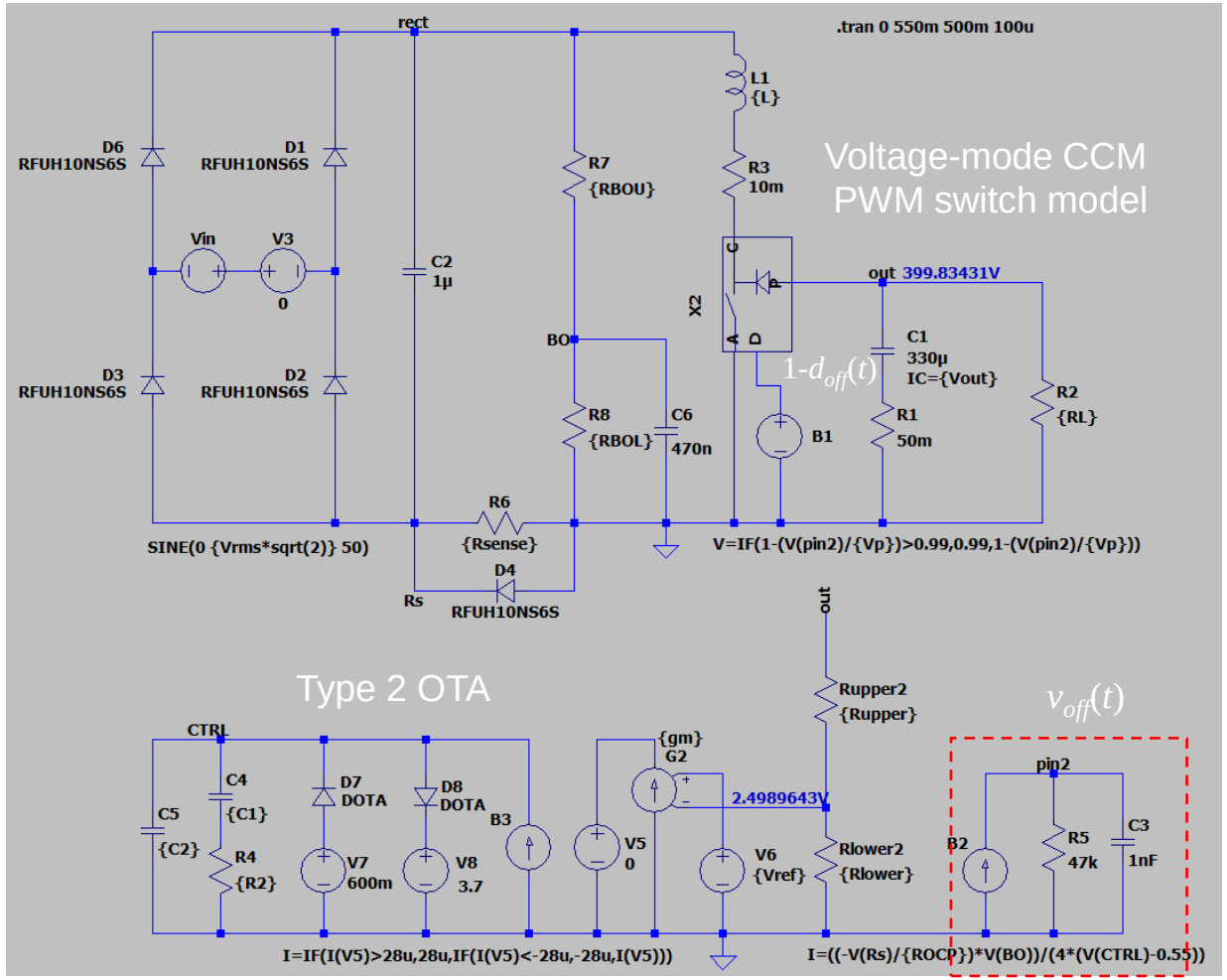
The ramp duration lasts a switching period and is easily determined as:

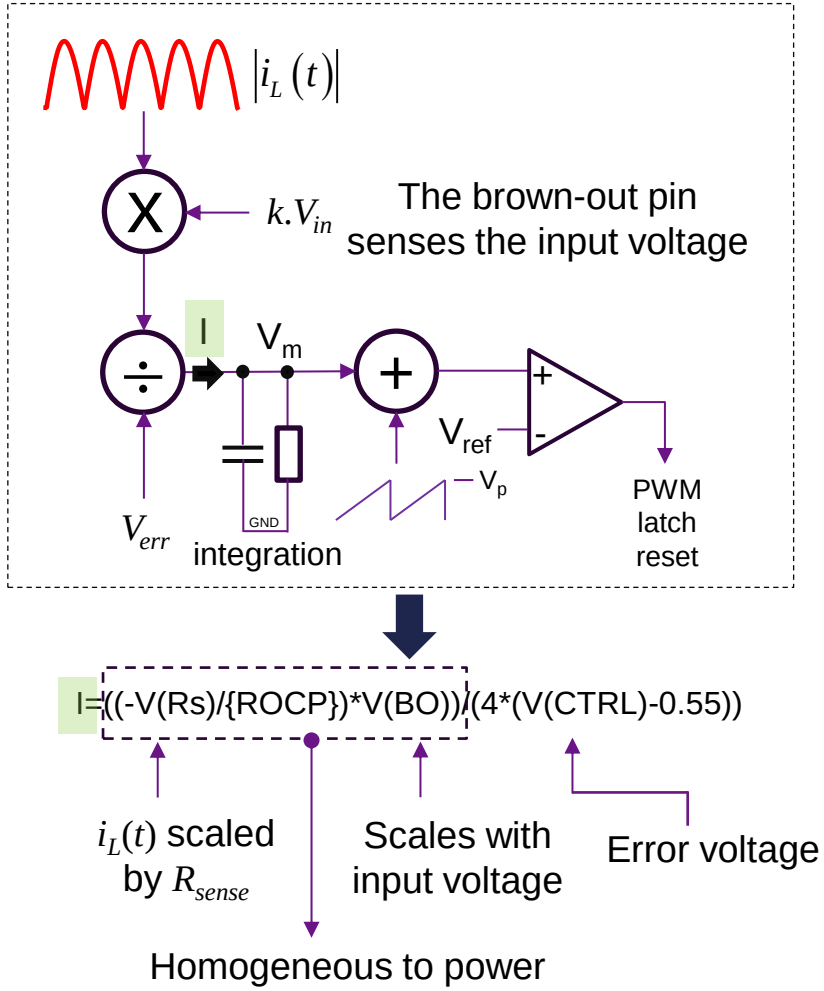
$$T_{sw} = \frac{C_{ramp} V_{ref}}{I_{ch}} \rightarrow I_{ch} = \frac{C_{ramp} V_{ref}}{T_{sw}}$$ Replace I_{ch} in the above expression

➡ $V_{ref} = V_m + \frac{\left(C_{ramp} V_{ref} / T_{sw}\right) dT_{sw}}{C_{ramp}} \rightarrow V_m = V_{ref}(1-d)$ ➡ $R_{in} = \frac{V_{out}}{\langle i_L(t)\rangle} \frac{V_m}{V_{ref}}$

Averaged Modeling of NCP1654

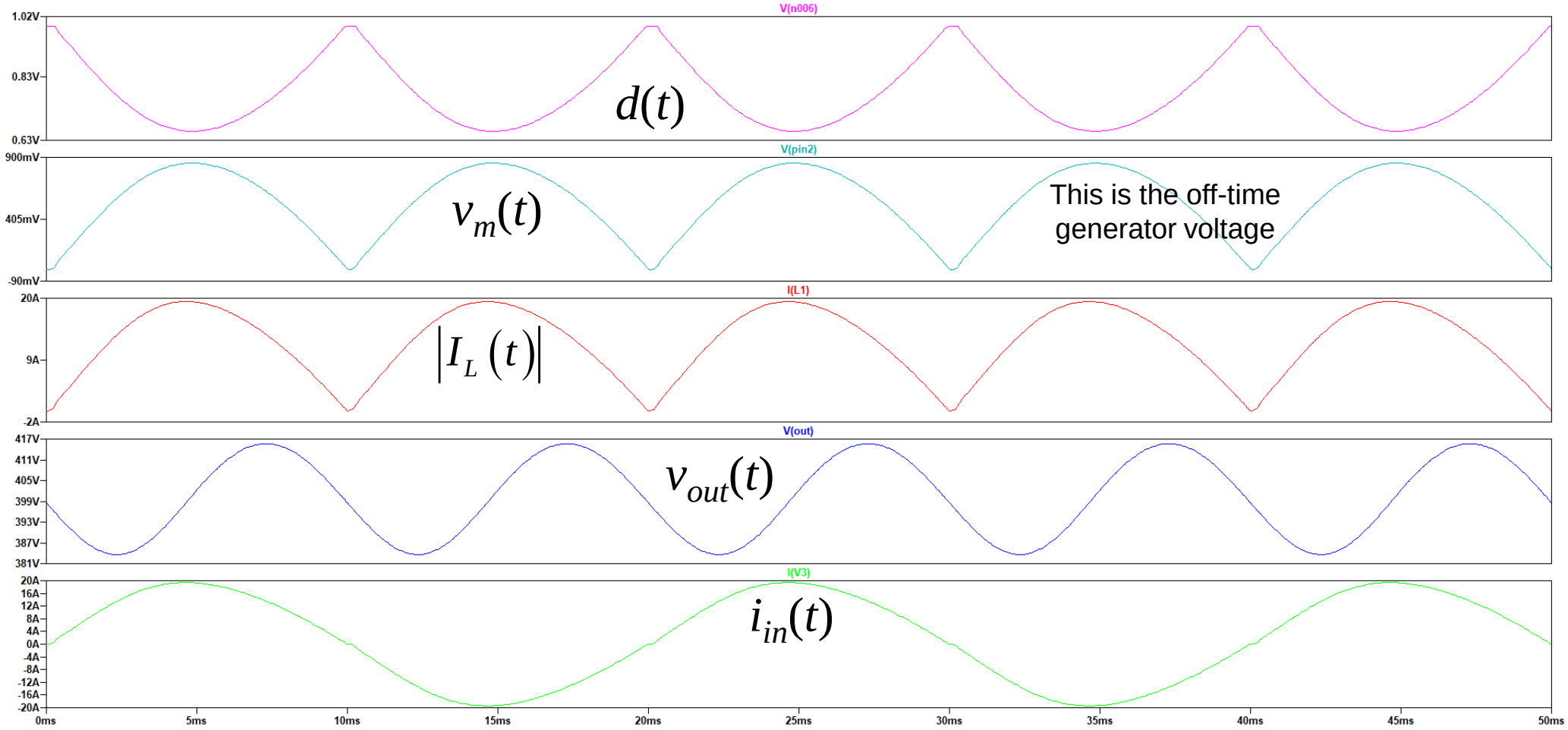
- The averaged large-signal model will simulate fast in lack of switching component
- SPICE linearizes equations and we can obtain the control-to-output transfer function





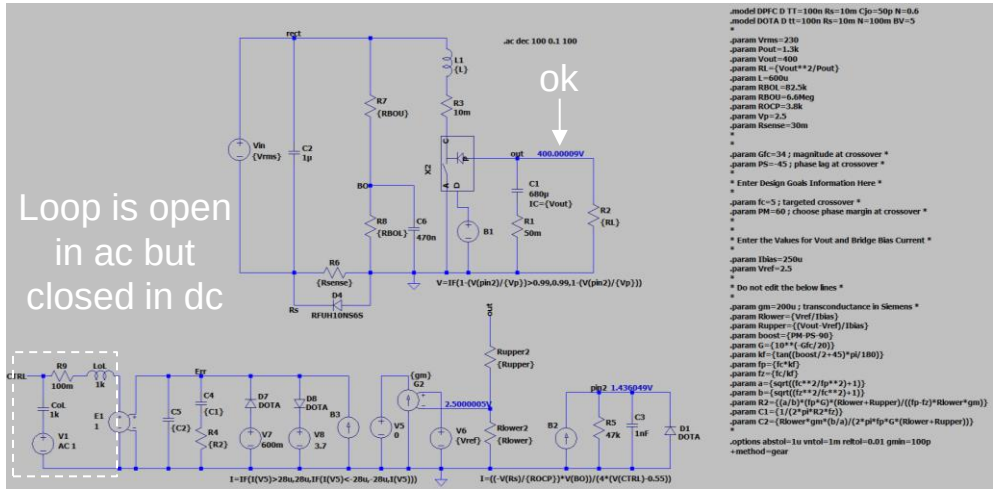
Simulation Results for the Averaged Model

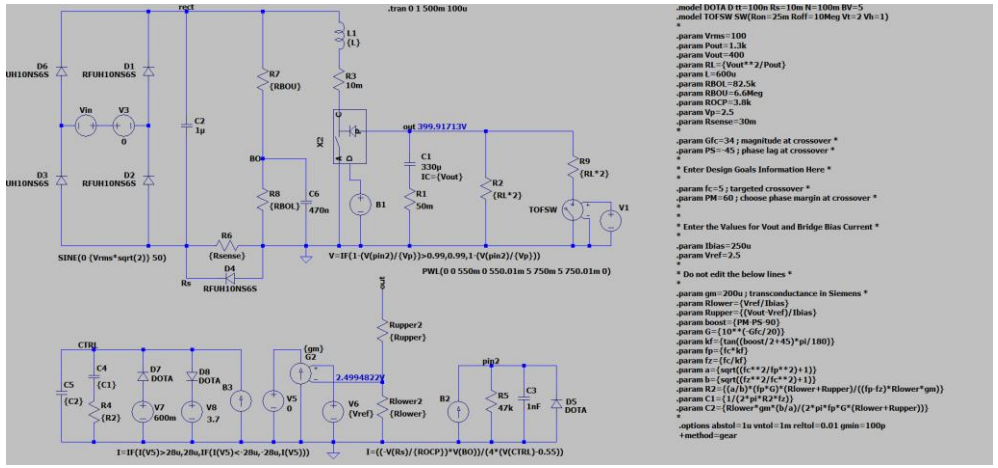
- The simulation time is extremely fast and helps test the overall architecture
- The low-frequency rms current in the capacitor can be quickly assessed

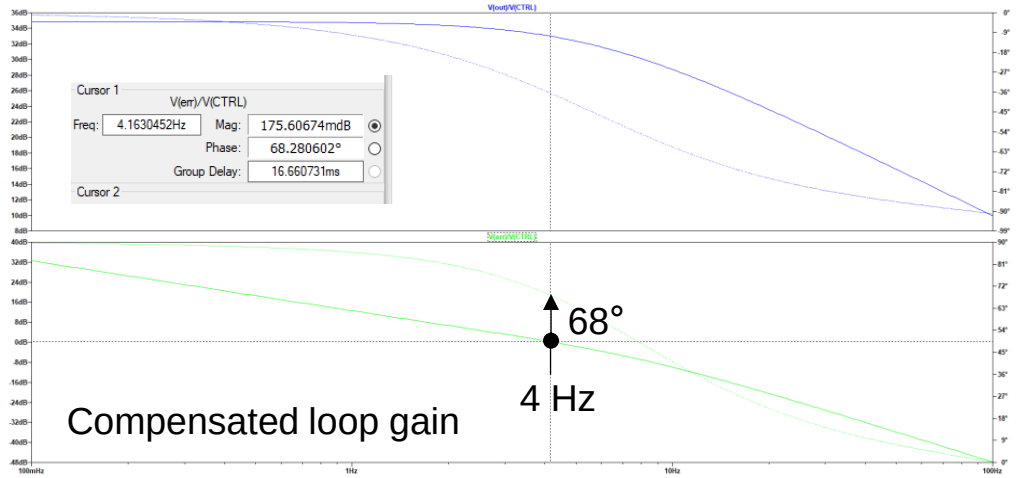


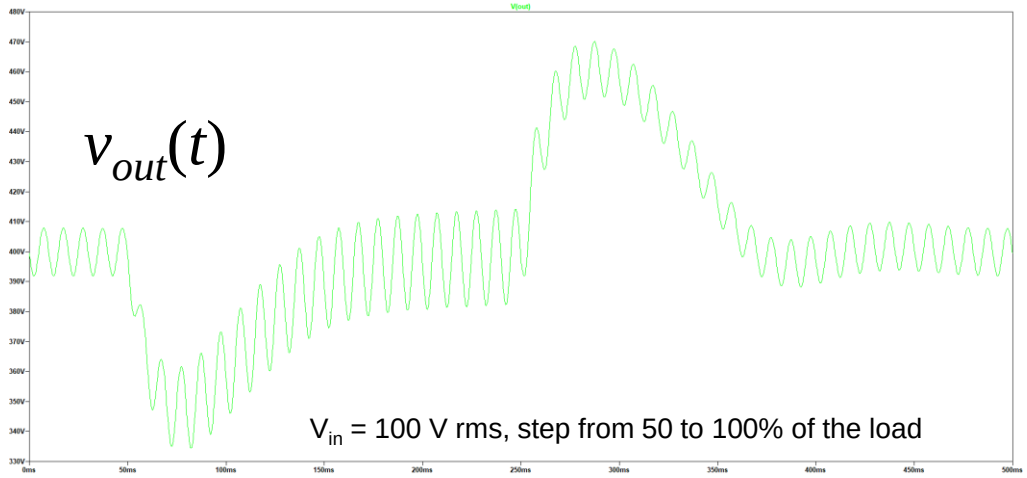
Stability Analysis and Compensation

- An averaged model lets you quickly obtain the control-to-output transfer function
- Once in hand, you can think of a compensation strategy and immediately test it







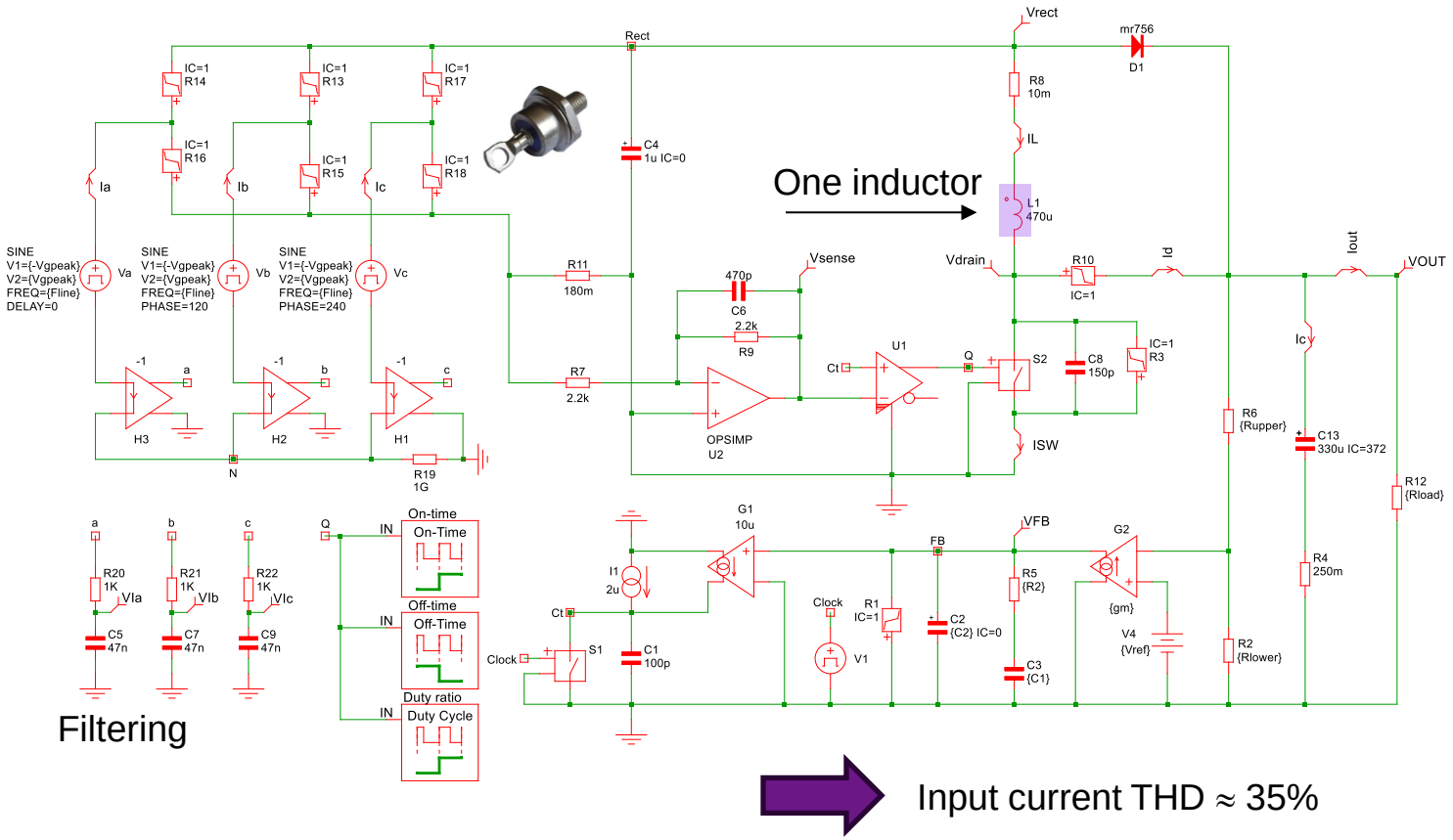


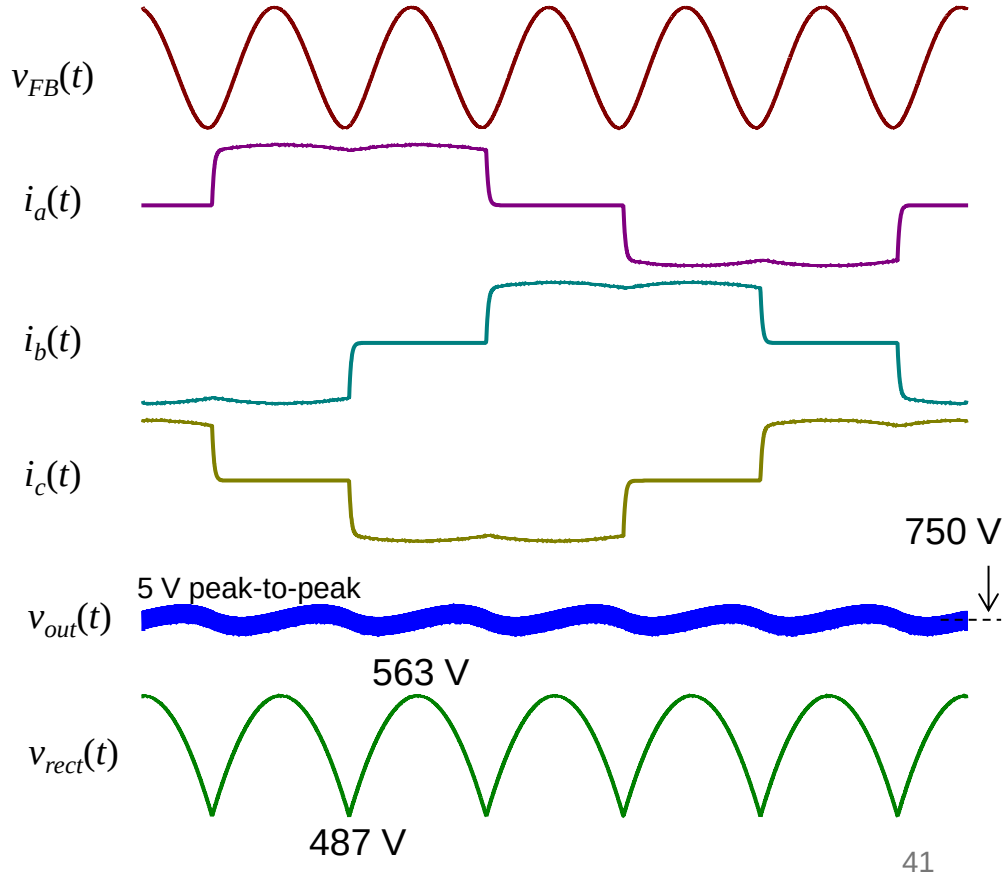
Agenda

- Notions of Power Factor
- PFC Architectures
- Processing Power – Single Phase
- Processing Power – Three Phases

Three-Phase Single-Switch Active PFC

- The classical boost structure does not lend itself for low-distortion current absorption
  - The input current is distorted considering the “hole” in input diodes conduction time
  - The high-voltage bus is typically regulated at 800 V dc for a 380/480-V ac input

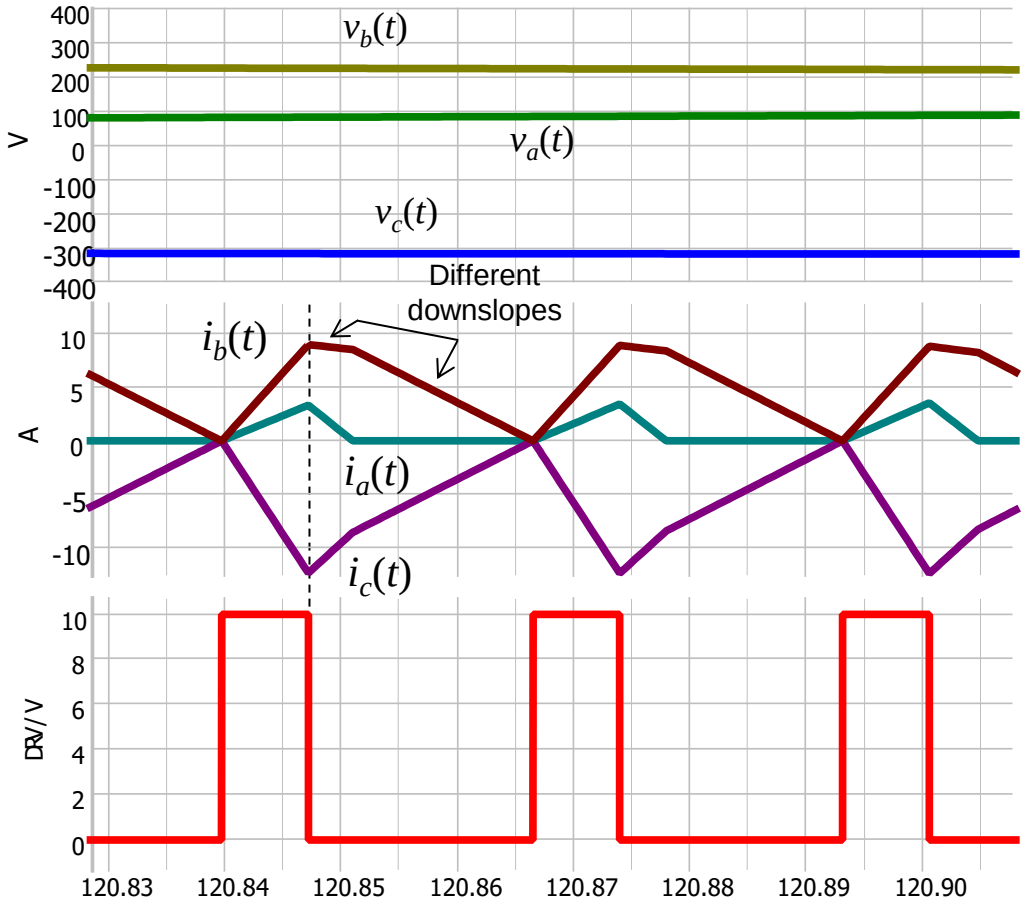


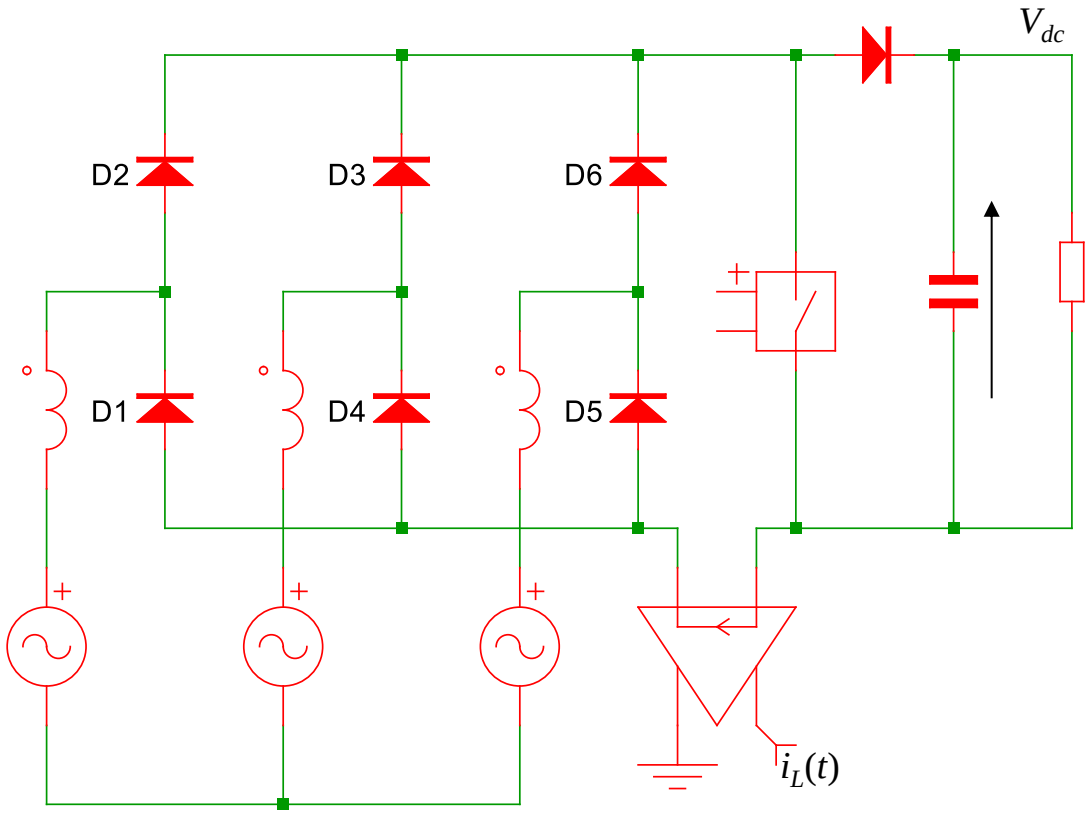


Single-Switch Borderline Operation

- Rather than using fixed-frequency operation, the PFC operates in borderline operation
- The total inductive current is sensed, ensuring no inductor operates in CCM

✓ No particular control law, classical free-running operation, constant on-time

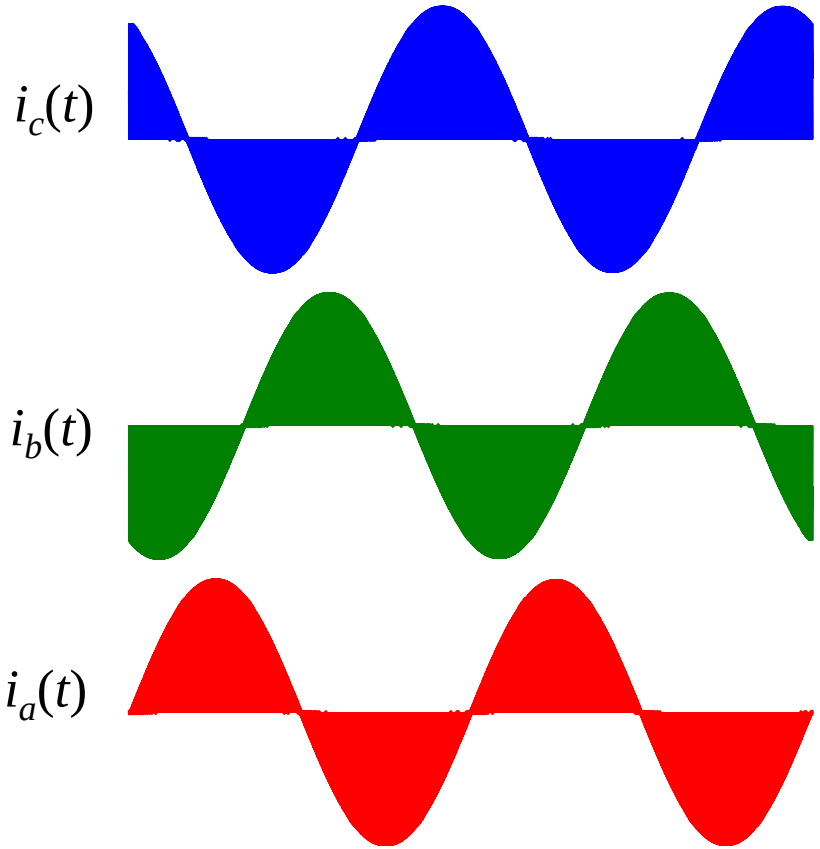




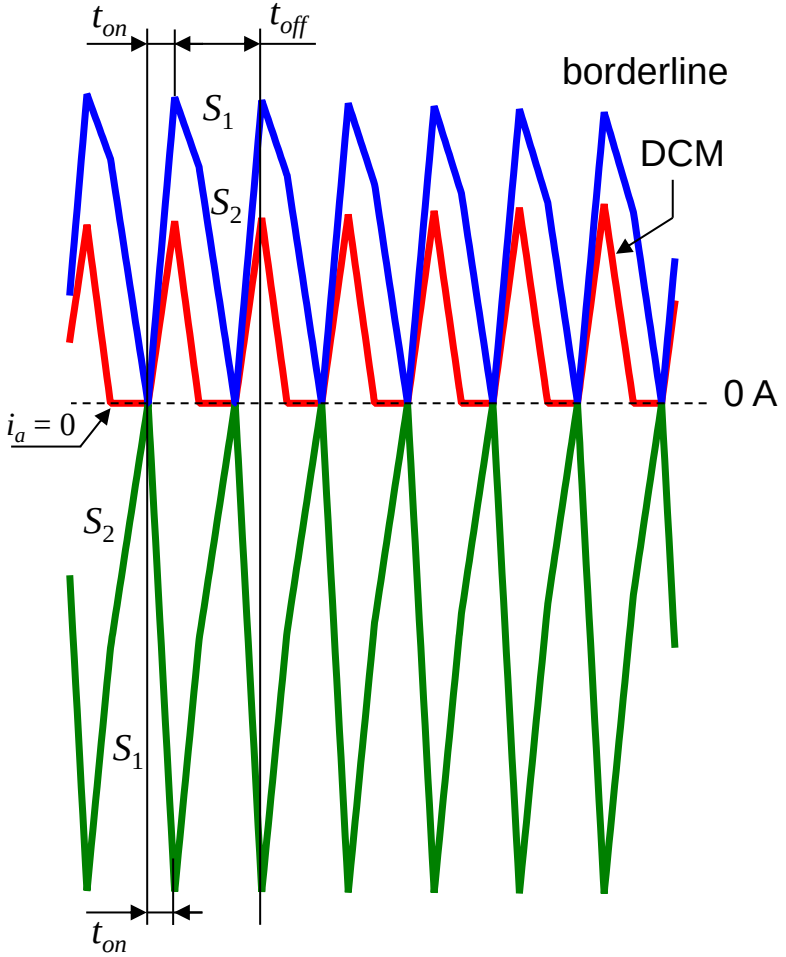
D. S. L. Simonetti, J. Sebastian and J. Uceda, *Single-switch three-phase power factor preregulator under variable switching frequency and discontinuous input current*, *Proceedings of IEEE Power Electronics Specialist Conference - PESC '93*

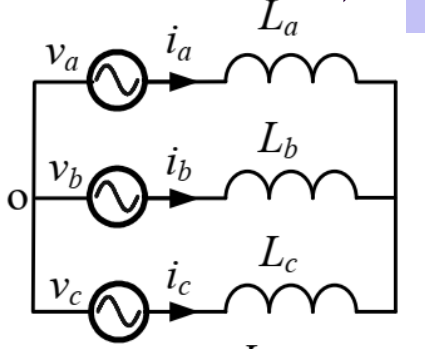
Non-Sinusoidal Average Inductor Current

- The inductor currents go through different downslopes at the switch turn-off
- The input current envelope is sinusoidal but not the average current ➡ $\langle i_L(t) \rangle_{T_{sw}} \neq \frac{I_{L,peak}}{2}$



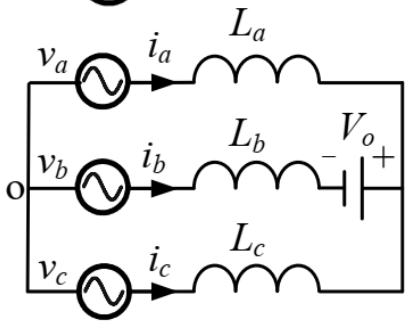
$$i_a(t) + i_b(t) + i_c(t) = 0$$



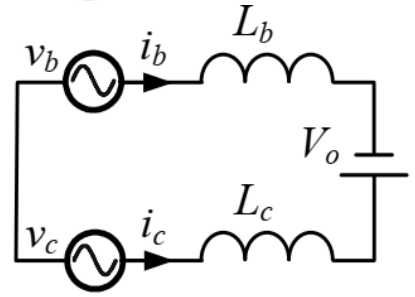


Mains switch is turned on:

$$S_k = \frac{V_k}{L_k}$$



Mains switch is turned off, diode D_b conducts

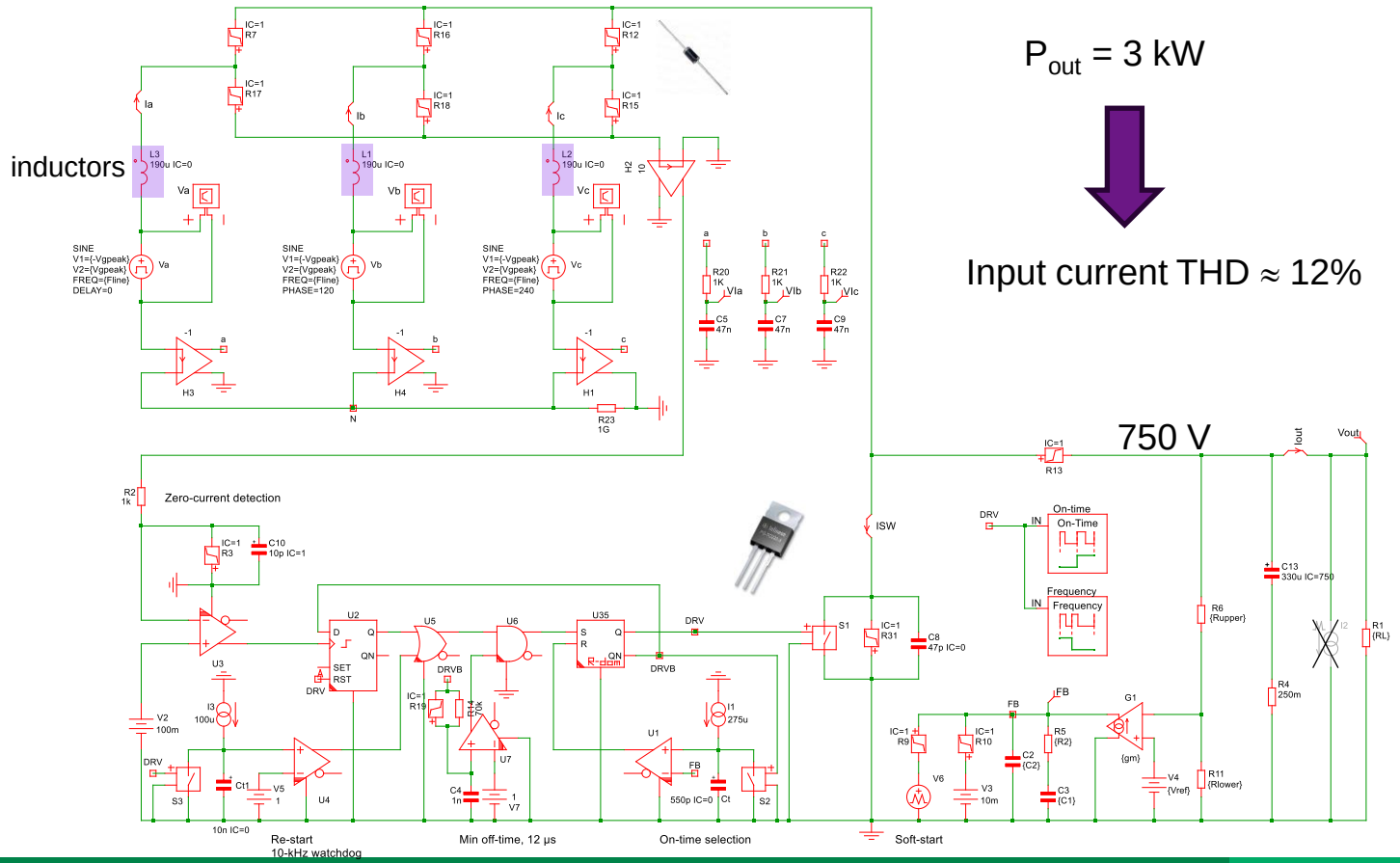


Mains switch is turned off, $i_a = 0$

K. Yao et al., *A Novel Control Scheme of Three-Phase Single-Switch Quasi-CRM Boost Rectifier*, *IEEE Transactions on Power Electronics*, vol. 32, no. 8, August 2017

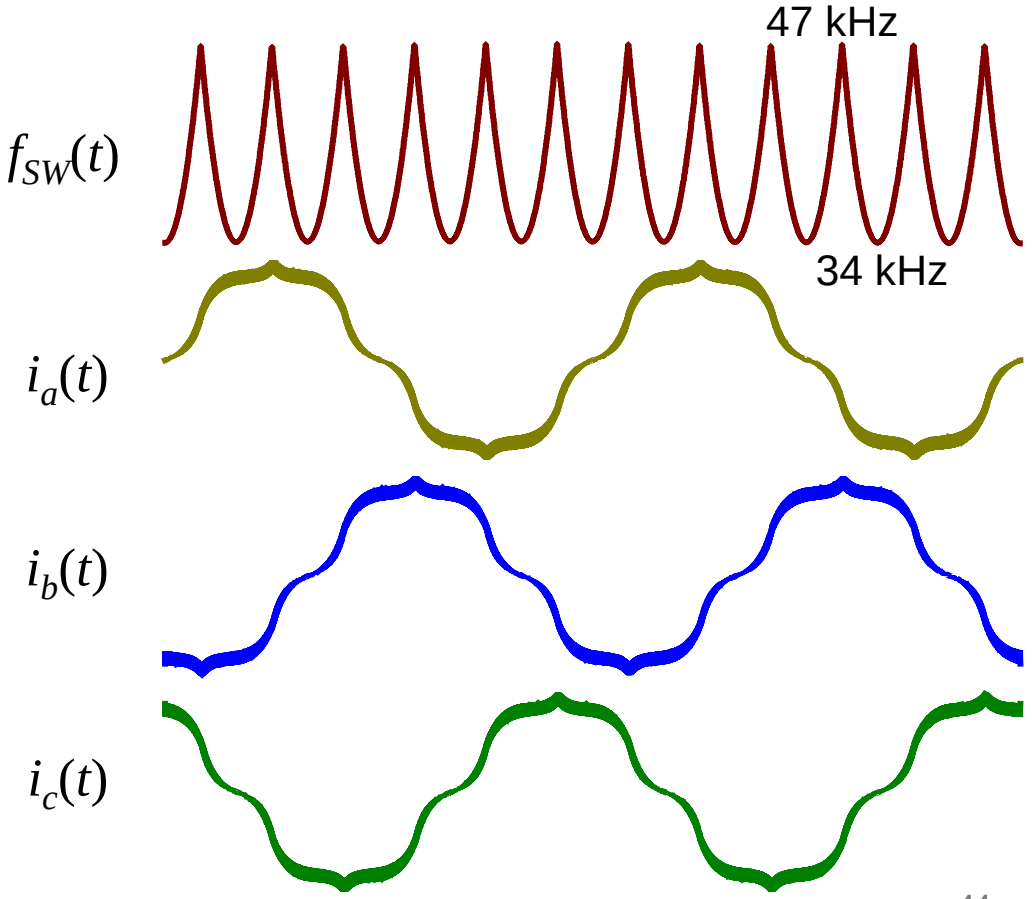
Simulation of the BCM 3-Phase PFC

- You can implement a BCM circuit where the inductive current is always discontinuous
- ✓ No CCM operation hence lower switching losses at turn-on
- ❖ Requires a high-voltage output to minimize input current distortion



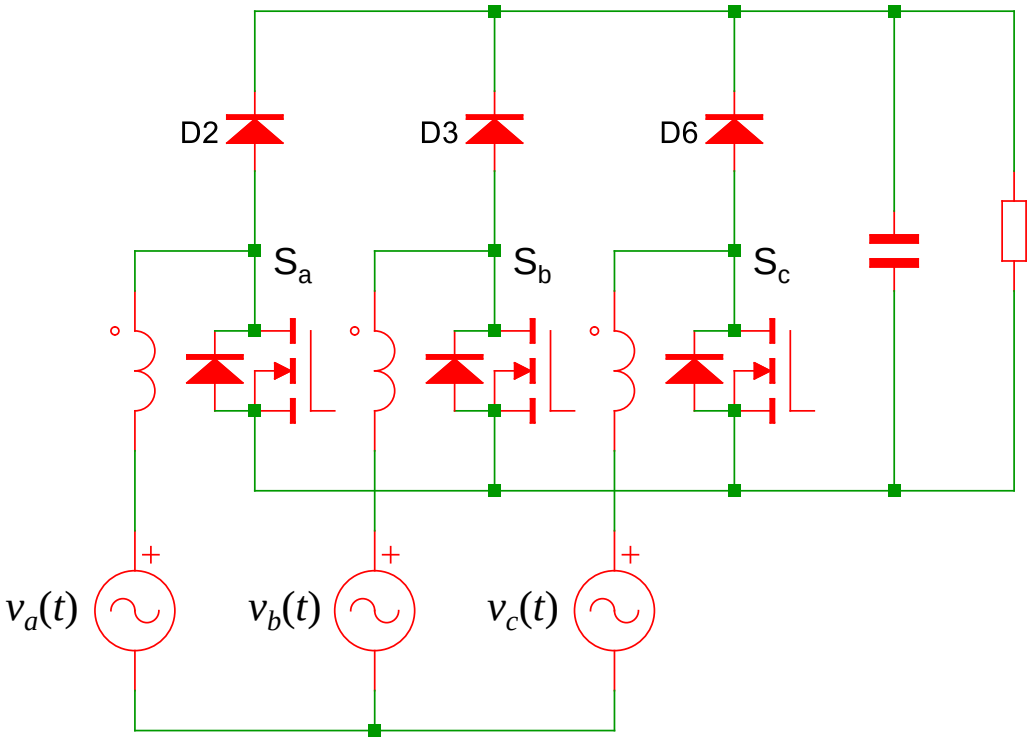
P_{out} = 3 kW

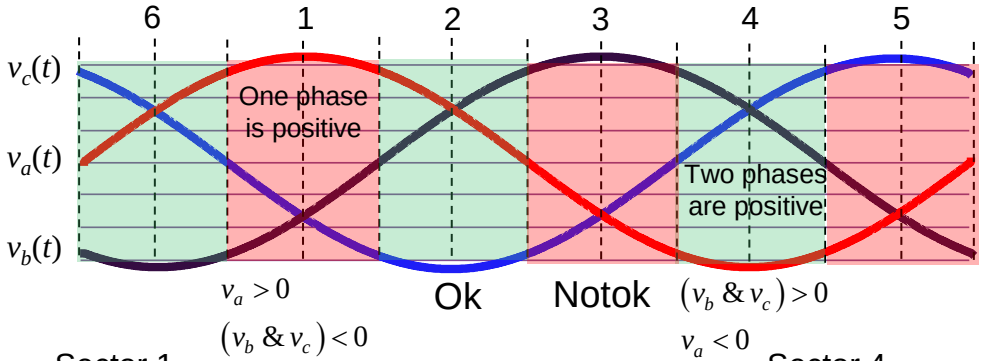
Input current THD ≈ 12%



Three-Phase PFC – Identifying Sectors

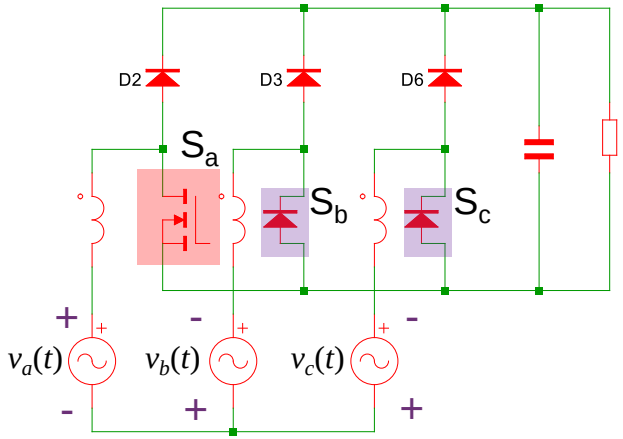
- This hybrid half-controlled 3-switch PFC cannot achieve a sinusoidal input current
- ✓ You can only impress a sinusoidal shape if at least *two* phases are controlled
- ❖ The equation $i_a(t) + i_b(t) + i_c(t) = 0$ could lead to a sinusoidal input only in a few sectors





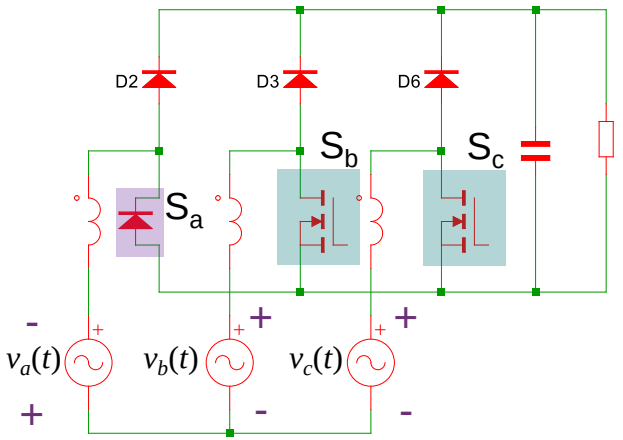
Sectors
6-2-4
1-3-5

Sector 1



S_b and S_c switches have no effect as body diodes conduct

Sector 4

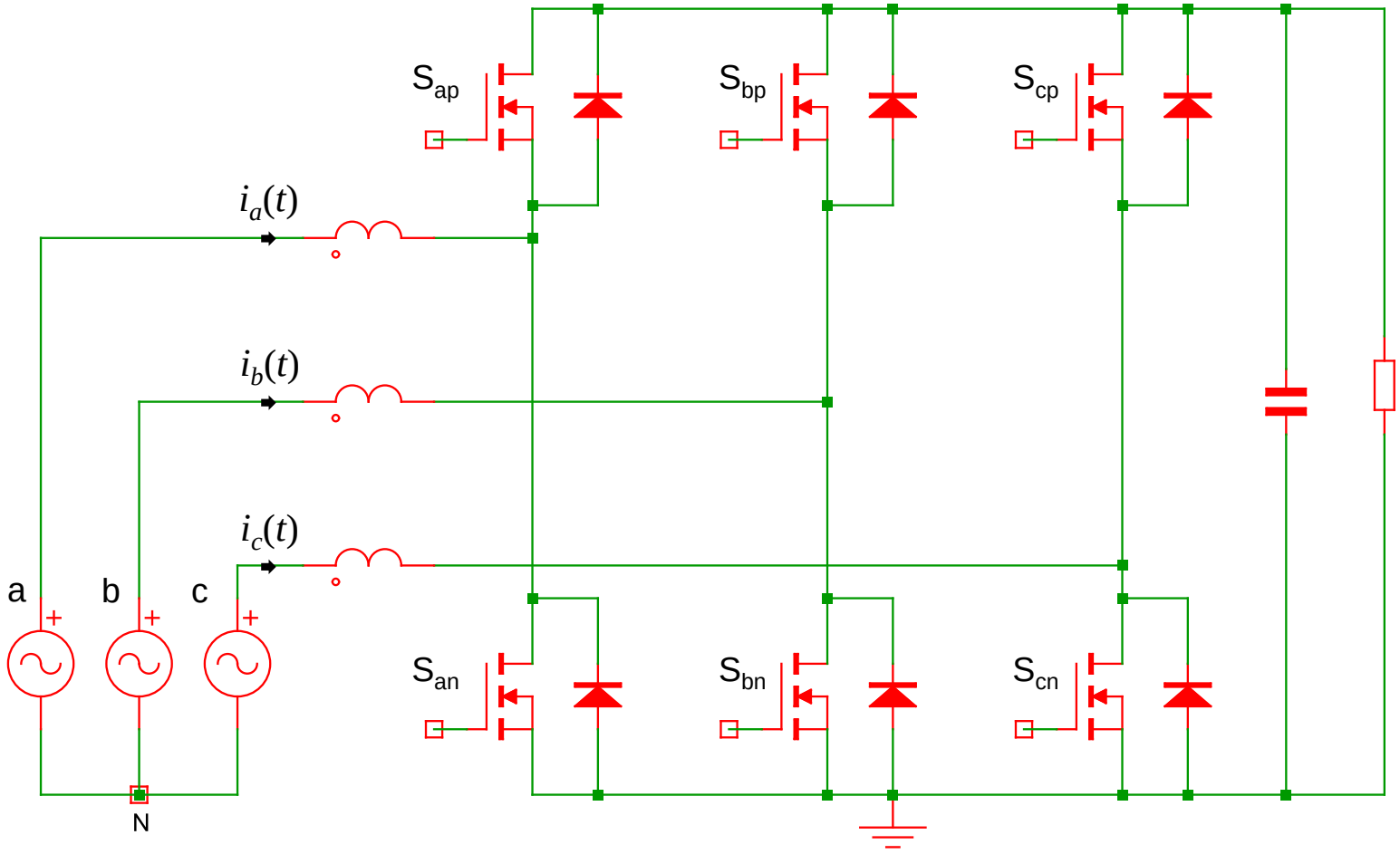


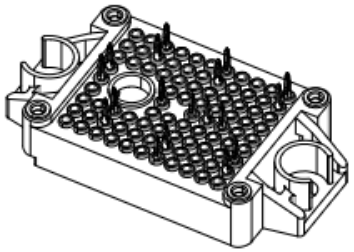
S_b and S_c are driven, S_a body conducts: $i_a = -(i_b + i_c)$

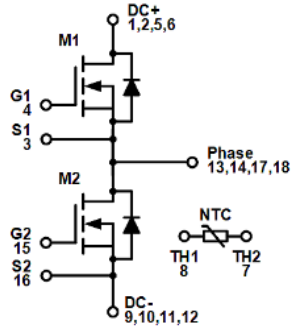
J. W. Kolar and T. Friedli, *The Essence of Three-Phase PFC Rectifier Systems—Part I*, *IEEE Transactions on Power Electronics*, vol. 28, no. 1, Jan. 2013

Six-Switch or Sixpack Configuration

- This is a 2-level bidirectional boost converter allowing sinusoidal current absorption
- Several techniques exist to control the power switches like 6-step modulation and dq0



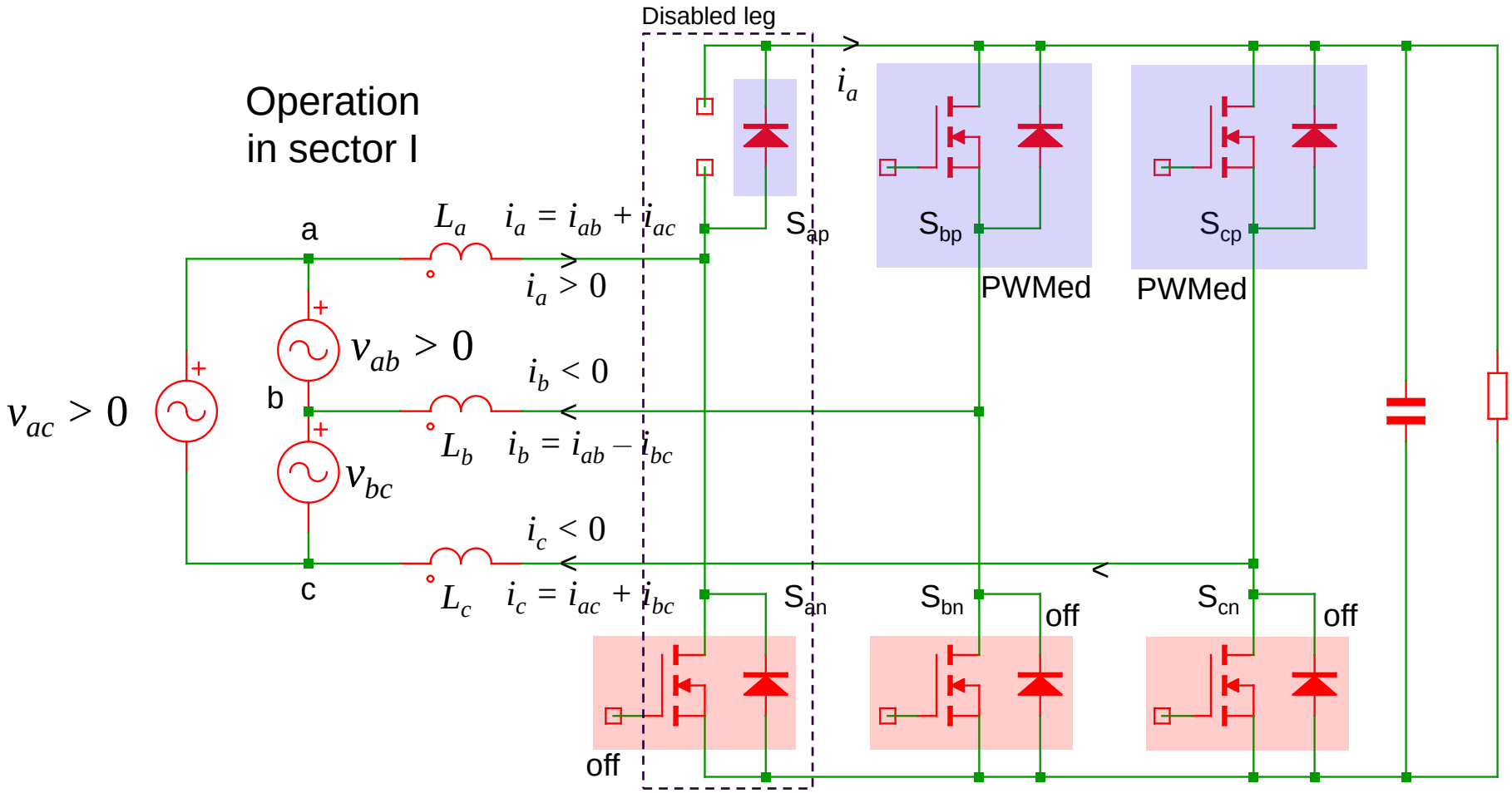


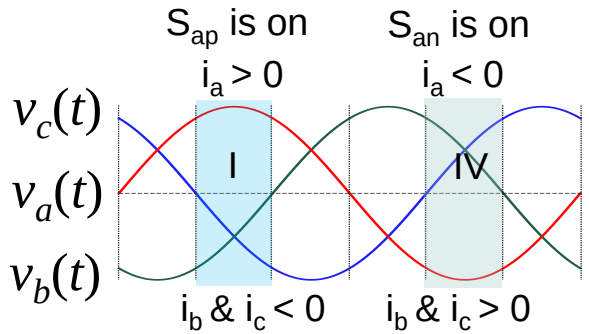


onsemi [SEC-25KW-SIC-PIM-GEVK]

6-Step Operation Needs Logic Decoding

- You cannot impress a sinusoidal shape to phase A in sector 1 as S_{ap} conducts
- Two legs are made active while one of them is kept passive





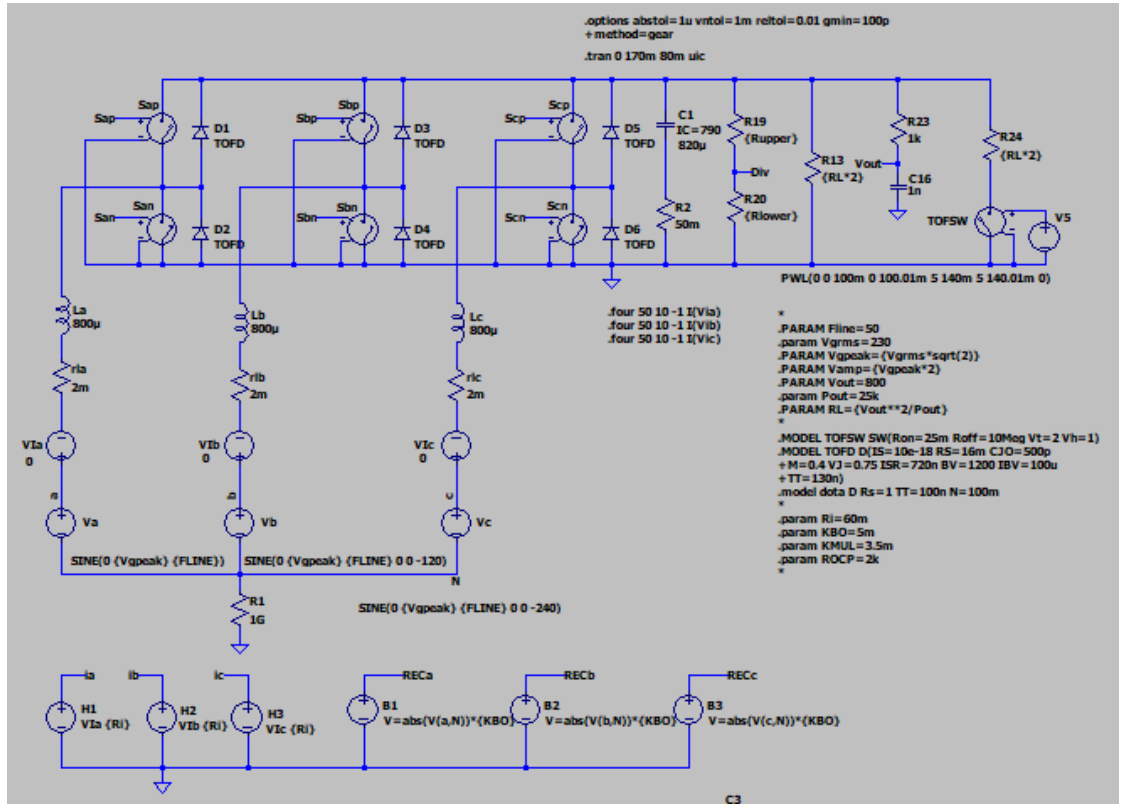
- ✓ S_{ap} is on permanently in sector I – S_{bp} & S_{cp} PWMed
- ✓ S_{an} is on permanently in sector IV – S_{bn} & S_{cn} PWMed

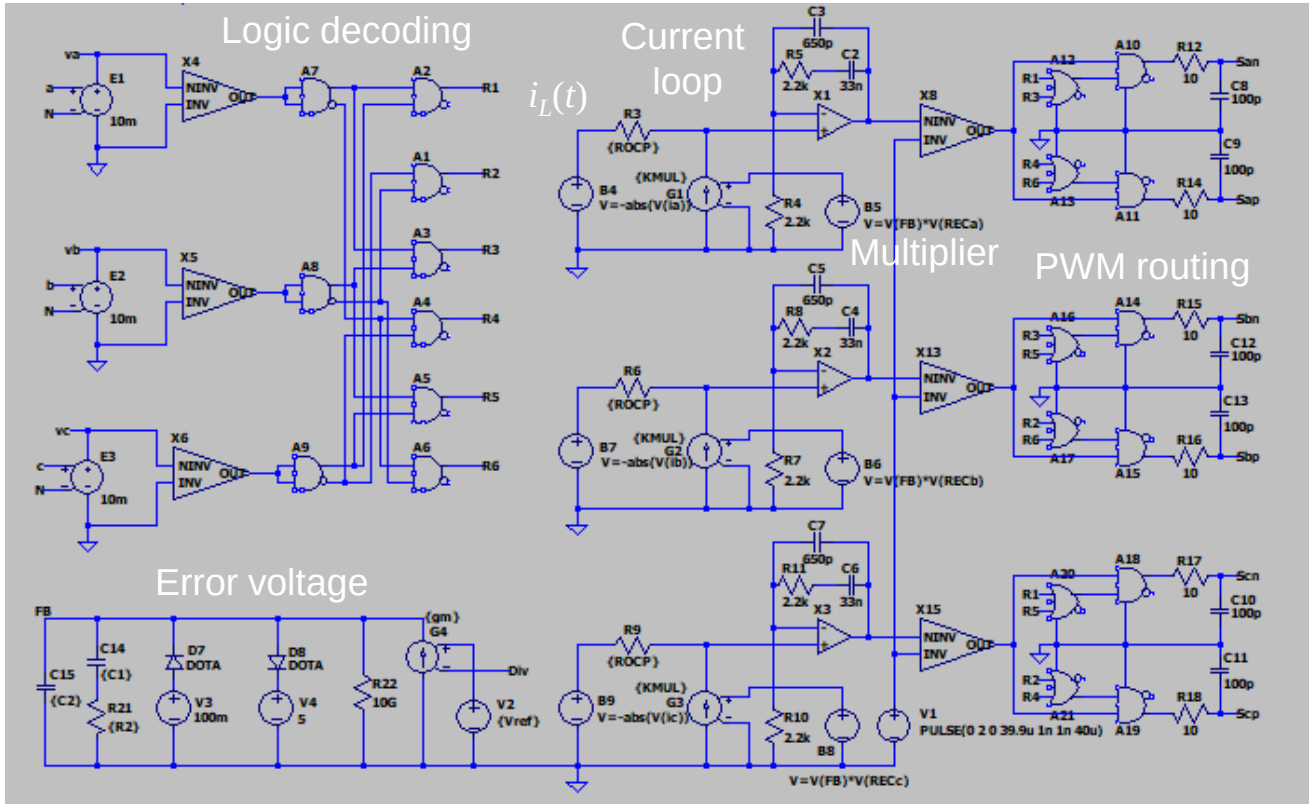
- ➢ Leg A is off in sectors I and IV
- ➢ Leg B is off in sectors III and VI
- ➢ Led C is off in sectors II and V

L. Huber, M. Kumar and M. M. Jovanović, *Performance comparison of three-step and six-step PWM in average-current-controlled three-phase six-switch boost PFC rectifier*, APEC 2015

Six-Pack Simulation with LTspice

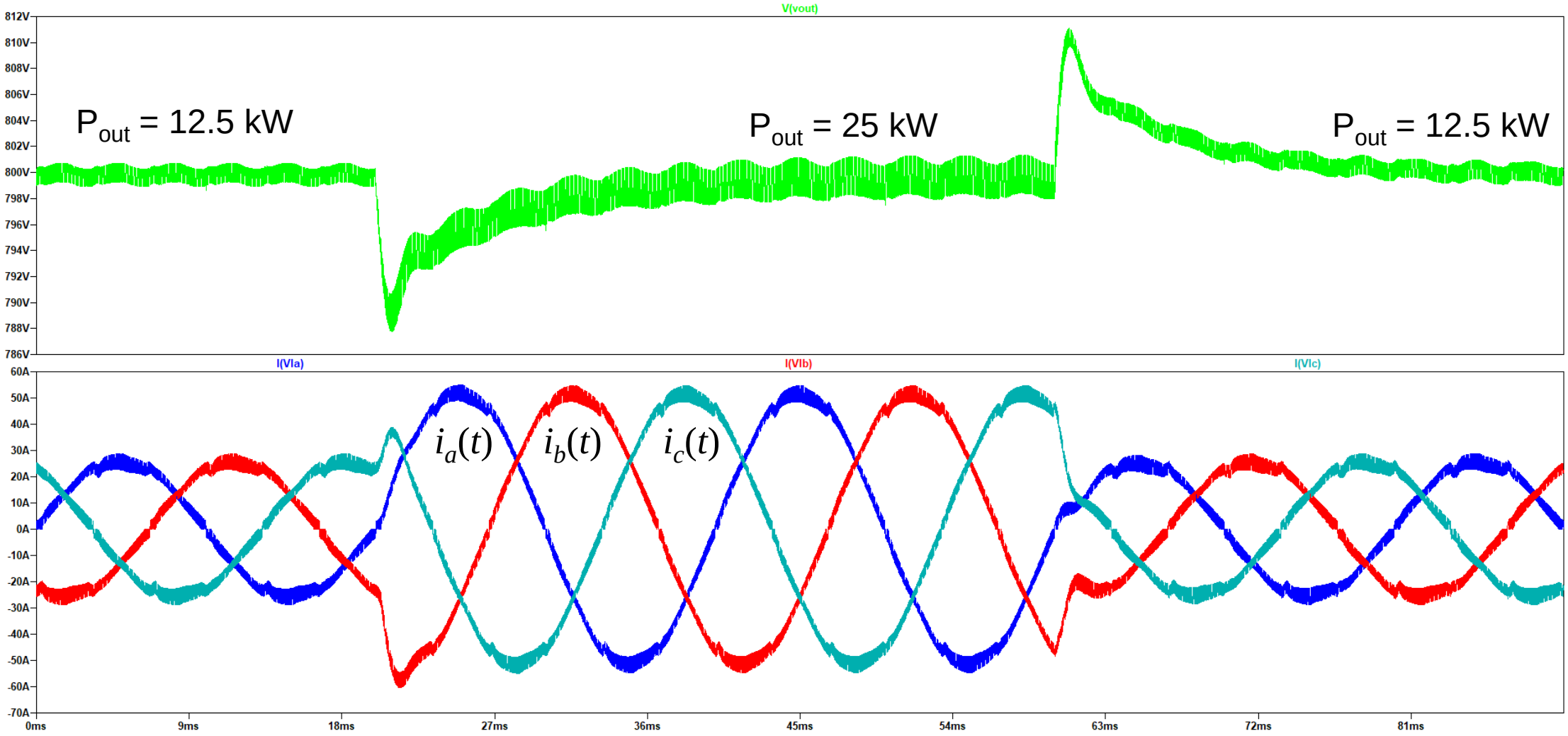
- The PFC is supplied from a 400-V phase-to-phase level and delivers 800 V/25 kW
- The switching frequency is 25 kHz – the loop has been compensated with SIMPLIS
- Three multipliers are used to shape the inductor current envelope





Testing the Transient Response

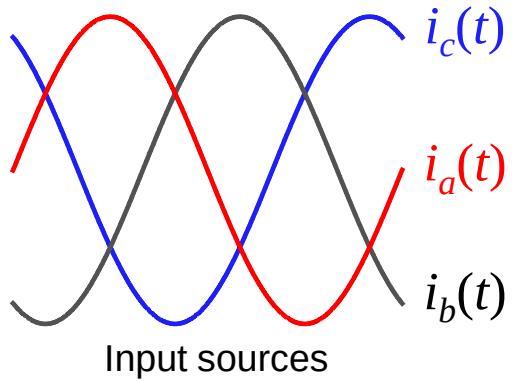
- The transient response from 50% to 100% of nominal power is excellent



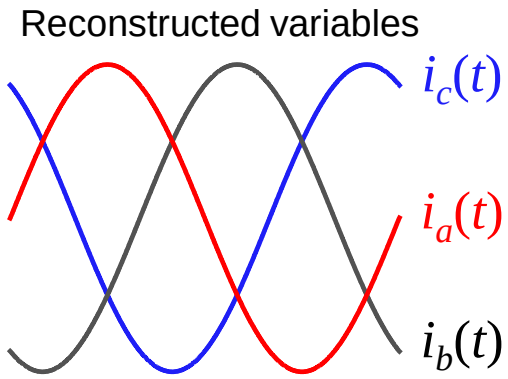
The dq0 Transformation

- We have three sinusoidal voltage sources and we want a resistive input
- We can transform the 3-variable input into two dc components, d and q
- Perform regulation on d and q and convert back into three sinusoidal setpoints

$$\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$



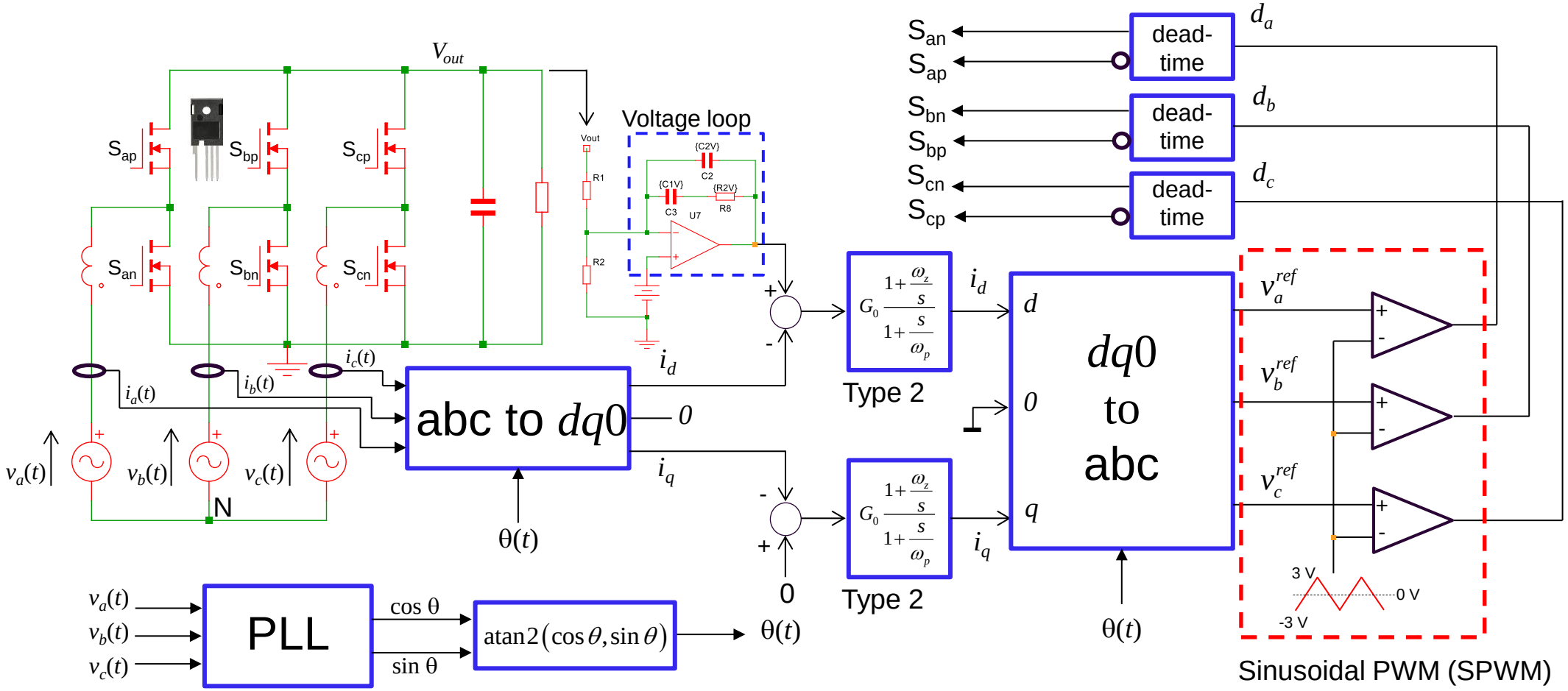
✓The inverse *dq0* reconstructs the corrected waveforms after corrected *d* and *q* variables



$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & -\sin(\theta) & \frac{\sqrt{2}}{2} \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}$$

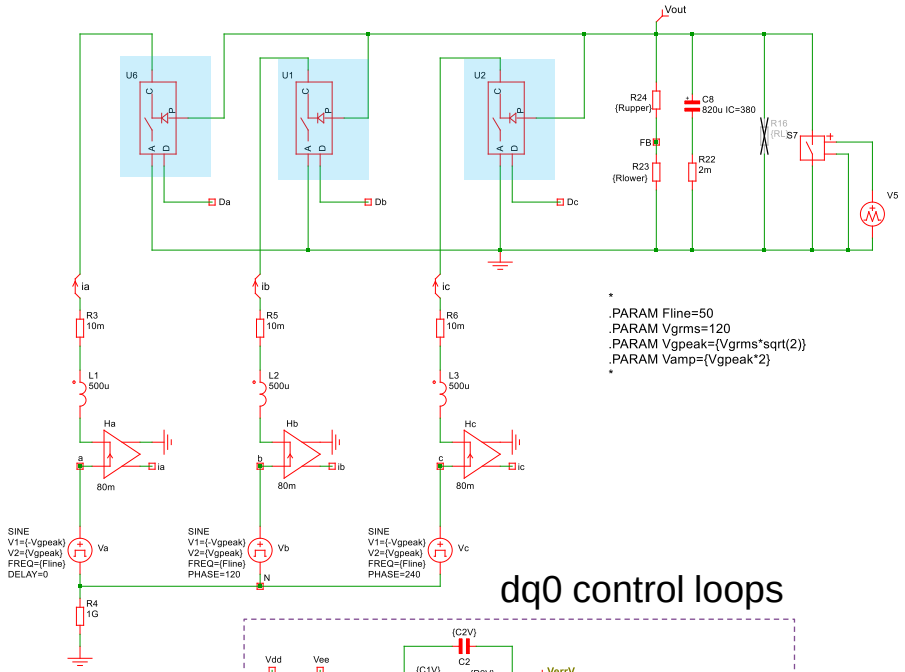
Three-Phase Rectifier with SPWM

- A phase-locked loop (PLL) is used for extracting the angle θ
- Each input current is sensed and used to compute $dq0$ variables with θ

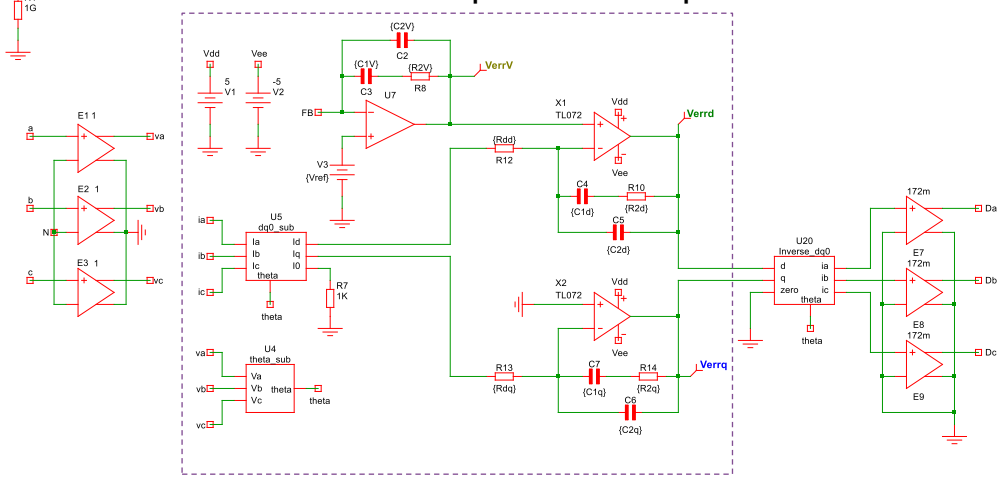


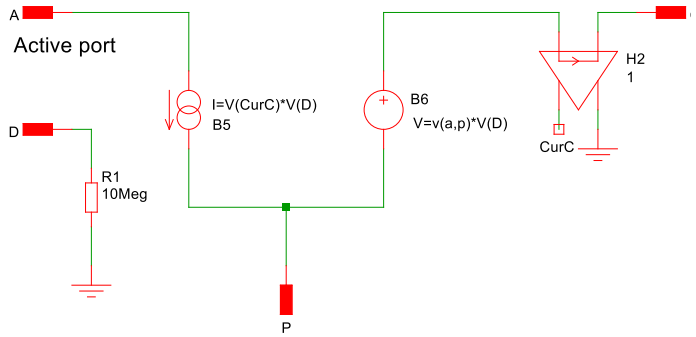
Average Modeling of the Whole Chain

- The PWM switch model lends itself perfectly for this 3-phase PFC ac simulation



dq0 control loops



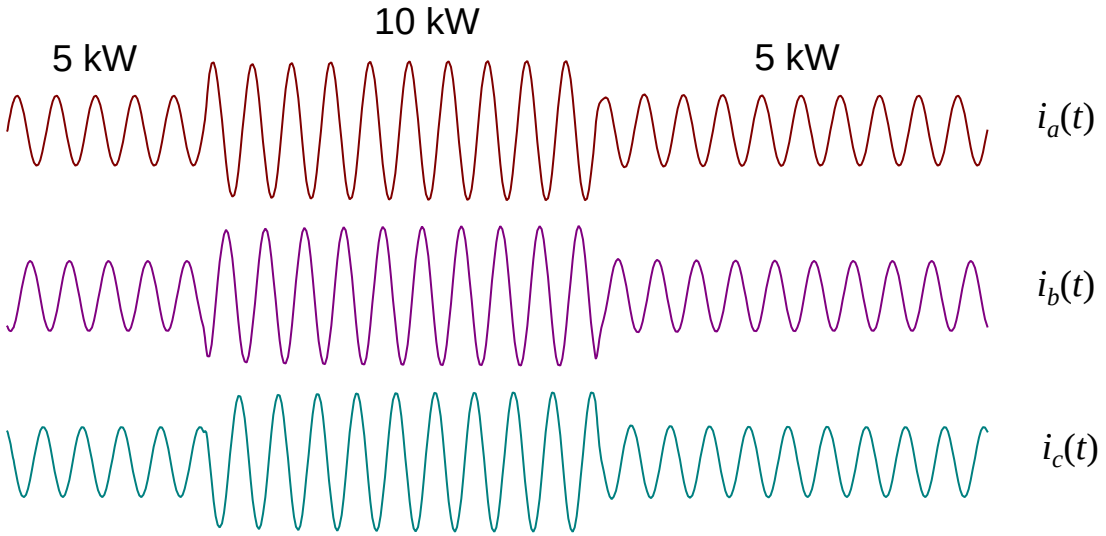


Simplified Analysis of PWM Converters Using Model of PWM Switch Part I: Continuous Conduction Mode

VATCHÉ VORPÉRIAN
Virginia Polytechnic Institute and State University

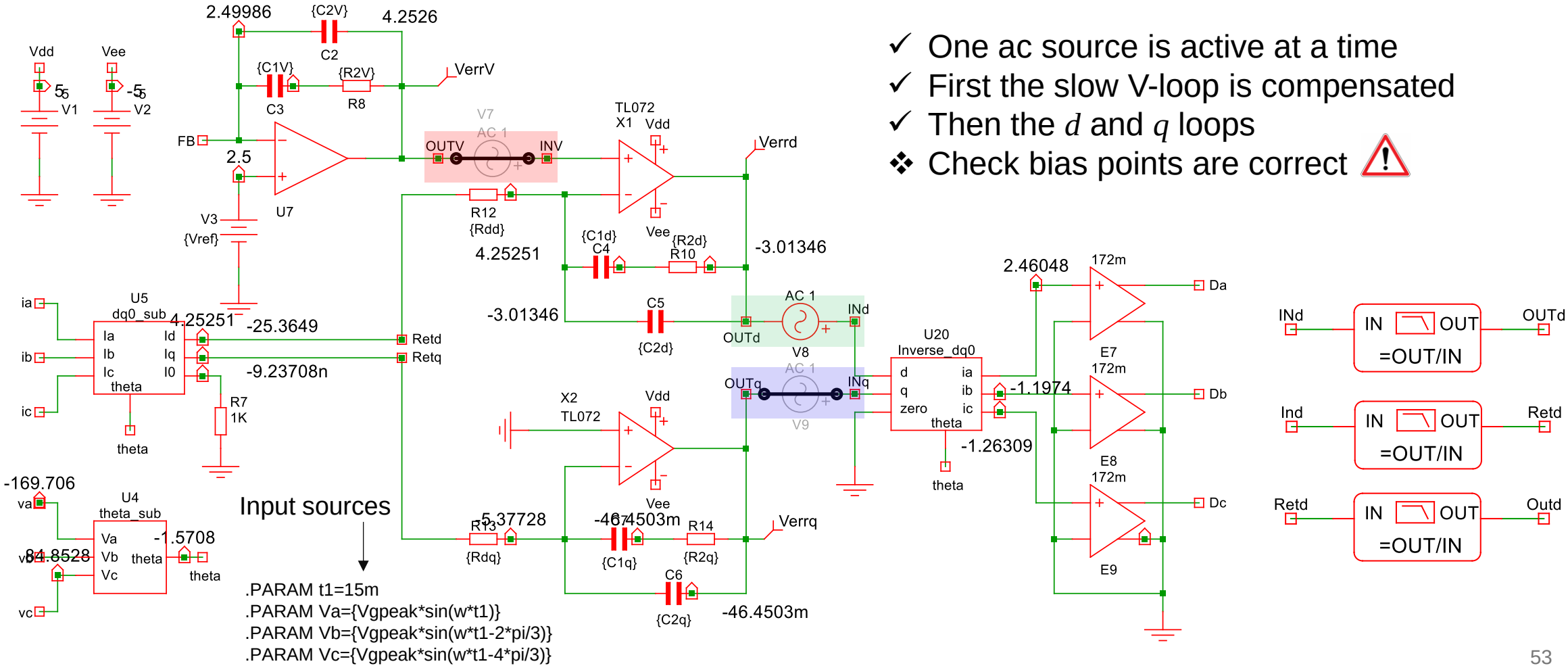
V. Vorpérian, *Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode*, in *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, no. 3,, May 1990

- I have replaced the switching cell by the VM PWM switch model
  - Pulse-width modulators are replaced by small-signal gains



Three Loops have to be Compensated

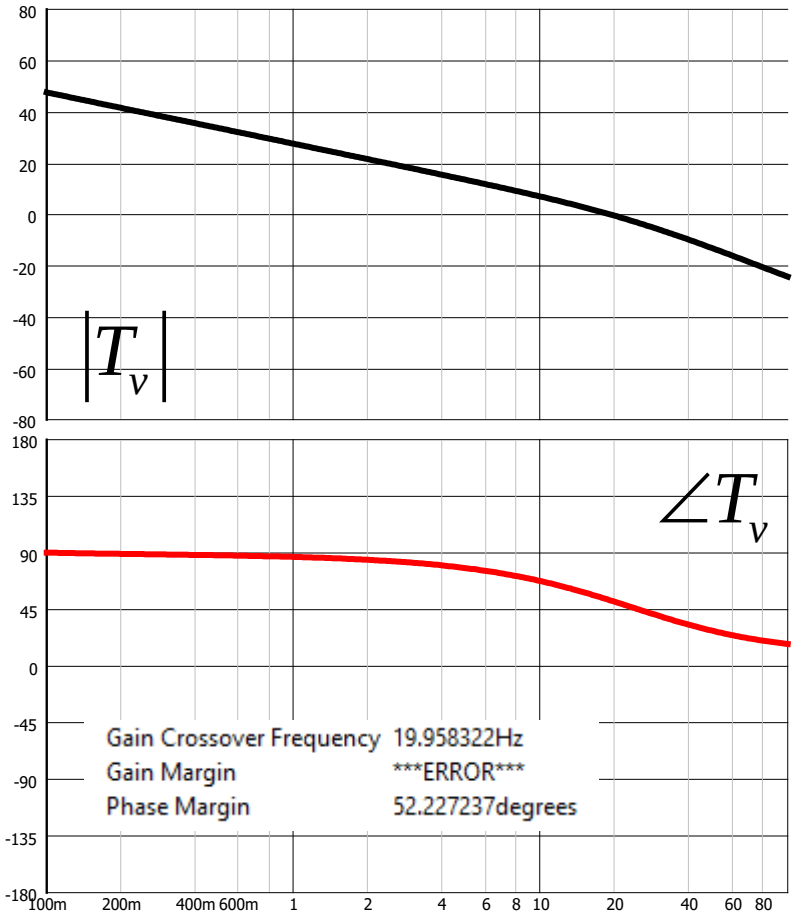
- Three loops: V_{out} to be regulated at 400 V and the d and q paths
- The voltage loop will be closed with a 20-Hz crossover while f_c for d and q will be 2 kHz



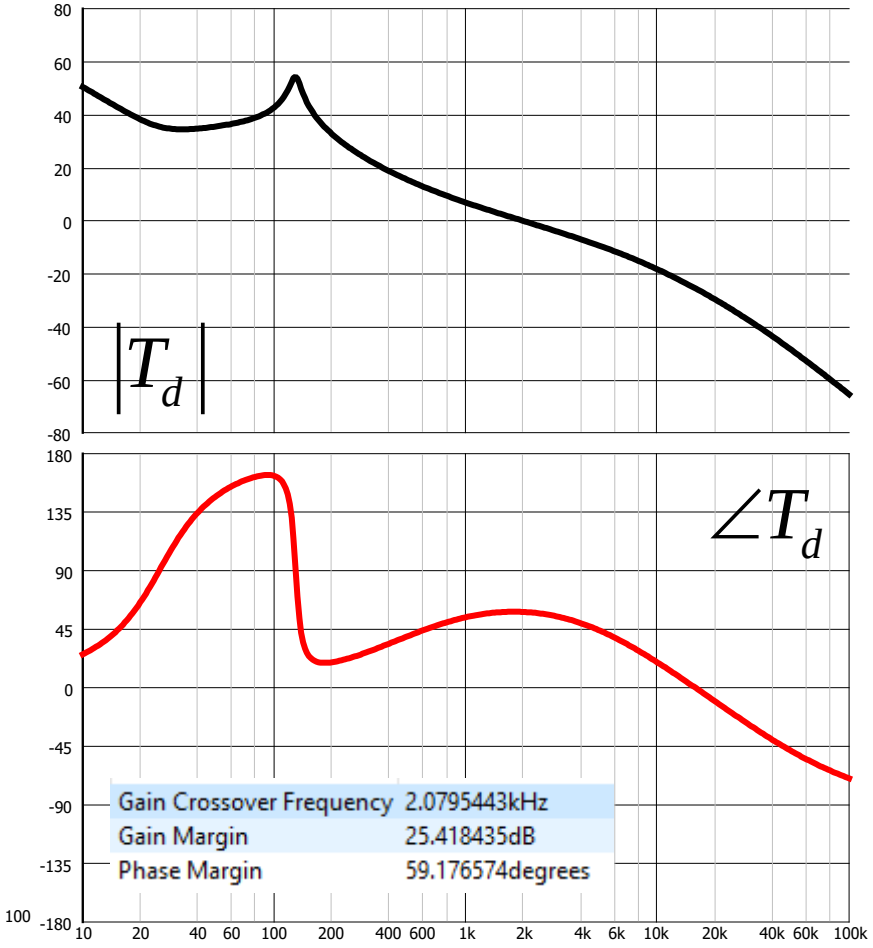
- ✓ One ac source is active at a time
- ✓ First the slow V-loop is compensated
- ✓ Then the d and q loops
- ❖ Check bias points are correct

All Loops show Comfortable Margins

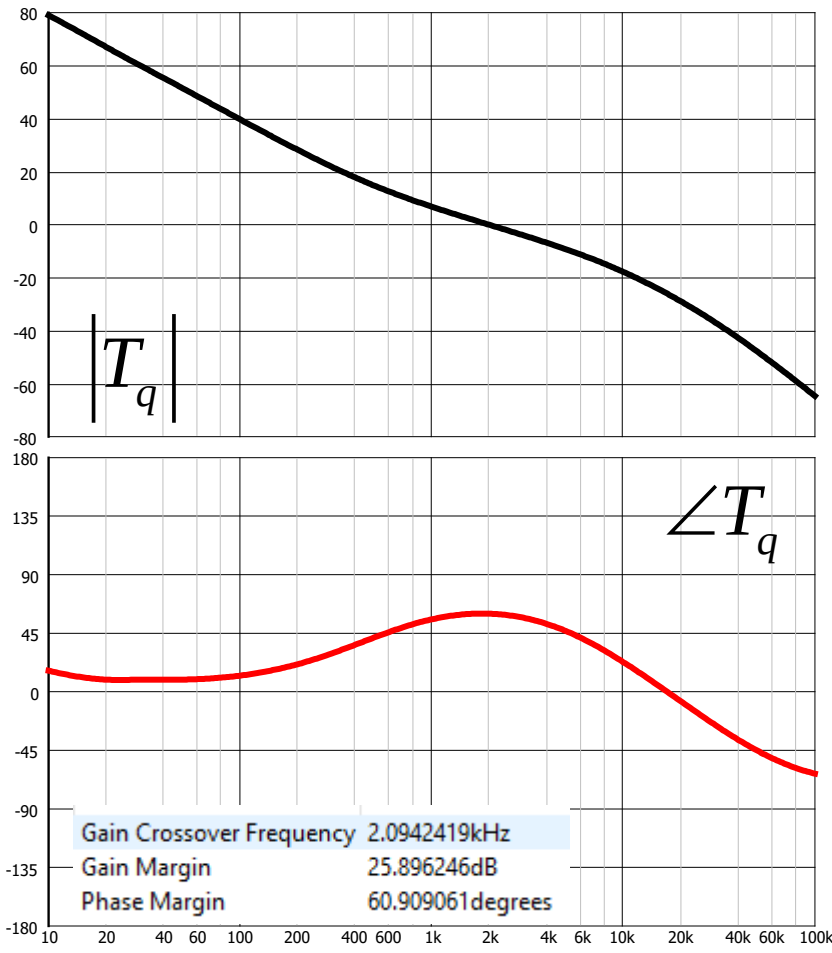
- The three loops are individually compensated with adequate phase and gain margins



Voltage loop – f_c = 20 Hz



d loop – f_c = 2 kHz

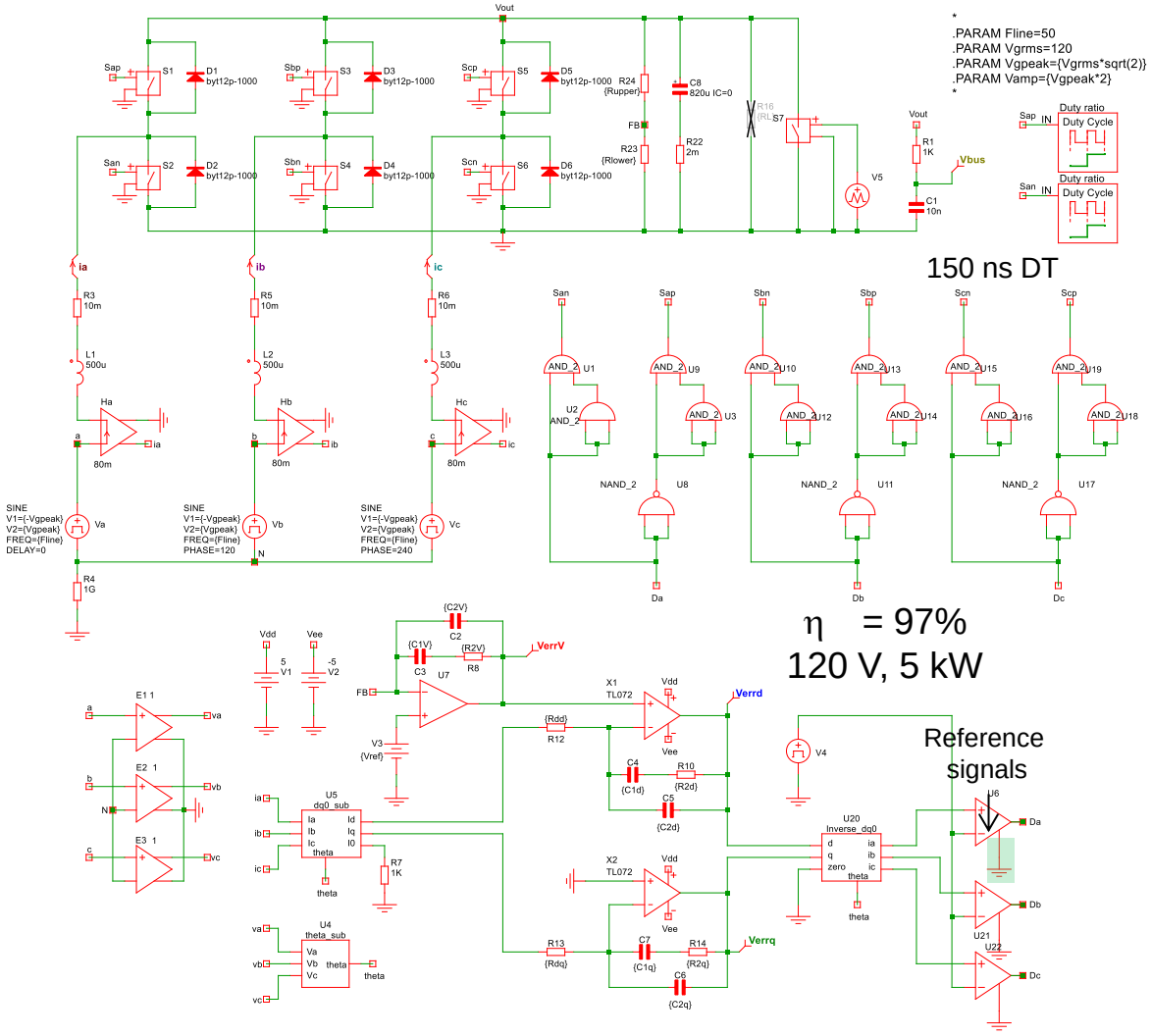


q loop – f_c = 2 kHz

Cycle-by-Cycle Simulation with SIMetrix

FUTURE ELECTRONICS
A WT Microelectronics Company

- This cycle-by-cycle SIMetrix simulation is fast and gives results in less than 5 mn



- There are three compensators in this circuit
- The voltage loop is compensated for a low crossover
- The inner current loops are faster ≈ 1-2 kHz
- The converter delivers 5 kW from a 120-V ac input

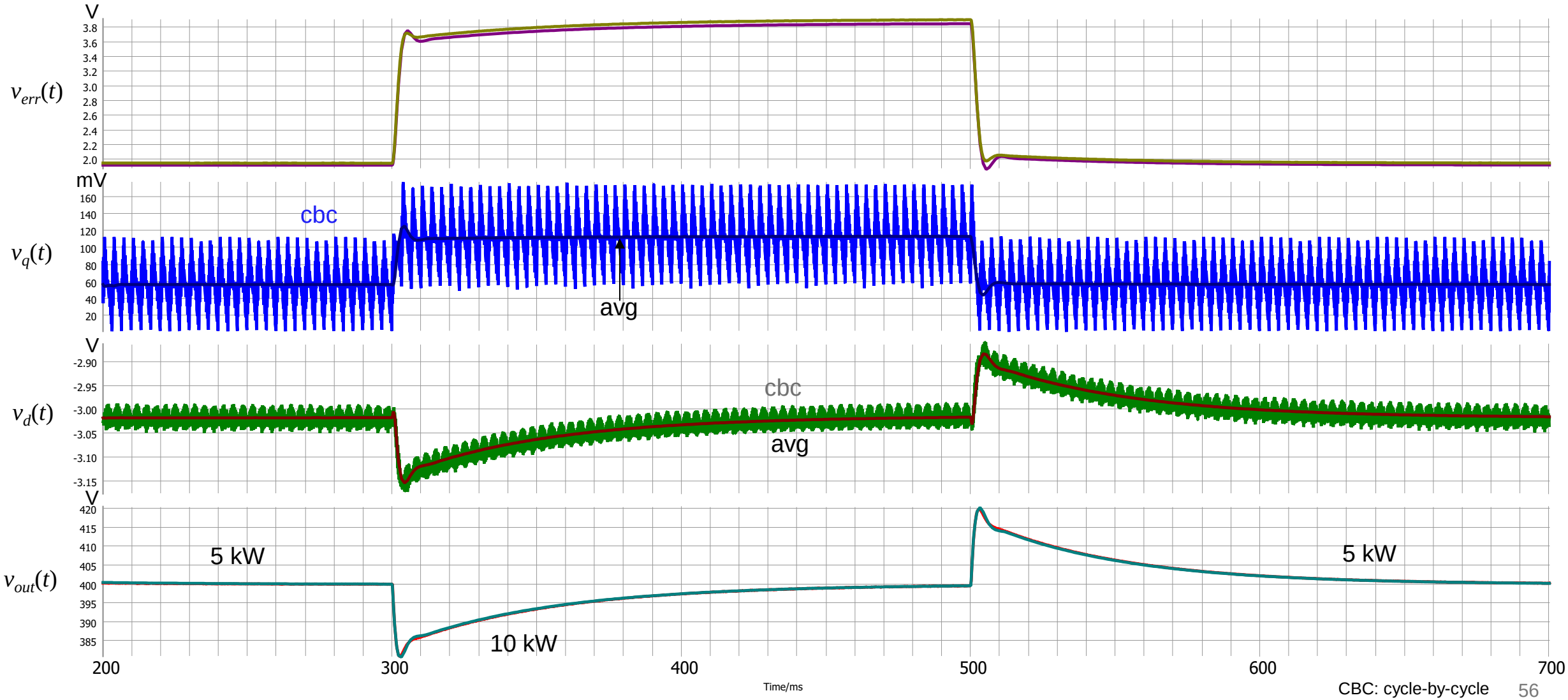

```
.param GfcV=20 ; magnitude at crossover *
.param PSV=-90 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fcV=20 ; targeted crossover *
.param PMV=60 ; choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Vout=400
.param Pout=5k
.param RL={(Vout)^2/(Pout)}
.param Ibias=100u
.param Vref=2.5
.param Rlower={Vref/Ibias}
.param Rupper={(Vout-Vref)/Ibias}
```

```
*
* Do not edit the below lines *
.param boostV={PMd-PSd-90}
.param GV={10^(-GfcV/20)}
.param kV={tan((boostV/2+45)*pi/180)}
.param fpV={fcV*kV}
.param fzV={fcV/kV}
.param C2V={1/(2*pi*fcV*GV*kV*Rupper)}
.param C1V={C2V*(kV^2-1)}
.param R2V={kV/(C1V*2*pi*fcV)}
```

Type 2 voltage loop compensation

Now compare Averaged and CBC Models

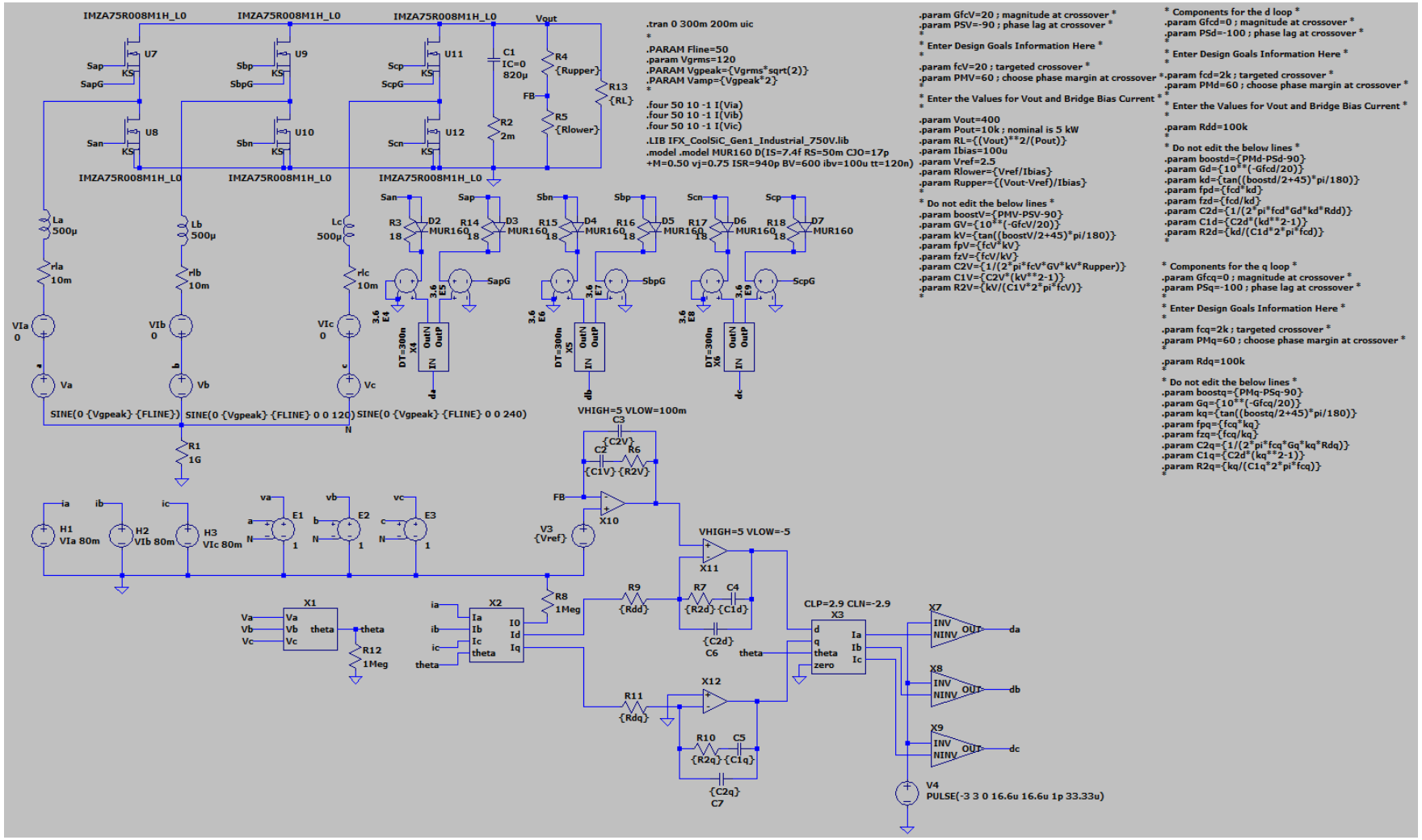
- Excellent correlation between cycle-by-cycle and average model waveforms



CBC: cycle-by-cycle

Simulation was also performed in LTspice

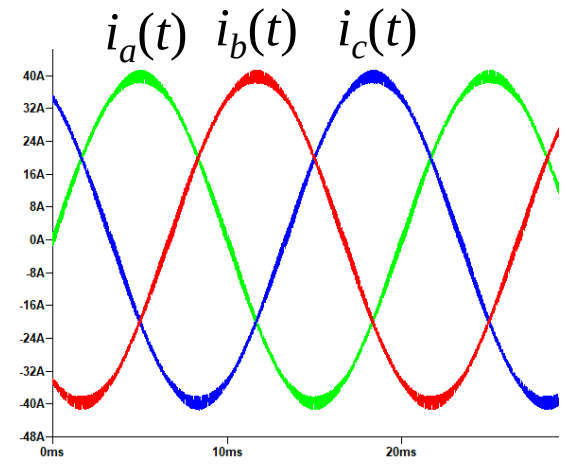
- LTspice can also run the entire simulation with SiC transistor models



CoolSiC™ MOSFET 750 V

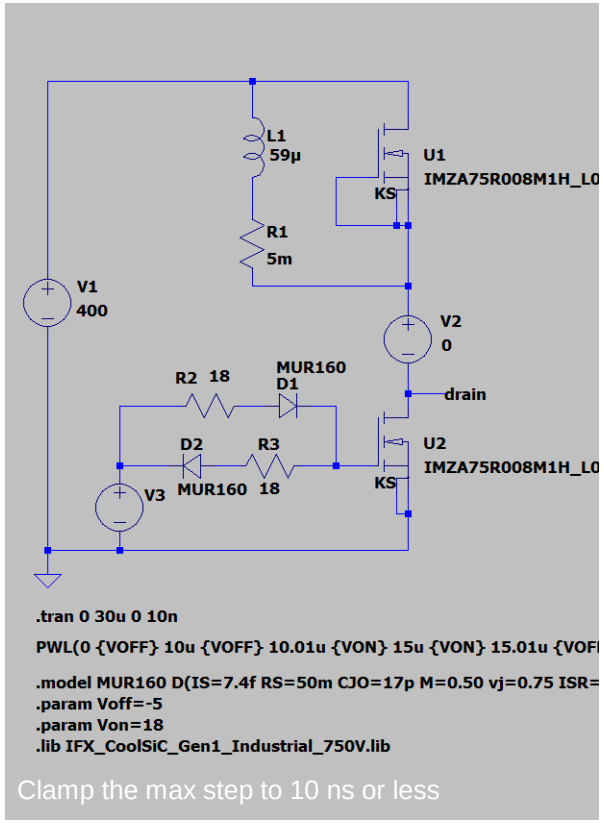
IMZA75R008M1H_L0

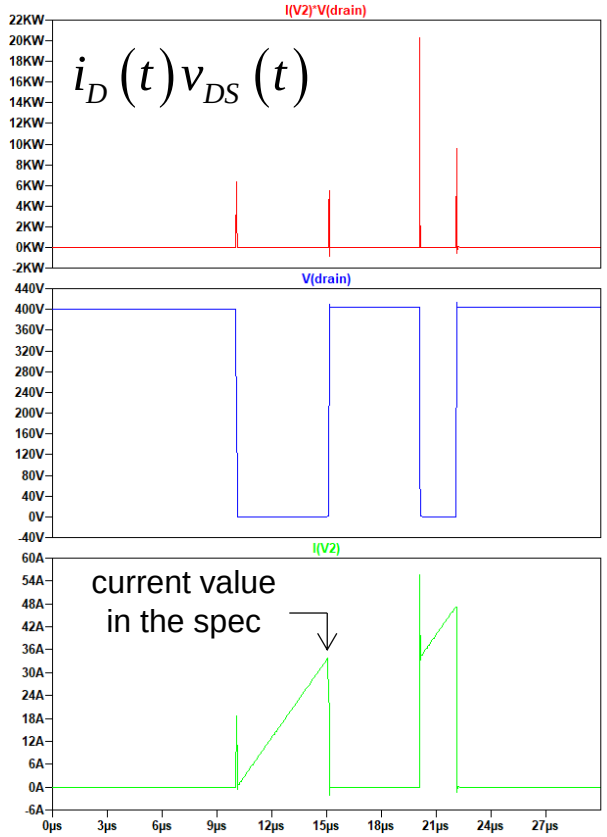

```
.SUBCKT SiCMOS_750V dd gg ss
*?@ Start SIMPLIS Encryption
    .PARAM fpar1 = {8.148}
    .PARAM fpar2 = {aabs/fpa
    .PARAM fpar3 = {abd_adj}
    .PARAM fpar4 = {abdch_ad
    .PARAM fpar5 = {23.1}
    .PARAM fpar6 = {aabs/fpa
    .PARAM fpar7 = {aabs_2*a
    .PARAM fpar8 = {rgint}
    .PARAM fpar9 = {4.27}
    .PARAM fpar10 = {17.67}
    .PARAM fpar11 = {cgs_aa/
```

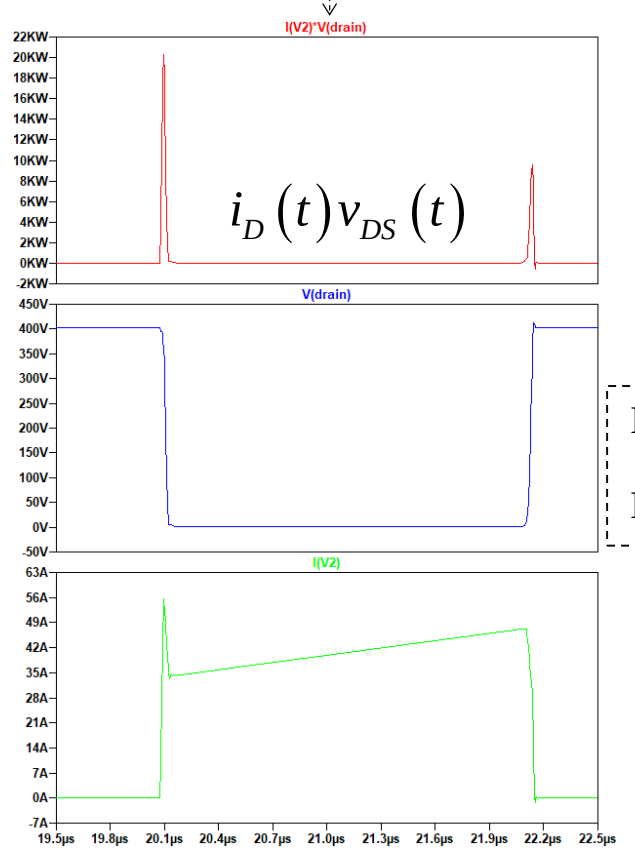


Always check your SPICE Models!

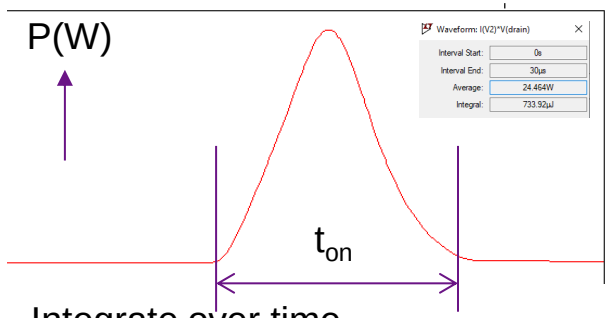
- An accurate model is necessary otherwise: garbage-in garbage out (GIGO)
- ✓ Implement a double-pulse test with the data-sheet conditions and check losses







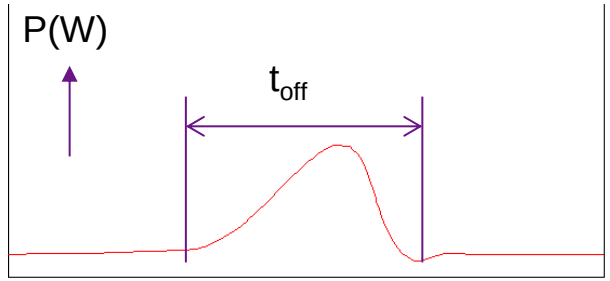
CTRL + left click on trace name



$$E_{on} = P_{avg}\big|_{\Delta t = t_{on}} t_{on}\ [J]$$

$$E_{off} = P_{avg}\big|_{\Delta t = t_{off}} t_{off}\ [J]$$

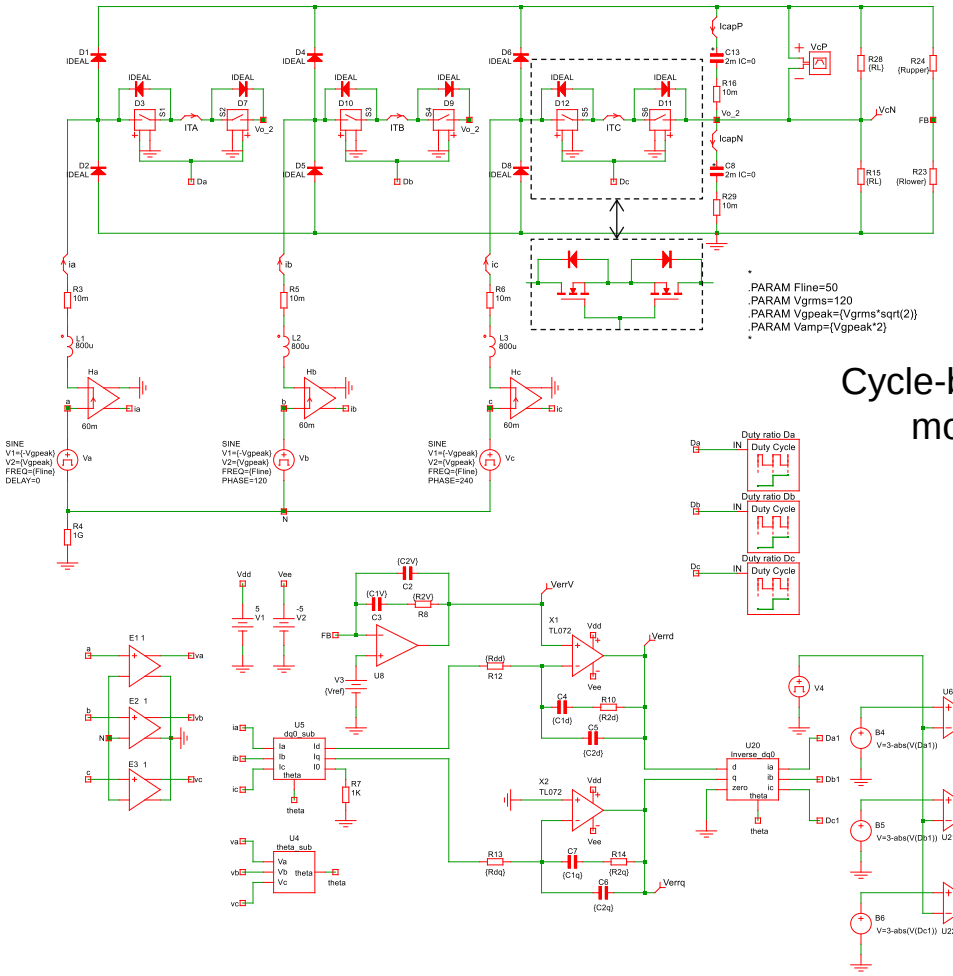
Check these losses!



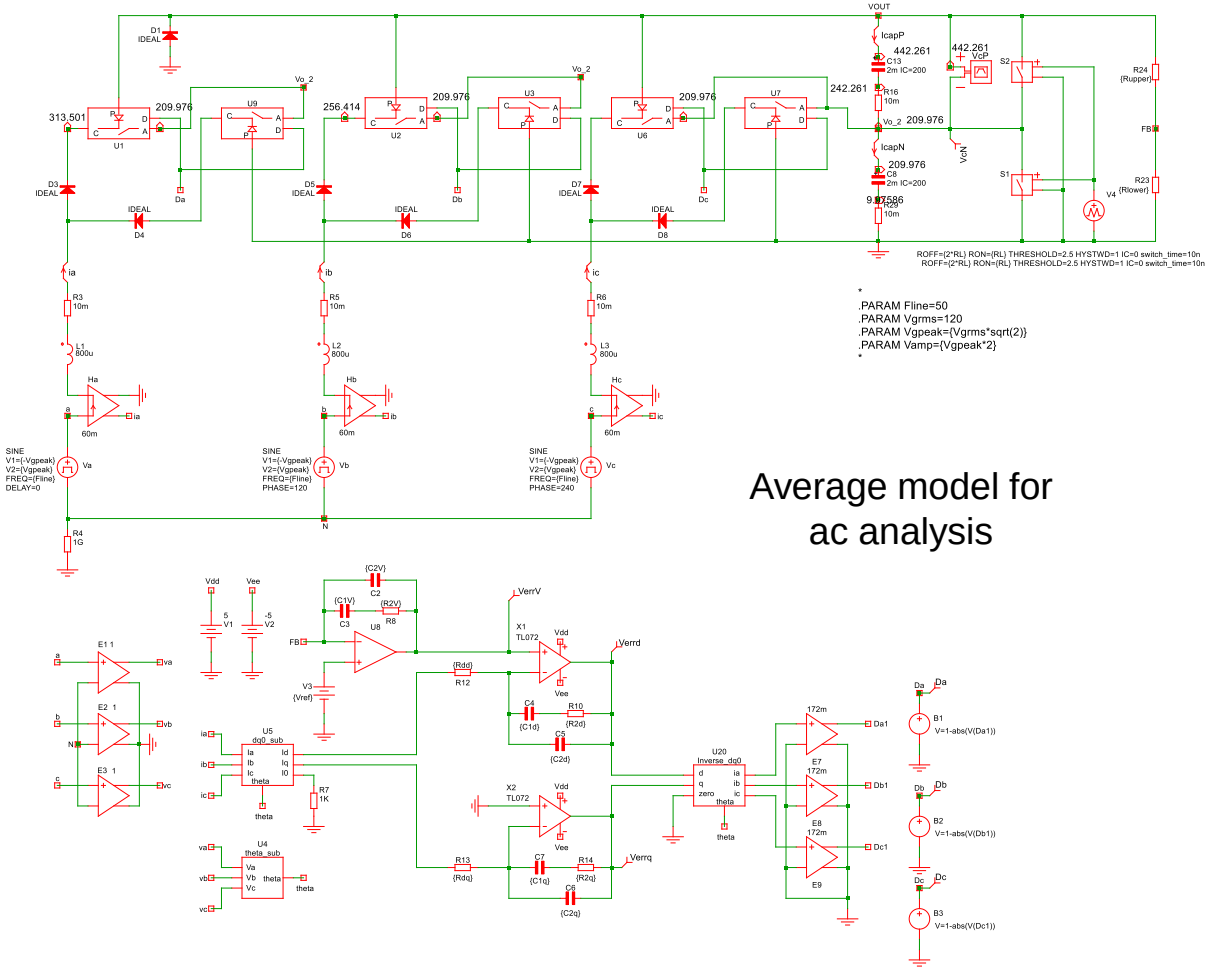
PWL(0 {VOFF} 10u {VOFF} 10.01u {VON} 15u {VON} 15.01u {VOFF} 20u {VOFF} 20.01u {VON} 22u {VON} 22.01u {VOFF})

Simulating a Vienna Rectifier

- The Vienna rectifier can be controlled using the dq0 blocks already available
- This 3-level converter requires two output capacitors, each biased at 400 V



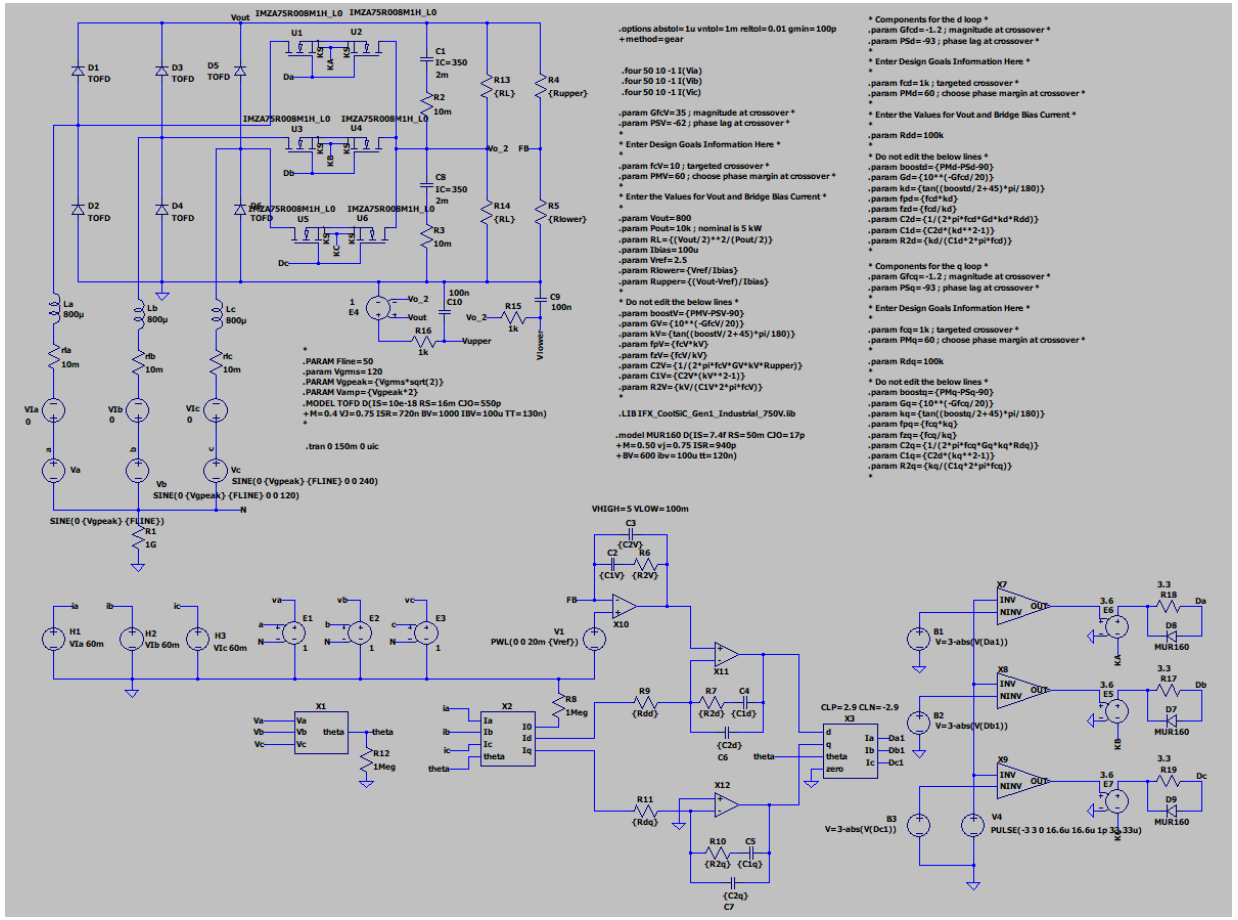
Cycle-by-cycle model

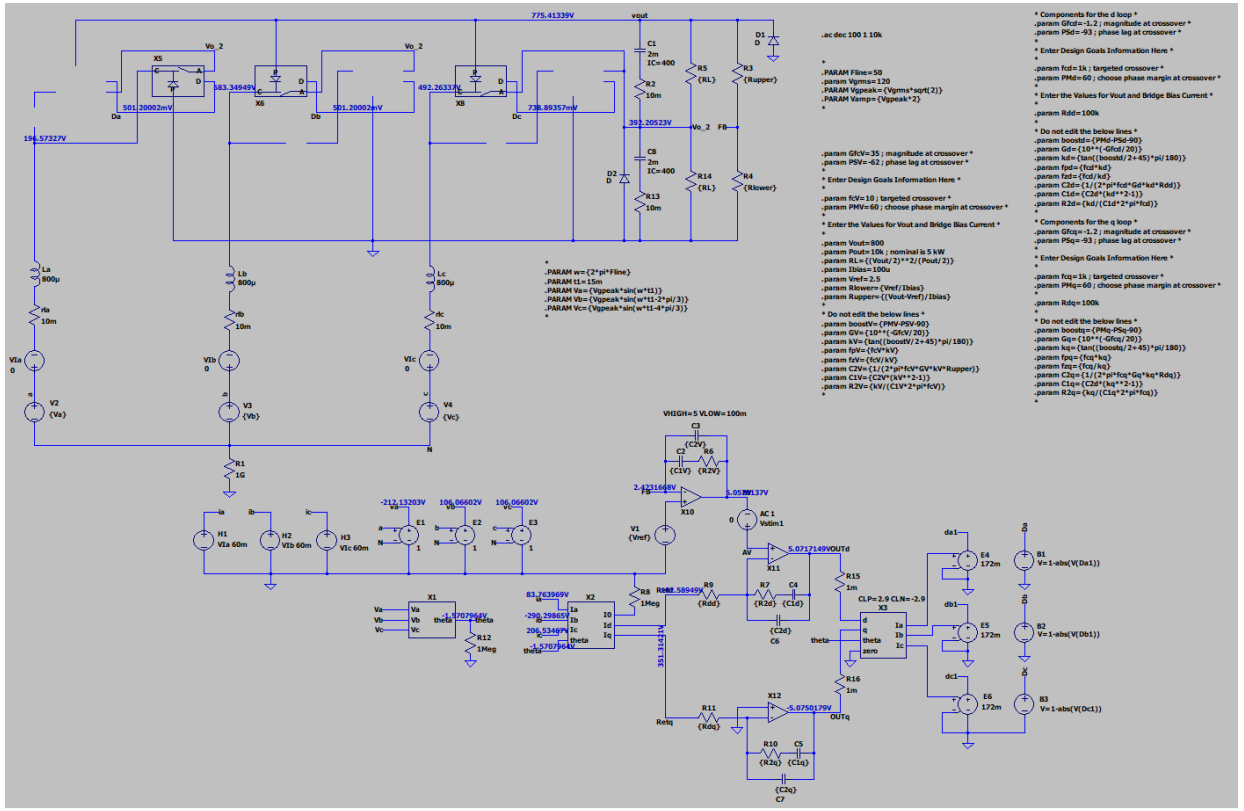


Average model for ac analysis

Vienna Rectifier with LTspice

- The same circuit can be reproduced in LTspice with averaged modeling too
- Transistors models can be inserted for a longer but more realistic simulation

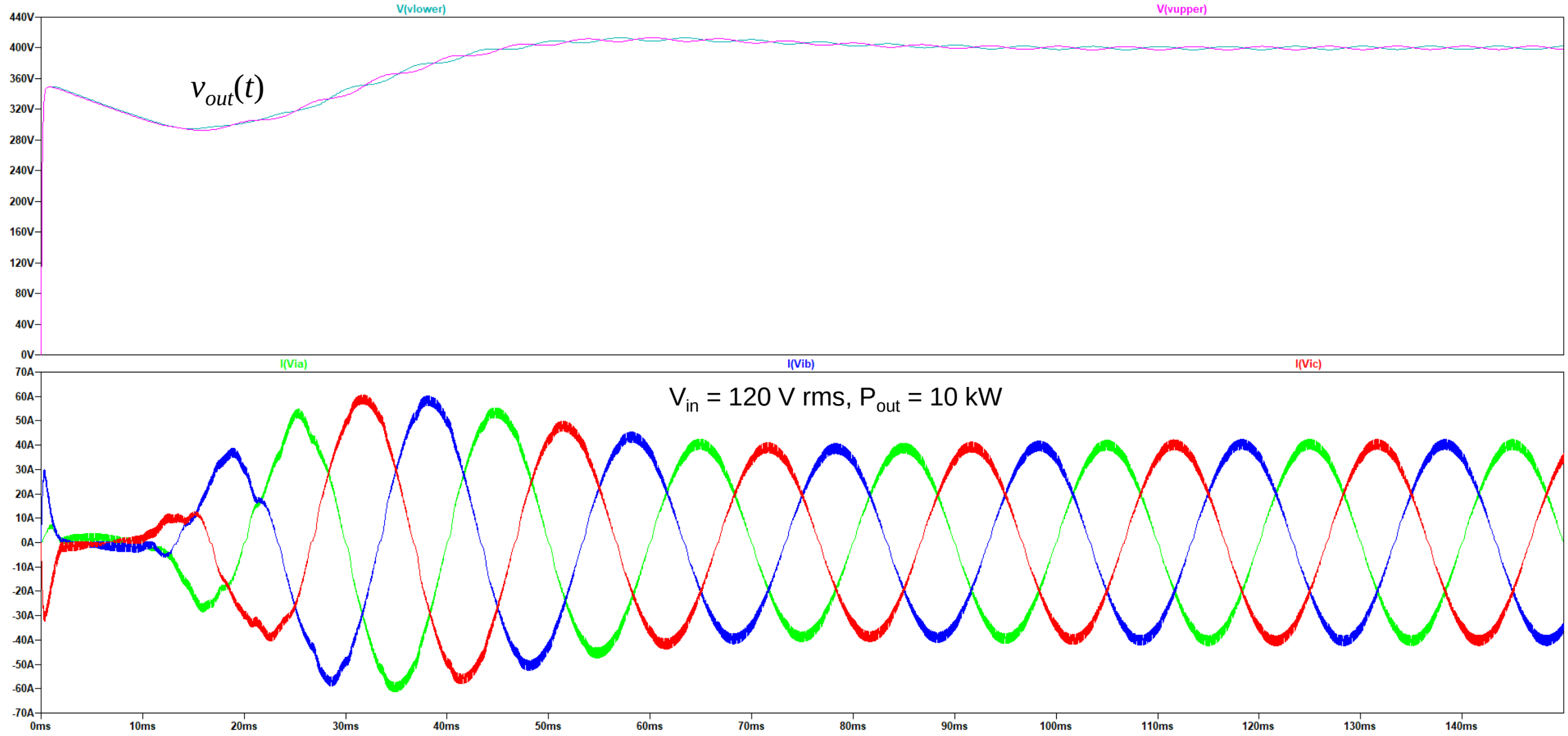




In the averaged model, some subcircuits are disabled depending on the input line polarity – always check the bias point is correct!

Simulation Results for a 10-kW Level

- The simulation is fast and the THD is 3.2% in this typical example

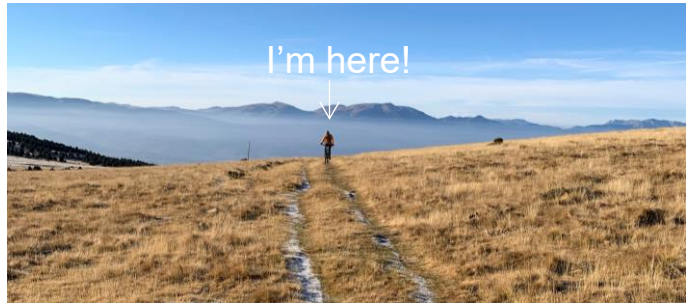


Conclusion

- Power Factor correction is a hot topic for several decades
- In single-phase applications, analog implementation is still possible
- Different techniques are available with or without input voltage sensing
- The totem-pole PFC gains traction owing to modern semiconductors like GaN and SiC
- Three-phase PFC is a complex matter, and I recommend to study rotating machines first
- ✓ Many terms and mathematical expressions come from this field
- Most of the 3-phase PFC projects I have seen deal with digital control
- Simulation helps a lot for assessing losses but also for conveniently closing the loop

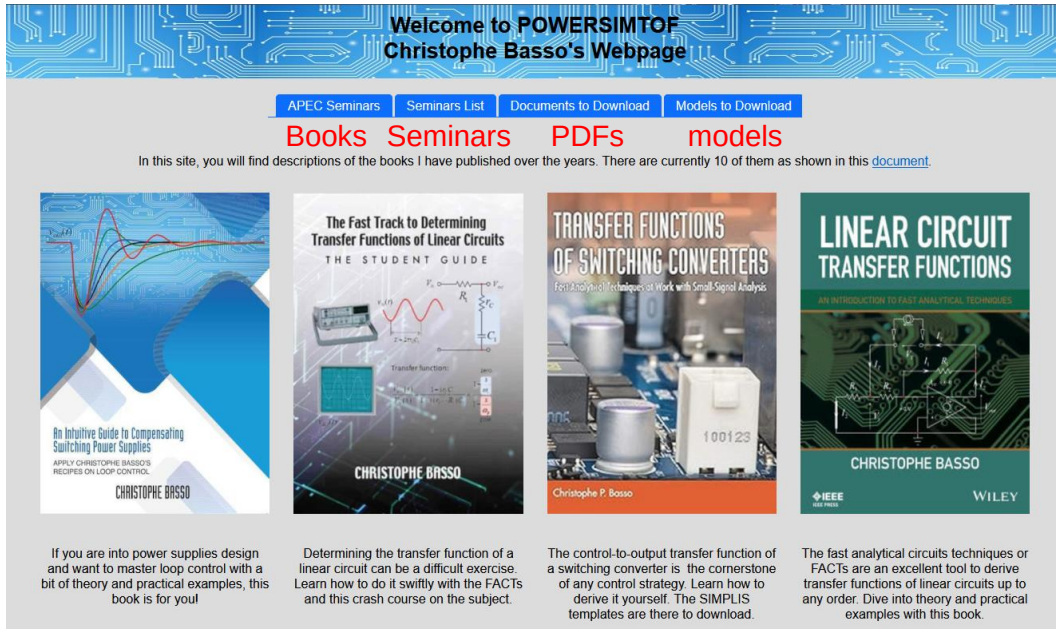
I'm done, merci, thank you
und danke vielmals!

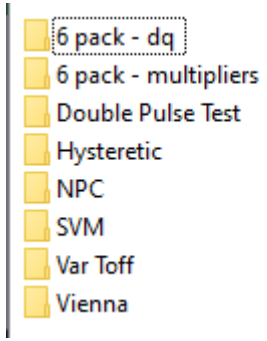
I don't care about PFCs when I cycle in the mountains!



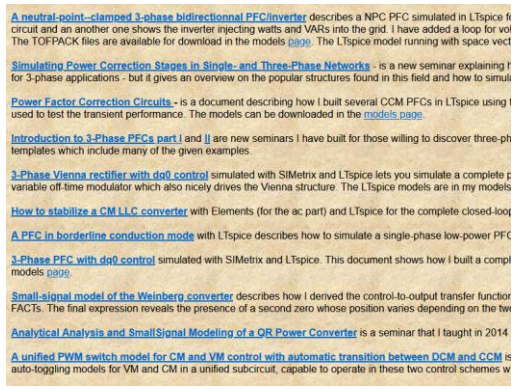
Where to download the Models?

- Christophe Basso's home page: www.powersimtof.com

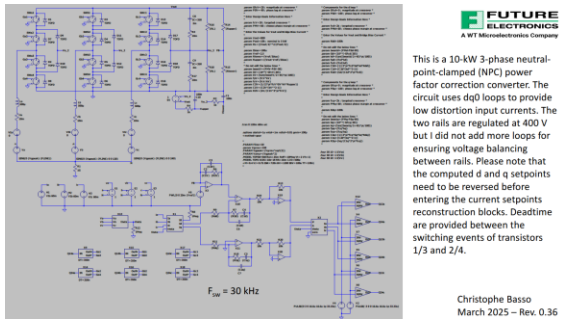




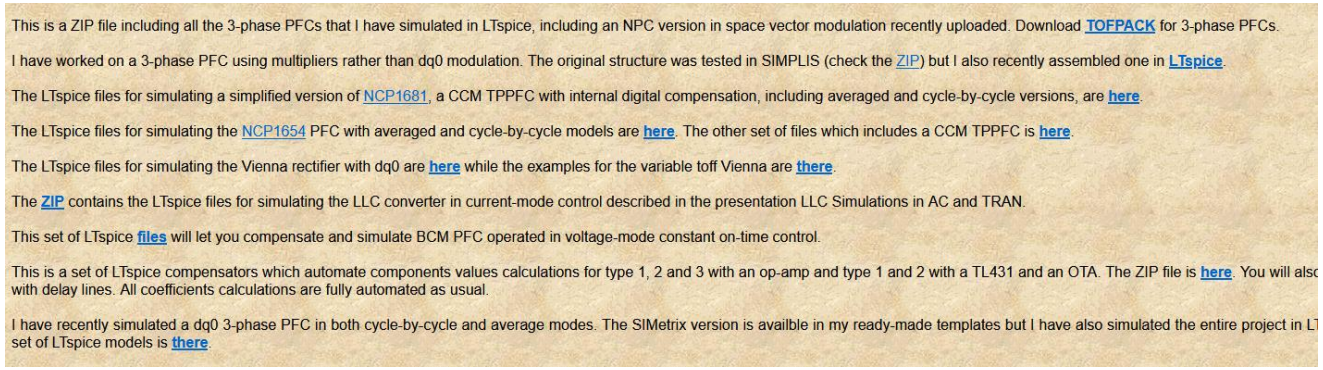
The TOFPACK PFC lets you download many 3-phase LTspice circuits ready to simulate.



Documents to download



A neutral-point--clamped 3-phase bidirectionnal PFC/inverter



Models to download