

A close-up photograph of a copper inductor on a green printed circuit board (PCB). The inductor is a toroidal coil with a green core. The background is blurred, showing other components on the board.

OMICRON Lab Webinar

Using WDS to Design:

- 1 - Analog Isolated Flyback**
- 2 - Digital Buck**

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Nov 2014

Forthcoming Workshops, Dates & Location

- Analog PSU Design Workshop
 - Dec 3rd to 5th and March 17th to 19th
 - Garching Germany
- Digital Power Workshop (Microchip dsPIC family)
 - Feb 10th to 12th 2015
 - Karlsruhe, Germany
- Digital PFC Workshop (TI C2000)
 - Feb 24th to 26th
 - Garching, Germany
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 - April 21st to 23rd 2015
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Abridged DPS Workshop Syllabus

- **Day 1: Starting with Embedded MCU Programming for Analog Engineers**
 - MCHP MCU 16 or TI C2000 family's development tools & features
 - Use Biricha Digital's libraries to run MCU code with minimal programming
 - Programming the MCU for digital power (Interrupts, Templates, PWMs etc)
 - Programming exercises and Labs (PWMs/ADCs/Interrupts etc)
- **Day 2: Voltage Mode PSU Design**
 - Step by step design of digital power supplies
 - Stable Analogue and digital power supply Design
 - Discrete time control theory, Z transforms & digital convolution
 - Avoiding stability issues in your digital power designs
 - Voltage mode PSU labs
- **Day 3: Digital Peak Current Mode**
 - Analogue current mode control
 - Digital peak current mode and slope compensation
 - Current mode PSU labs

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- **Day 2: Analog PFC Design**
 - Basic principles and foundations
 - Understanding EU regulations (EN-61000-3-2)
 - Stable analog voltage loop, current loop and voltage feed forward filter design
 - Using the PLD design software to design analog PFCs down to component level
 - Analog Labs

- **Day 3: Digital PFC**
 - Step-by-step block level digital PFC (single phase and interleaved)
 - Easy digital PFC implementation using Biricha's digital power libraries
 - Stable digital control loop design
 - Digital PFC labs (single phase and interleaved)

Abridged Analog PSU Design Workshop Syllabus

- Day 1: Introduction PSU Design, Control Theory, Test and Measurement
 - Fundamentals of power supply design
 - Frequency response analysis
 - Hands-on labs including:
 - Stable and robust voltage mode PSU design on a Forward type topology
 - Learning how to perform accurate loop measurement and stability analysis using a vector network analyser (each group will have their own network analyzer to use)
- Day 2: Peak Current Mode Control
 - Peak current design with state of the art modern ICs and controllers
 - Dealing with sub harmonic oscillations and slope compensation calculations
 - Hands-on labs including:
 - Designing a stable current mode power supply on Forward/Flyback topologies
 - Current mode controller transient response and loop measurement tests
- Day 3: Isolated Power Supply Design
 - Stable isolated PSU design and analysis
 - Designing with opto-couplers and programmable references (e.g. TL431)
 - Hands-on labs including:
 - Designing a stable opto-isolated power supply on Forward/Flyback topologies
 - Hands-on frequency response measurement of optoisolated compensators

Introduction to WDS

- WDS has been designed as the ultimate toolbox for the power supply design engineer.
 - Designs and stabilises analog and digital PSU control loops in minutes
 - Automatically calculates poles and zeros as well as component values of the worlds most popular topologies
 - Sophisticated control algorithms stabilise analog and digital power supplies
 - Automatic coefficient calculations for floating point, 32 bit and 16 bit processors
 - Automatic compensator design for isolated power supplies with TLx431/LMx431 and a host of industry standard optocouplers
 - Simulations in time domain, frequency domain and ability to superimpose real measurements on simulated data

Design Example Using WDS

Workshop_Vmode_Buck_UC3823.wds - WDS

File Calculations Help

Output Filter Controller Design Analog (Non-Isolated)

Specification Transformer Semiconductors

Converter Specification

Topology: Buck

Output voltage isolated from primary side: Non Isolated

Input Supply:

Maximum: 12 V
Nominal: 12 V
Minimum: 12 V

Output:

Maximum Current: 2 A
Voltage: 3.3 V

Output voltage ripple / overshoot:

Voltage Ripple (pk-pk): 0.5 %
Voltage Ripple (pk-pk): 16.5 mV
Load Step from 100% to: 50 %
Voltage Overshoot: 660 / 660 mV
Demand Efficiency: 85 / 85 %

Control Parameters

Control Mode: Voltage

Analog Control Digital Control

Switching Frequency: 200 kHz
Sampling Frequency: n/a kHz
Pure Time Delay: n/a x Tsamp
Crossover Frequency: 20 / 10 kHz
Phase Margin: 55 Degrees

Duty Cycle (per switch)

Maximum Duty Limit: 90 %
Minimum Duty Limit: 0 %
Maximum: 31.016 %
Nominal: 31.016 %

Frequency Response Circuit Power Loss Budget Summary Spice Simulation

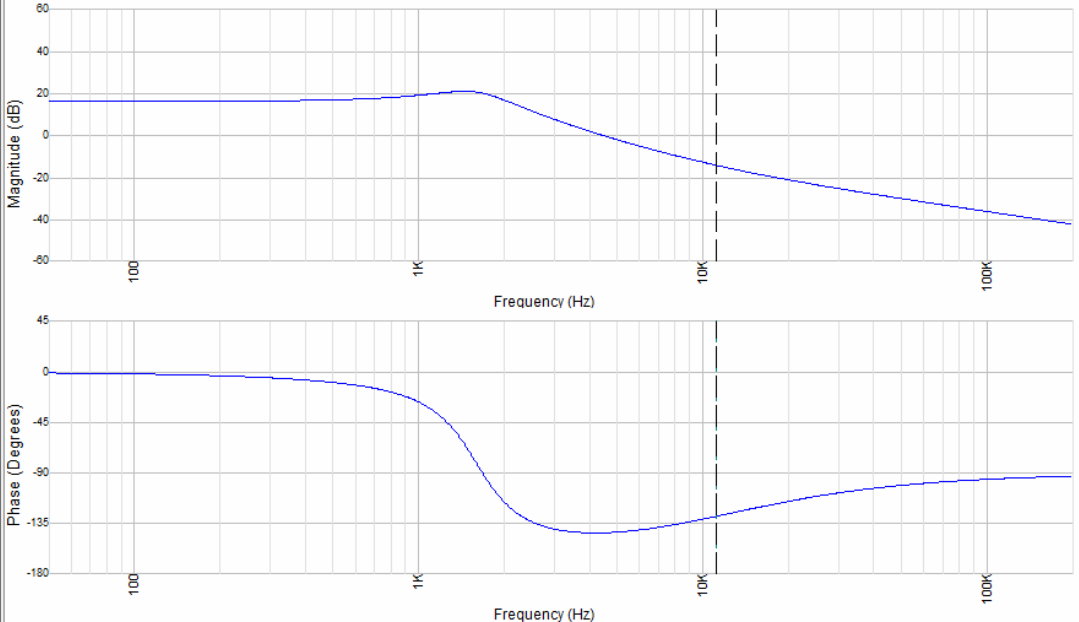
Bode Plot

Plant
 Comp
 Loop
 Measurement
Memory 1
 Spice

	Fx	P.m.	G.m.	Slope at Fx	RHPZ
Nominal	n/a	n/a	n/a	n/a	n/a
Measured	n/a	n/a	n/a	n/a	n/a

Stability Sweep (min/max)

Fx: 11.16 / 11.16kHz Slope at Fx: -23.1 / -23.1dB/dec
P.m.: 60 / 60° RHPZ: n/a
G.m.: 33 / 33dB



NEW: Analog and Digital Power Factor Correction Workshop - July 15th 2014
Find out more: <http://www.biricha.com/pfc>

For Help, press F1 NUM Power Loss Budget: 1.0 W used of 1.0 W allowed

Design Example Using WDS

Converter Specification

Topology:

Output voltage isolated from primary side:

Input Supply:

Maximum V

Nominal V

Minimum V

Output:

Maximum Current A

Voltage V

Output voltage ripple / overshoot:

Voltage Ripple (pk-pk) %

Voltage Ripple (pk-pk) mV

Load Step from 100% to %

Voltage Overshoot mV

Demand Efficiency %

Control Parameters

Control Mode:

Analog Control Digital Control

Switching Frequency kHz

Sampling Frequency kHz

Pure Time Delay x Tsamp

Crossover Frequency kHz

Phase Margin Degrees

Design Example Using WDS

Primary Switch			
"On" Resistance	<	<input type="text" value="31.625"/>	<input type="text" value="4.8"/> mΩ
Rise Time	<	<input type="text" value="25"/>	<input type="text" value="25"/> ns
Fall Time	<	<input type="text" value="5"/>	<input type="text" value="25"/> ns
Parasitic Cap (Coss)	<	<input type="text" value="1285.495"/>	<input type="text" value="580"/> pF
Peak Switch Voltage		<input type="text" value="12.4"/>	V
Average Switch Current		<input type="text" value="0.62"/>	A
RMS Switch Current		<input type="text" value="1.118"/>	A
Peak Switch Current		<input type="text" value="2.301"/>	A
Conduction Losses		<input type="text" value="0.006"/>	W
Switching Losses		<input type="text" value="0.147"/>	W
Recommended values for calculations			

Diode/Switch			
Forward Voltage Drop	<input type="text" value="0.6"/>	<input type="text" value="0.4"/>	V
Peak Voltage Stress	<input type="text" value="11.989"/>		V
Average Current	<input type="text" value="1.38"/>		A
RMS Current	<input type="text" value="1.667"/>		A
Peak Current	<input type="text" value="2.301"/>		A
Conduction Losses	<input type="text" value="0.552"/>		W
Recommended values for calculations			

Design Example Using WDS

Output Filter Inductor

Specified Ripple (pk-pk)		25	%
Specified Ripple (pk-pk)	0.5		A
L0 Inductance	26.52	22	μ H
L0 DCR		70	m Ω
Actual % Ripple (pk-pk)	30.1		%
Actual Ripple (pk-pk)	0.603		A
Peak Current	2.301		A
Average Current	2		A
Power Dissipation	0.28		W
DCM/CCM Boundary	0.301022		A

Recommended values for calculations

Output Filter Capacitor

C0 Capacitance	500.277	440	μ F
C0 ESR	26.905	34	m Ω
C0 ESR Zero	10638.699		Hz
Specified Overshoot	660		mV
Actual Overshoot	49.643		mV
Specified Ripple (pk-pk)	16.5		mV
Actual Ripple (pk-pk)	20.107		mV
RMS Current	0.17		A
Ripple Current (pk-pk)	0.591		A
Peak Voltage	3.32		V
Power Dissipation	0.988		mW

Recommended values for calculations

Calculated capacitance is based on the voltage ripple requirement to meet both overshoot and voltage ripple specifications.

Design Example Using WDS

Controller Type

Type III

$$H_C(s) = \frac{\omega_{CP0}}{s} \times \frac{(s + \omega_{CZ1})(s + \omega_{CZ2})}{(s + \omega_{CP1})(s + \omega_{CP2})}$$

PWM Parameters

PWM Ramp Height: 1.8 V

Controller Poles and Zeros

Automatic placement Manual placement

Pole at the origin	3979.289	3979.289	Hz
First Pole	10638.699	10638.699	Hz
Second Pole	100000	100000	Hz
First Zero	4860.243	4860.243	Hz
Second Zero	1601.229	1601.229	Hz

Error Amplifier

Reference Voltage: 2.55 V

Sampling Divider

Desired current through divider: 0.15 mA

R1: 5 kΩ 10 kΩ

Rb: 34 kΩ

Actual current through pd: 0.075 mA

Controller Component Values

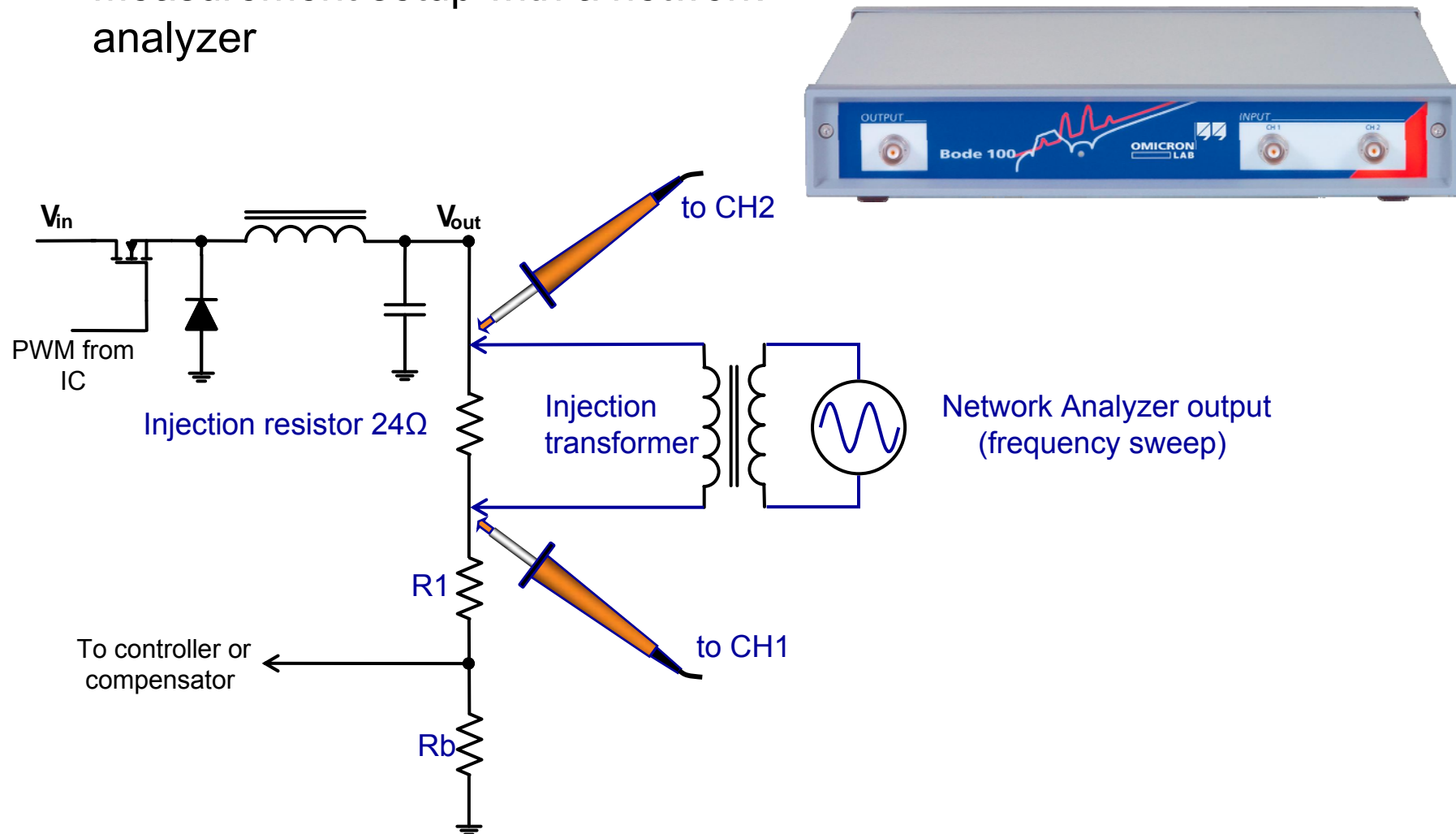
R2	15.074	14	kΩ
R3	0.163	0.18	kΩ
C1	2.172	2.2	nF
C2	9.78	10	nF
C3	1.827	1.5	nF

Actual Controller Poles and Zeros

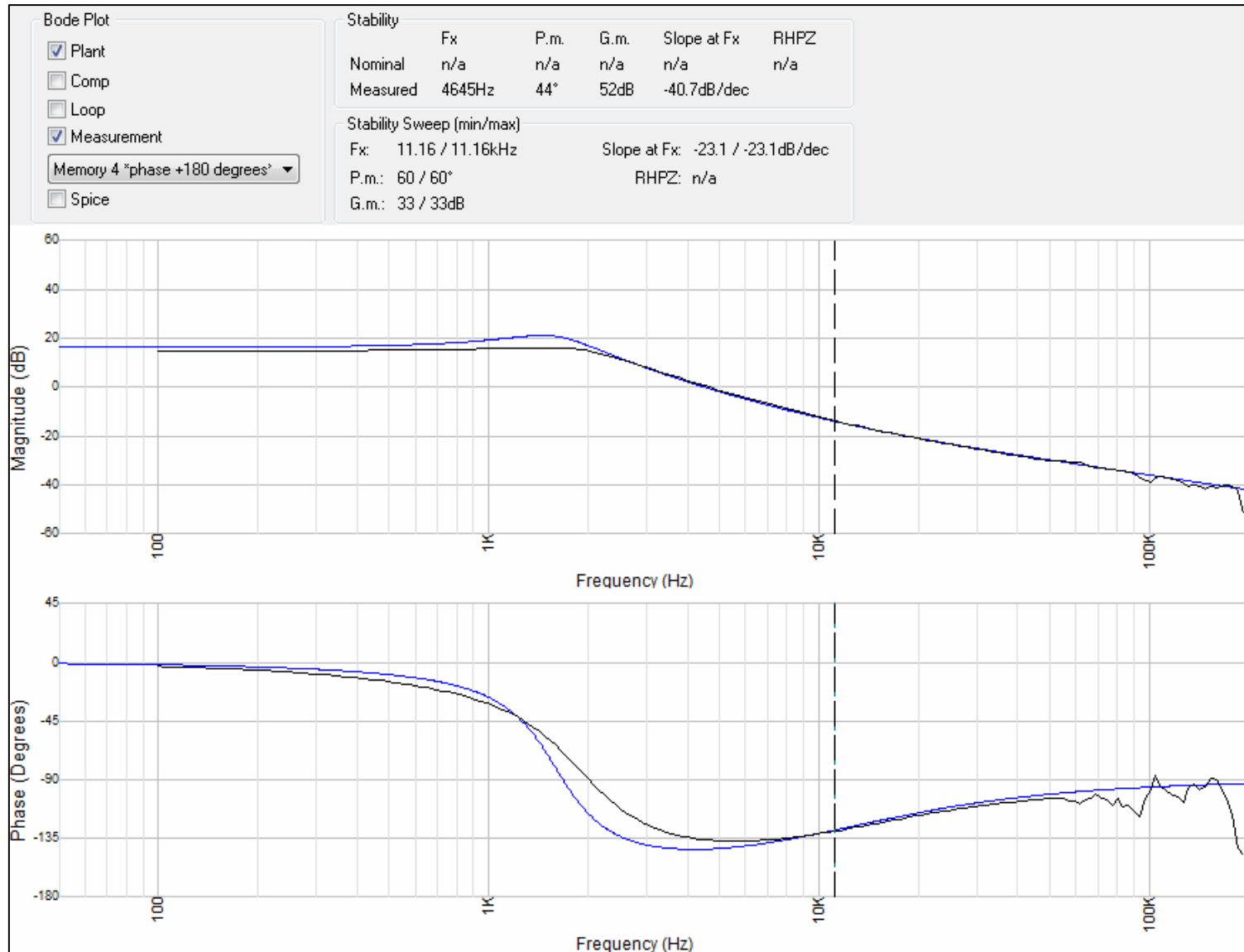
Pole at the origin	4301.485	Hz
First Pole	12746.175	Hz
Second Pole	88419.413	Hz
First Zero	5167.368	Hz
Second Zero	1563.408	Hz

Analyzing Your Converter in Frequency Domain

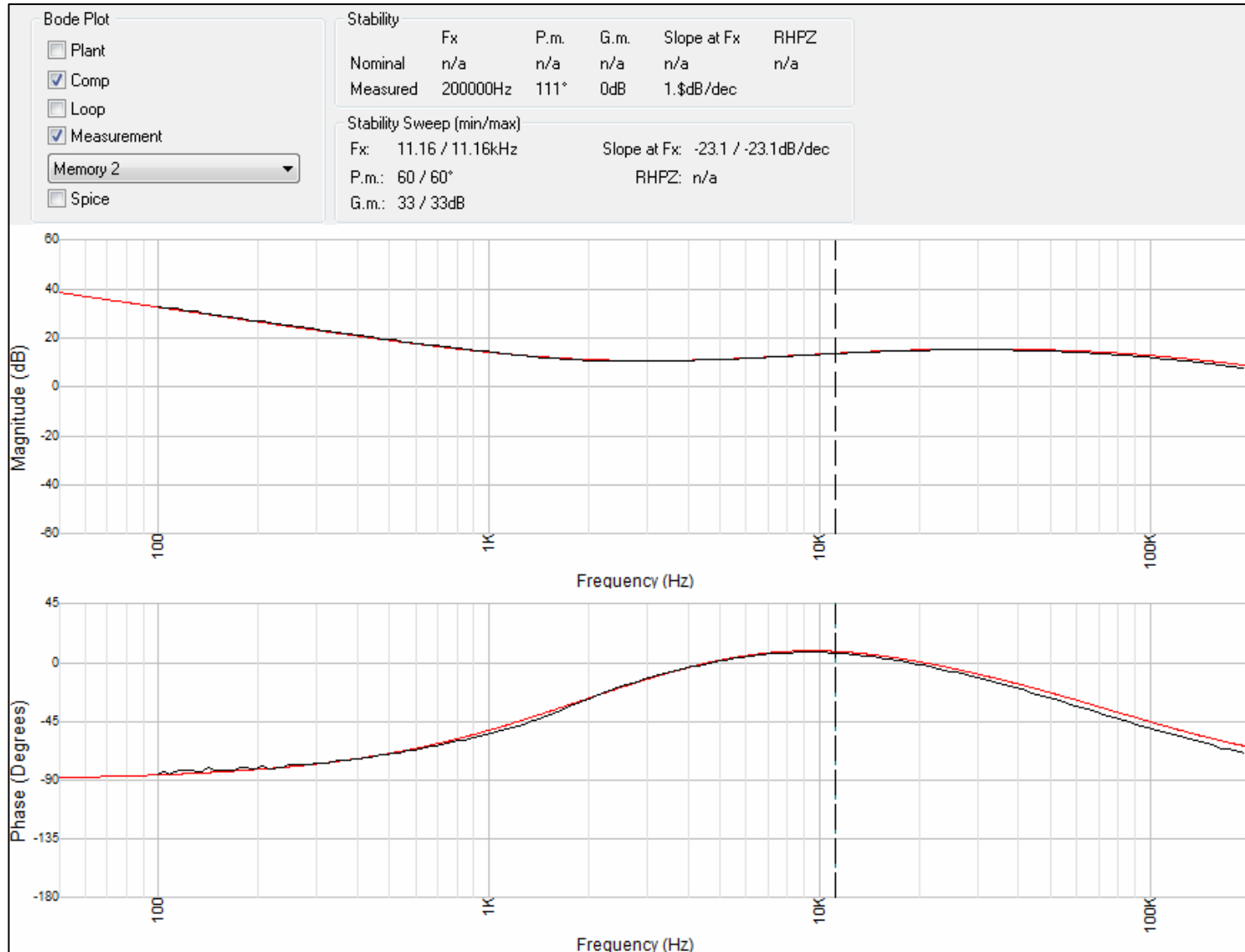
- Measurement setup with a network analyzer



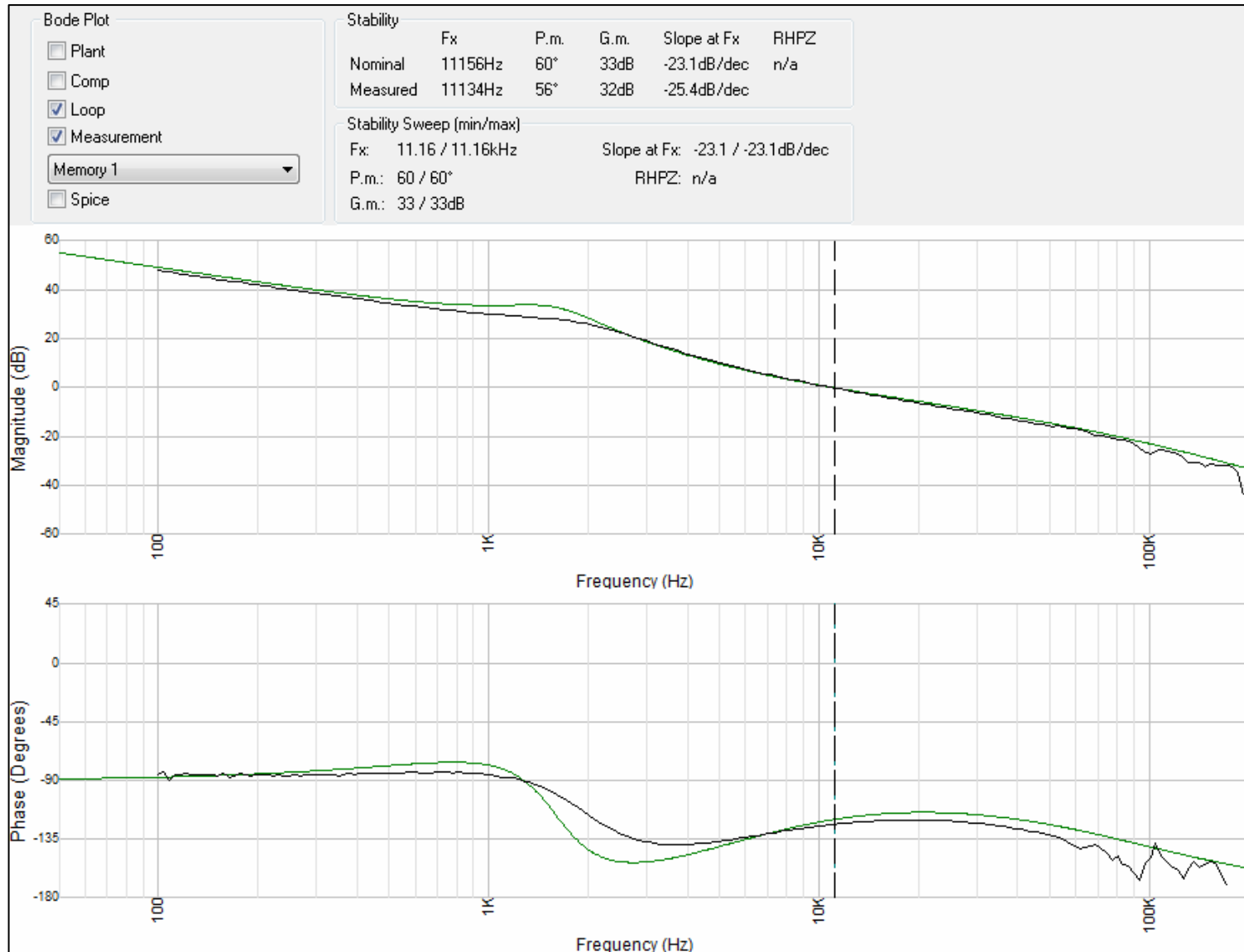
Results from Exercise 1c



Results from Exercise 1c

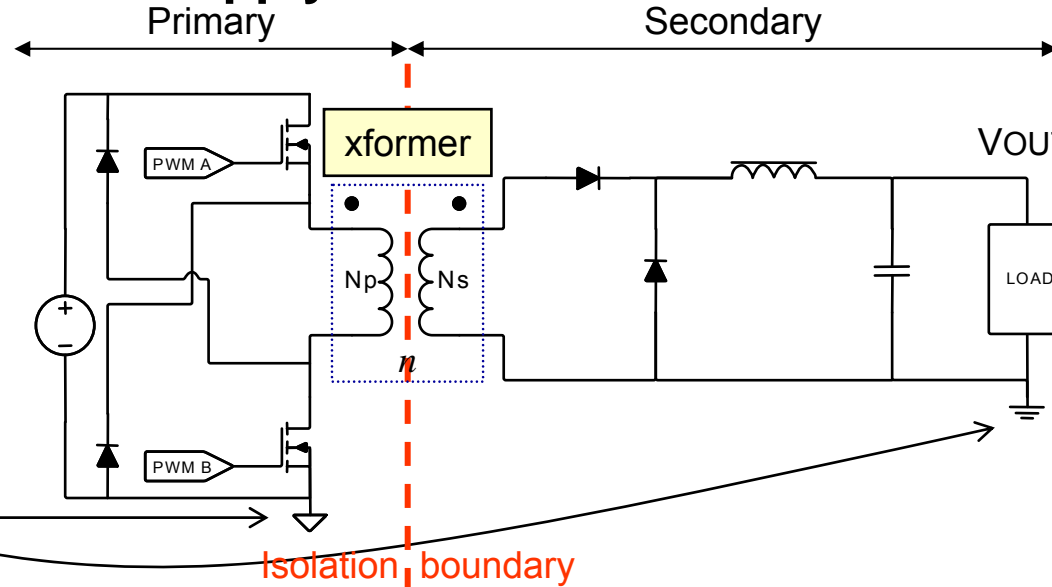


Results from Exercise 1c



- Live Design Demo
 - 1 - Isolated Peak Current Mode Flyback
 - 2 – Digital Buck Converter

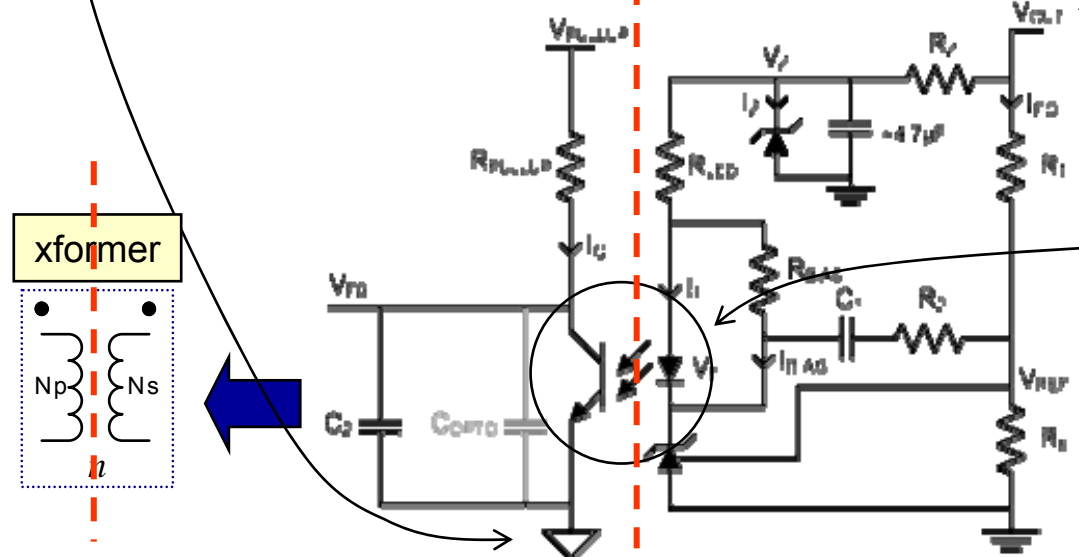
Typical Isolated Power Supply



Note different grounds

We need to measure VOUT on the secondary and feed back across the isolation barrier to the controller IC

We do this using the optocoupler



Real Life Design Example 1: Common Emitter with RPULLUP = 2.2kΩ

Controller Type

Type II

$$H_C(s) = \frac{\omega_{CP0}}{s} \times \frac{(s + \omega_{CZ1})}{(s + \omega_{CP1})}$$

PWM Parameters

PWM Ramp Height: n/a V

Current Sense and Slope Compensation

Current Sense Gain <: 0.399, 0.16 V/A

Magnetizing "Free" Ramp: 0 V(pk-pk)

Optimal External Ramp: 0.272 V(pk-pk)

Amount of Ramp to Add: 0.272, 0.6 V(pk-pk)

V. on Current Sense Pin: 1.001 V

Controller Poles and Zeros

Automatic placement Manual placement

Pole at the origin: 2695.138, 2695.138 Hz

First Pole: 10334.737, 10334.737 Hz

Second Pole: n/a, n/a Hz

First Zero: 1056.177, 1056.177 Hz

Second Zero: n/a, n/a Hz

Optocoupler

Isolation Configuration: CNY17-3 *user edited*

[Let Biricha characterize your opto](#)

Max. CTR: 180 %

Typ. CTR: 125 %

Min. CTR: 100 %

Vpullup (Primary): 8 V

Vce(sat) (Primary): 0.25 V

Copto (Primary): 2.8 nF

Desired Ic Max. (Primary): 8 mA

Rpullup (Primary): 0.969, 2.2 kΩ

Actual Ic Max. (Primary): 3.523 mA

Calculated If (Secondary): 2.818 mA

Vf (Secondary): 1.39 V

Zener Reference

Vz <=: 5.6 V

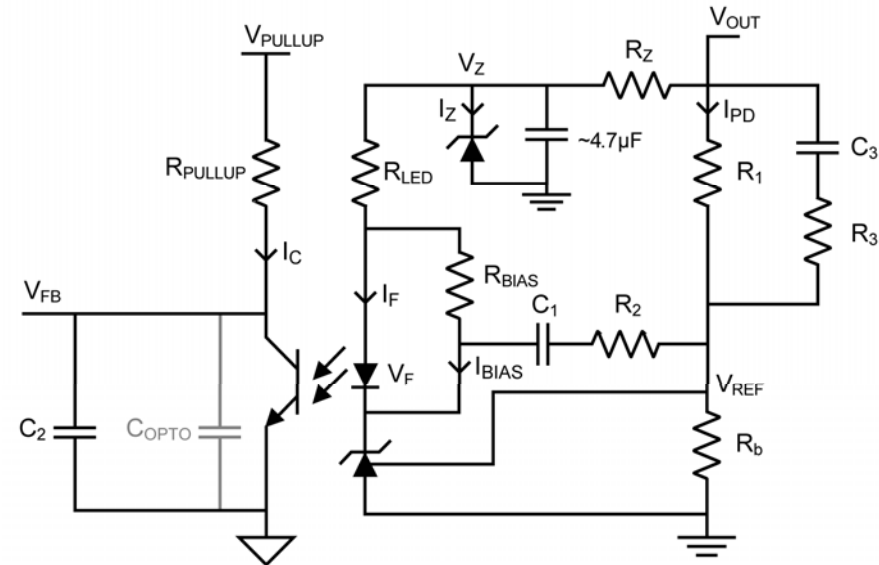
Desired Iz: 2.5 mA

Rz <=: 0.344, 0.33 kΩ

Actual Iz: 2.735 mA

Real Life Design Example 1

Controller Component Values			
Rled (max)	0.984		kΩ
Rled (recommended)	0.738	0.68	kΩ
R2	15.144	15	kΩ
R3	n/a	n/a	kΩ
C1	9.951	10	nF
C2	4.2	4.7	nF
C3	n/a	n/a	nF

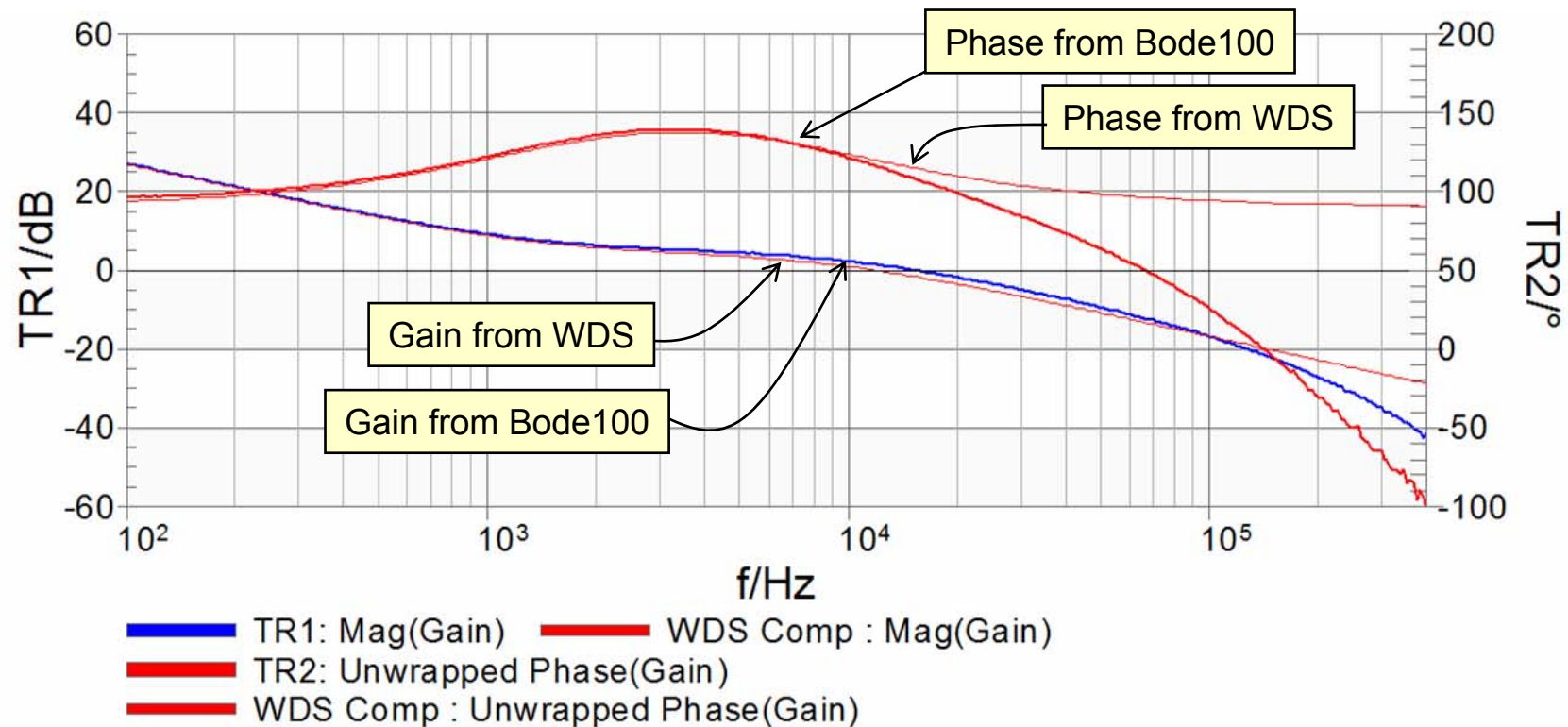


- Now that we have got our component values we can test *the compensator* to make sure that:
 - Our programmable reference is stable
 - Compensator poles and zeros are where we think they are
 - Opto bandwidth is not messing up our loop
 - Opto is being operated in the linear region

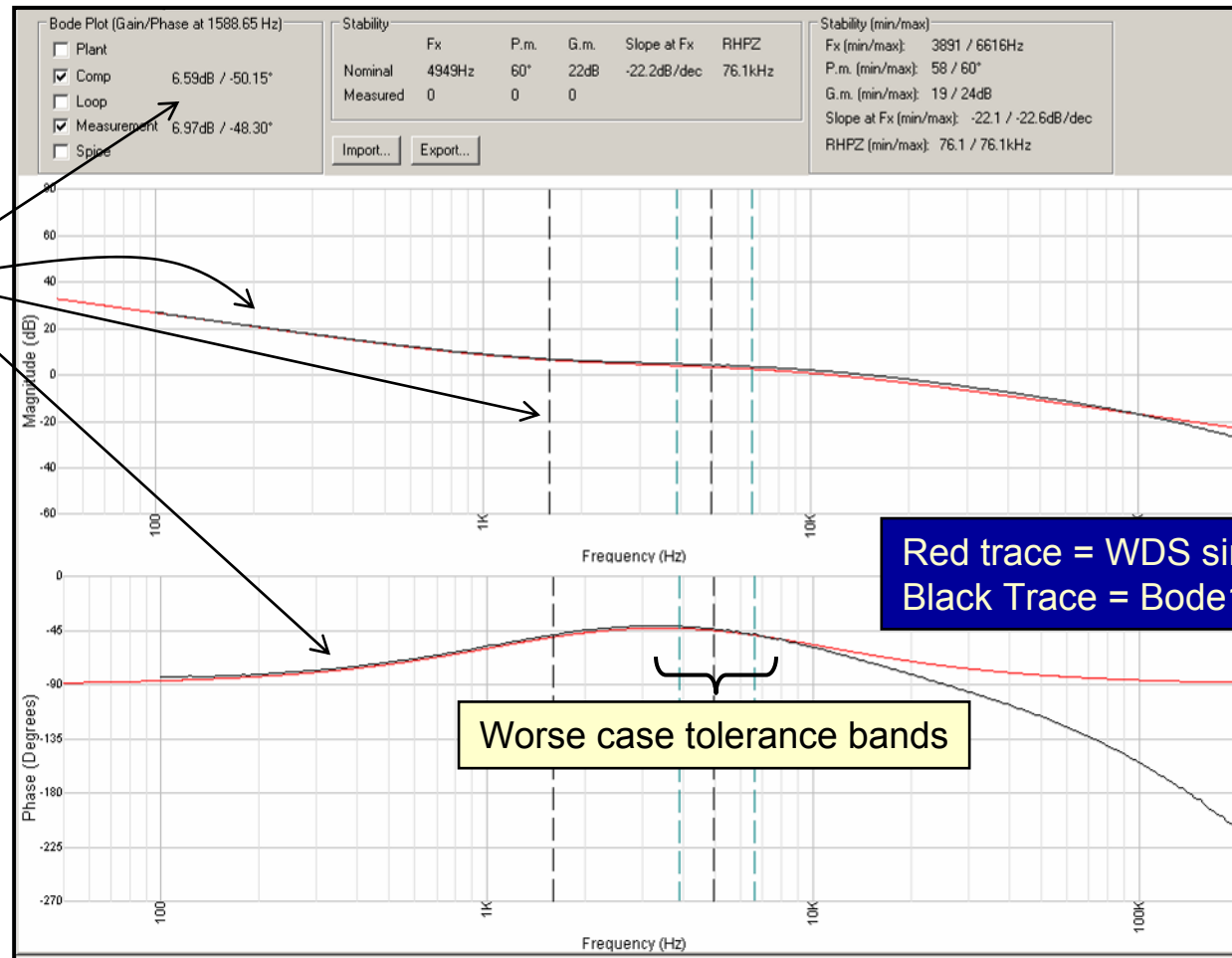
We can now run a lab to make sure the compensator works perfectly before moving on to our real power supply

Exercise 3b: Isolated Compensator Design Using WDS

- Exported simulation into Bode Analyser Suite is almost a perfect match
 - This is a stable compensator with poles and zeros at correct locations



Exercise 3b: Isolated Compensator Design Using WDS

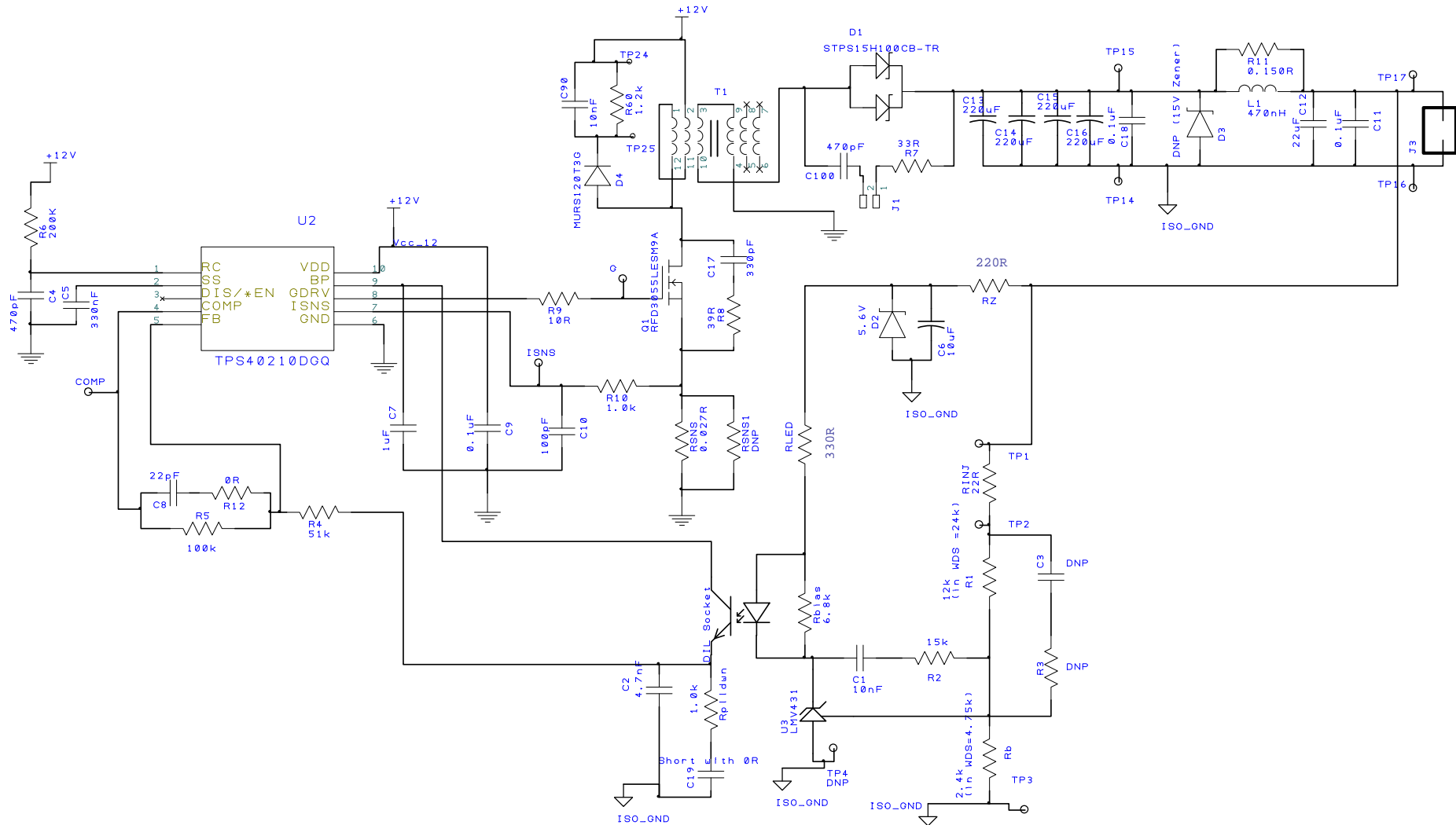


Almost a perfect match!
Red = WDS
Black = Bode100

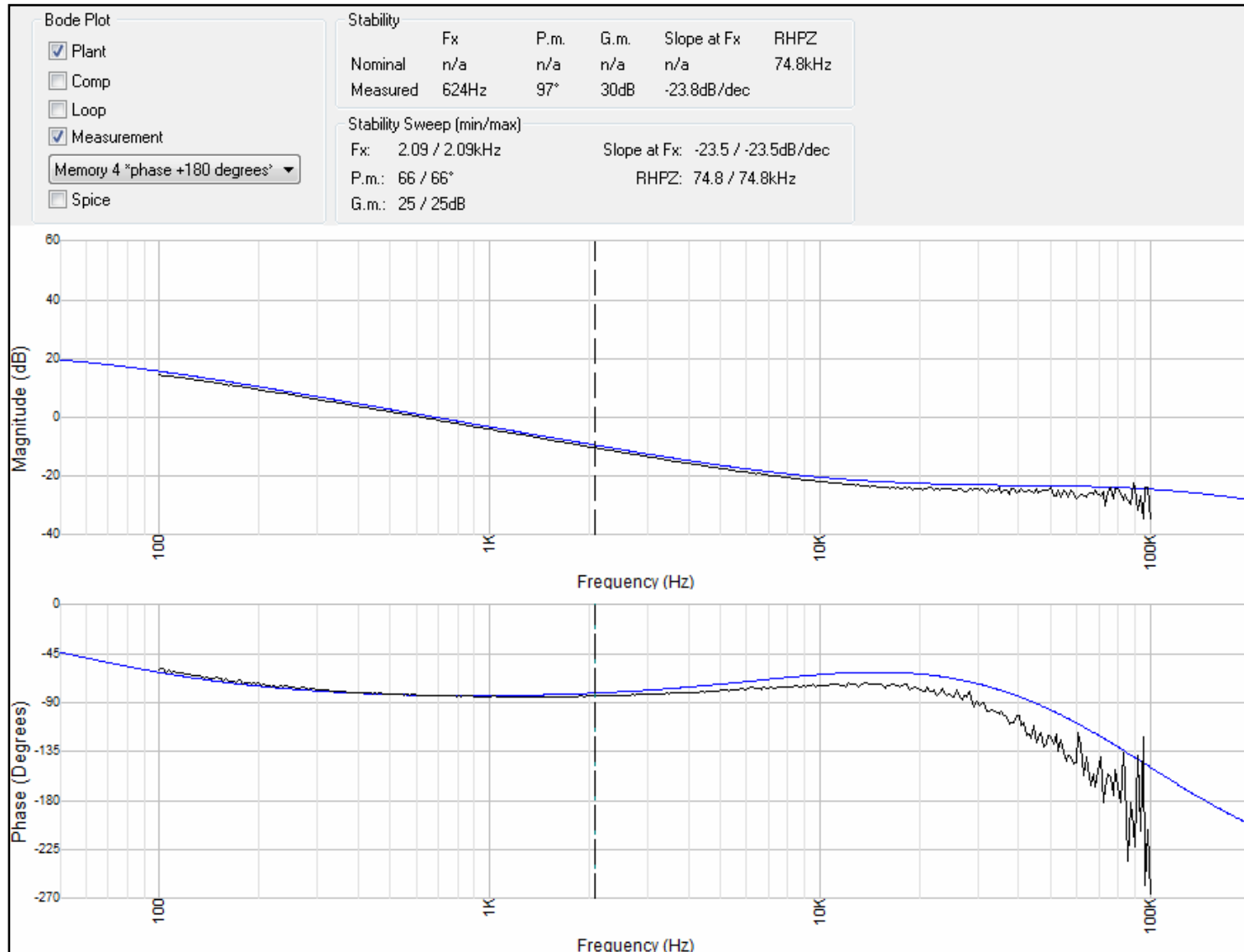
Red trace = WDS simulation
Black Trace = Bode100

Worse case tolerance bands

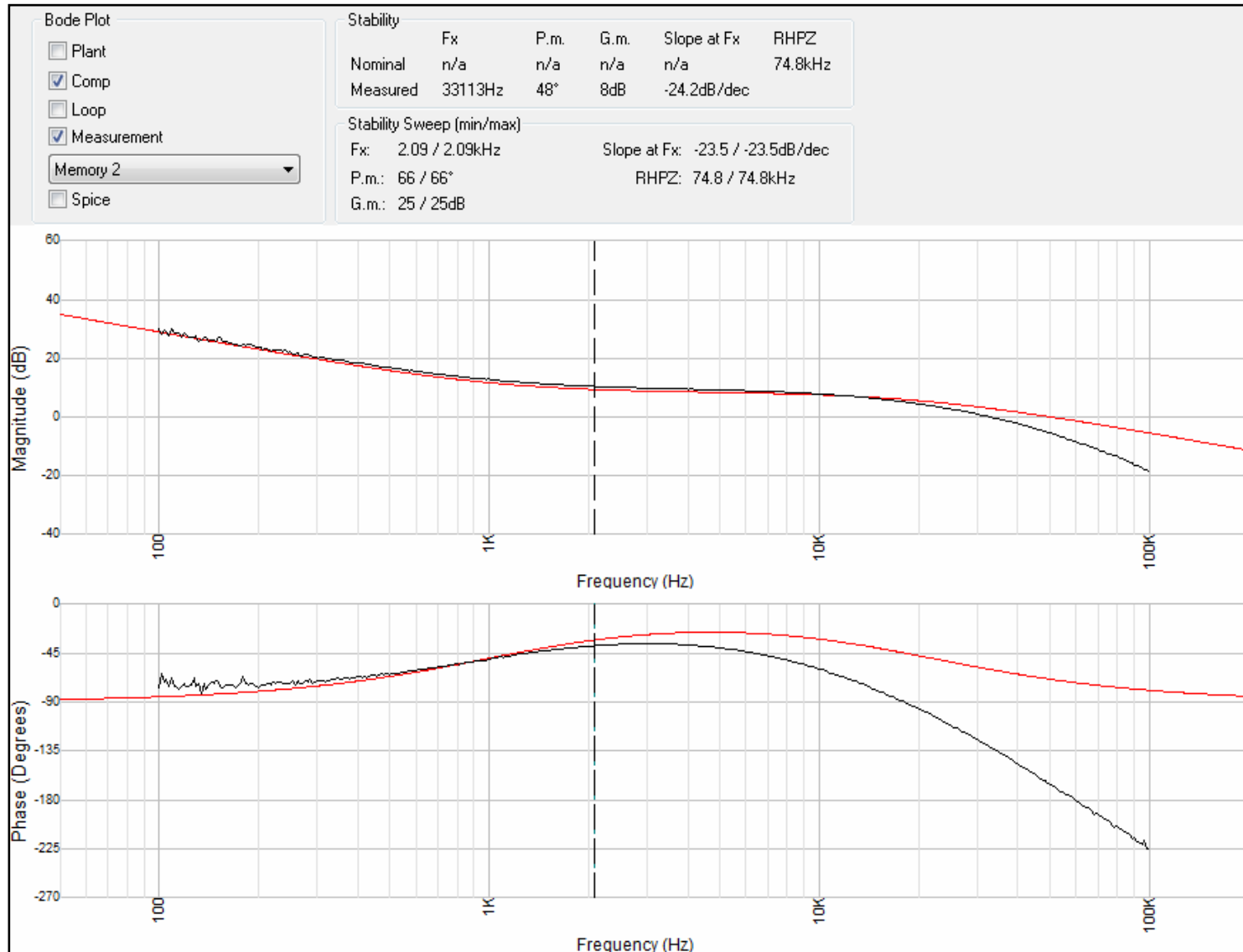
Real Life Design Example: BDP-206



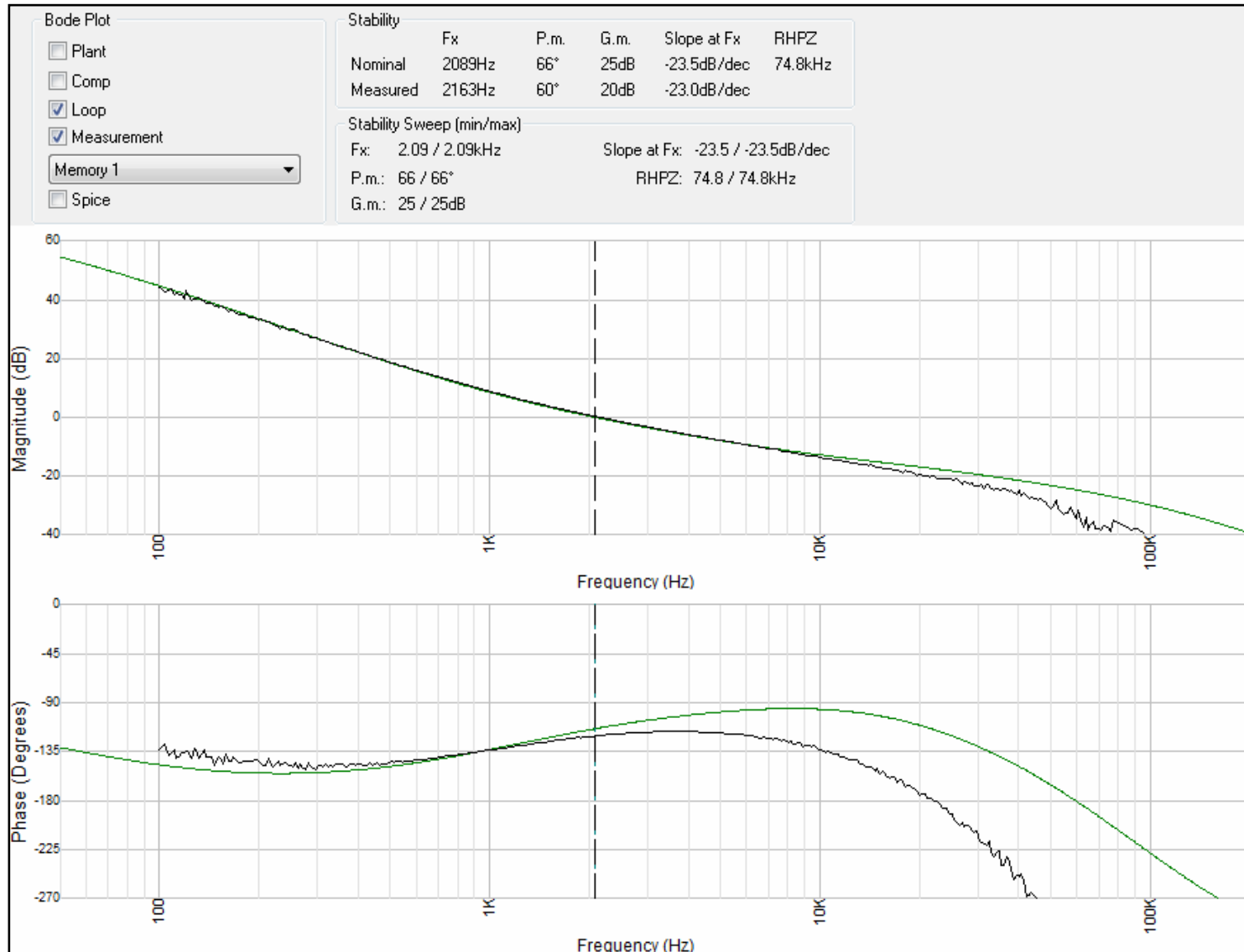
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 - Hands-on frequency response measurement of optoisolated compensators

***End of the workshop
Thank you for taking part***

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