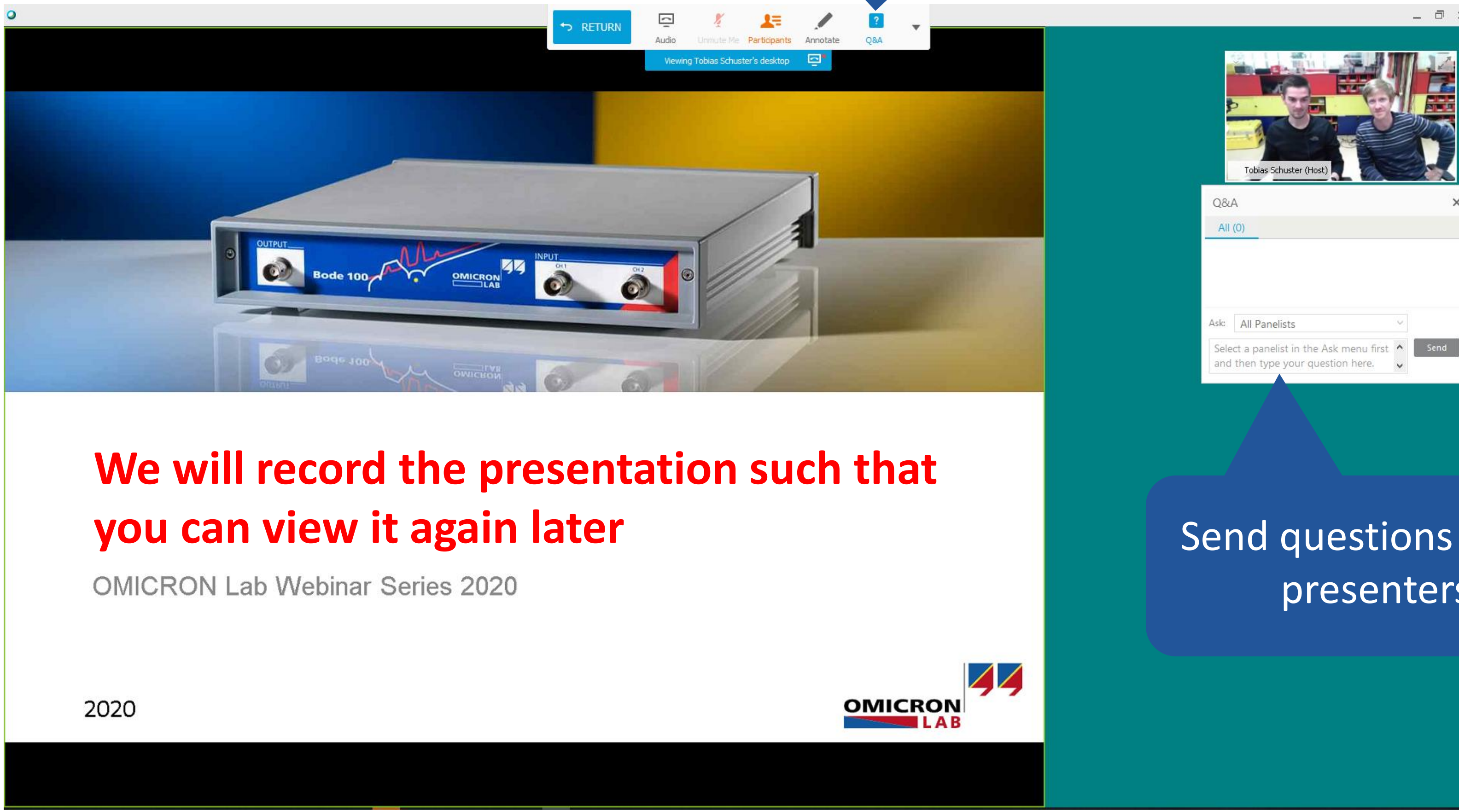
Output Impedance

OMICRON Lab Webinar Series 2020

2020-04-29

Webinar Hints

Open the Q&A function



Send questions to the presenters

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- Working at OMICRON Lab since 2010 in:
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Agenda

- DC voltage source (ideal vs. real)
- Output Impedance of VRM
- NISM (Non-Invasive Stability Measurement)
- From the power to the load
- Measuring Output Impedance
- Examples

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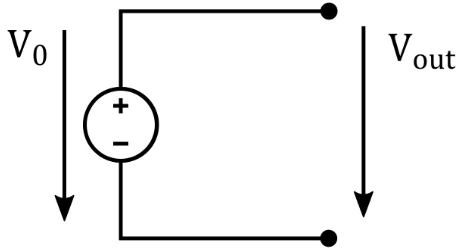
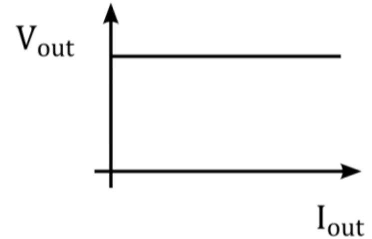
DC Voltage Source

Two-terminal device that can maintain a fixed DC voltage.

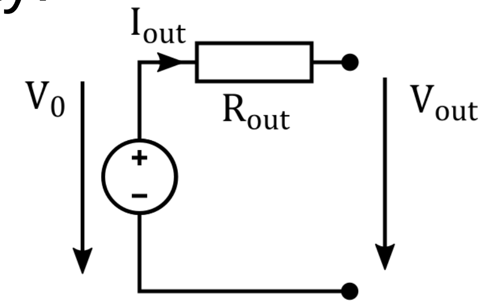
Ideally:



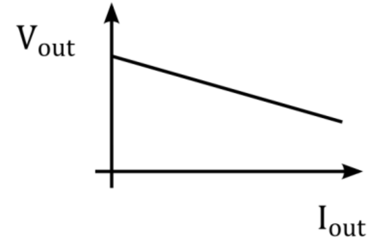
$$R_{out} = 0 \;\rightarrow\; V_{out} = V_0$$



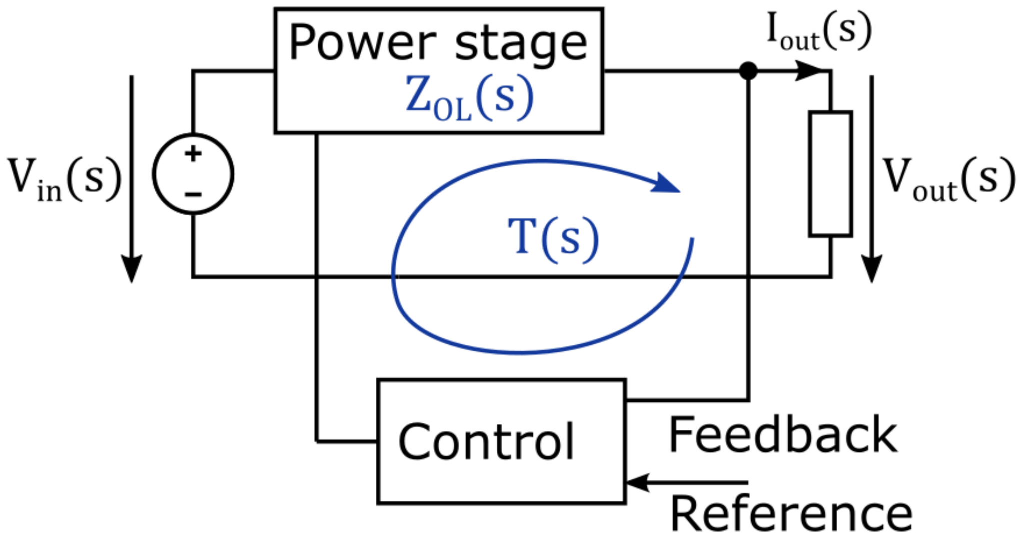
In reality:



$$R_{out} \neq 0 \;\rightarrow\; V_{out} = V_0 - I_{out} R_{out}$$



Stabilizing Output via Voltage Feedback



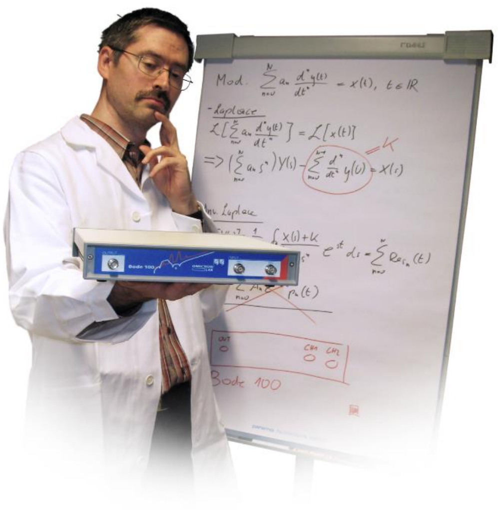
- Closing the loop changes the output impedance to:

$$Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)}$$

$T(s)$...Loop Gain
$Z_{OL}(s)$...Open-Loop Output Impedance
$Z_{out}(s)$...Closed-Loop Output Impedance

Closed-Loop Output Impedance

$$Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)}$$



- If $T(s) \gg 1$ then $Z_{out}(s) \ll Z_{OL}(s)$
- If $T(s) \ll 1$ then $Z_{out}(s) = Z_{OL}(s)$
- If $T(s) = 1$ then $Z_{out}(s) = ½\, Z_{OL}(s)$

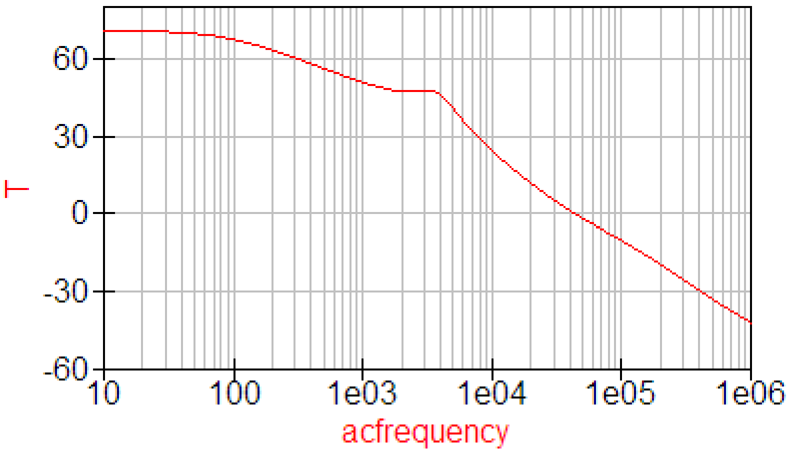
➢ High loop gain results in low output impedance

Loop Gain

- Loop Gain at DC is not ∞ → $R_{out} \neq 0$
- Control loop is not infinitely fast → Loop Gain reduces with f
- Loop Gain crosses 0 dB line at some crossover frequency f_c

➢ Control loop affects Z_{out} mainly below f_c

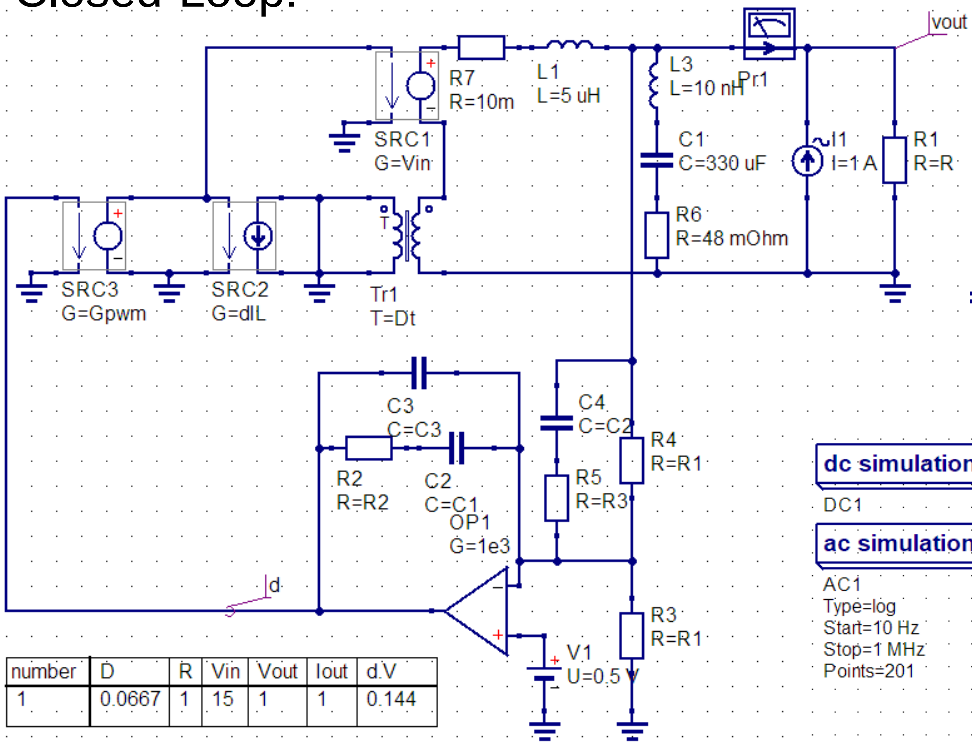
➢ Above f_c the feedback has nearly no effect: $Z_{out}(s) = Z_{OL}(s)$



Simulation example (Linearized Buck)
$f_c \approx 40$ kHz
$\varphi_m \approx 30°$
DC Gain limited to roughly 70dB

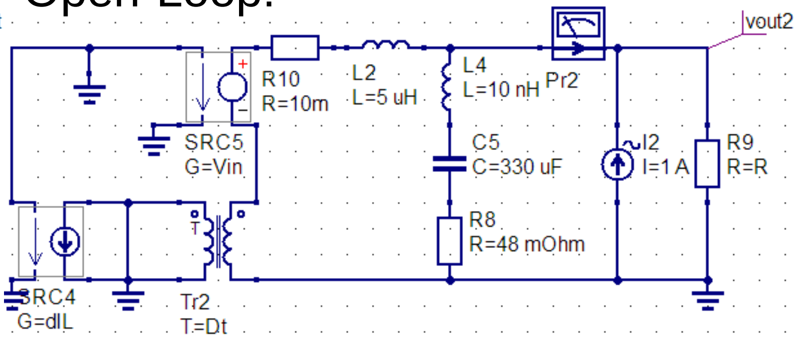
Buck Output Impedance Simulation

Closed-Loop:



number	D	R	Vin	Vout	Iout	d.V
1	0.0667	1	15	1	1	0.144

Open-Loop:



dc simulation

DC1

ac simulation

AC1
Type=log
Start=10 Hz
Stop=1 MHz
Points=201

Equation
Input1
Vin=15
Vout=1
D=Vout/Vin
R=1
Iout=Vout/R
Dt=1/D
IL=Iout
dIL=-IL
dVin=-Vin
Vramp=2.14
Gpwm=1/Vramp

~~Equation~~
Compensator70
R1=2k
R2=3.641k
R3=1.278k
C1=11.16n
C2=12.4n
C3=88.11p

Equation
Compensator30
R1=1k
R2=20.48k
R3=0.358k
C1=2.208n
C2=2.96n
C3=1.19n

Equation
Result1
Zout=vout.v/-Pr1.i
magZout=abs(Zout)
argZout=180*arg(Zout)/pi

Equation
CalculateLoopGain
Tcalc=(Zol/Zout)-1
magTcalc=20*log10(mag(Tcalc))
argTcalc=180*(arg(Tcalc))/pi

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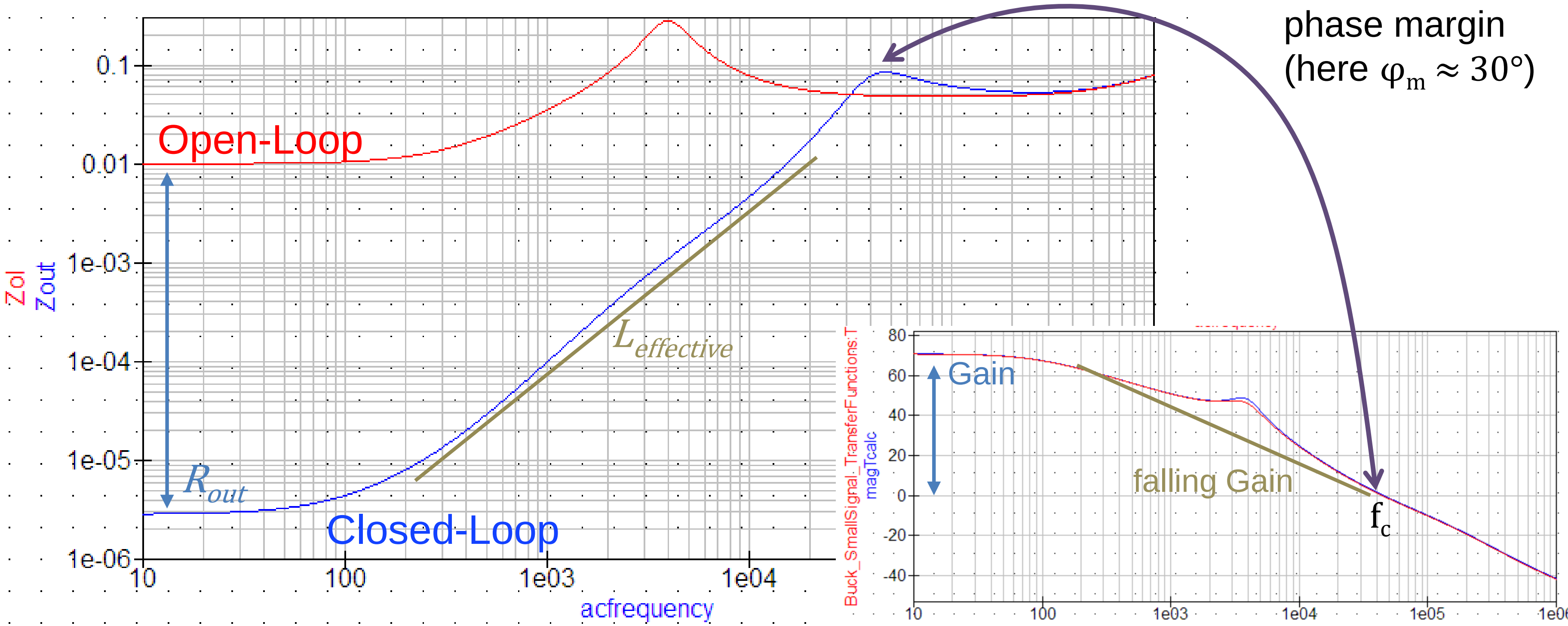
Output Impedance

Resonance peak at f_c correlates to phase margin (here $\varphi_m \approx 30°$)



$$Z_{out}(s) = \frac{Z_{OL}(s)}{1+T(s)} \rightarrow T(s) = \frac{Z_{OL}(s)}{Z_{out}(s)} - 1$$

- Output Impedance contains information about Loop Gain (Stability)!

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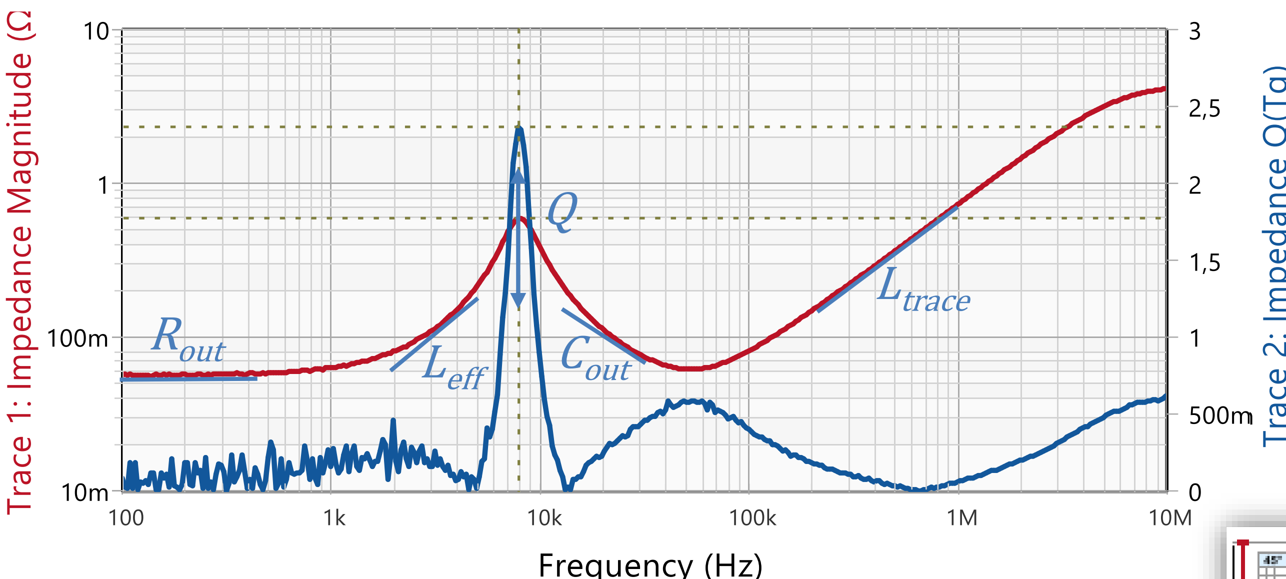
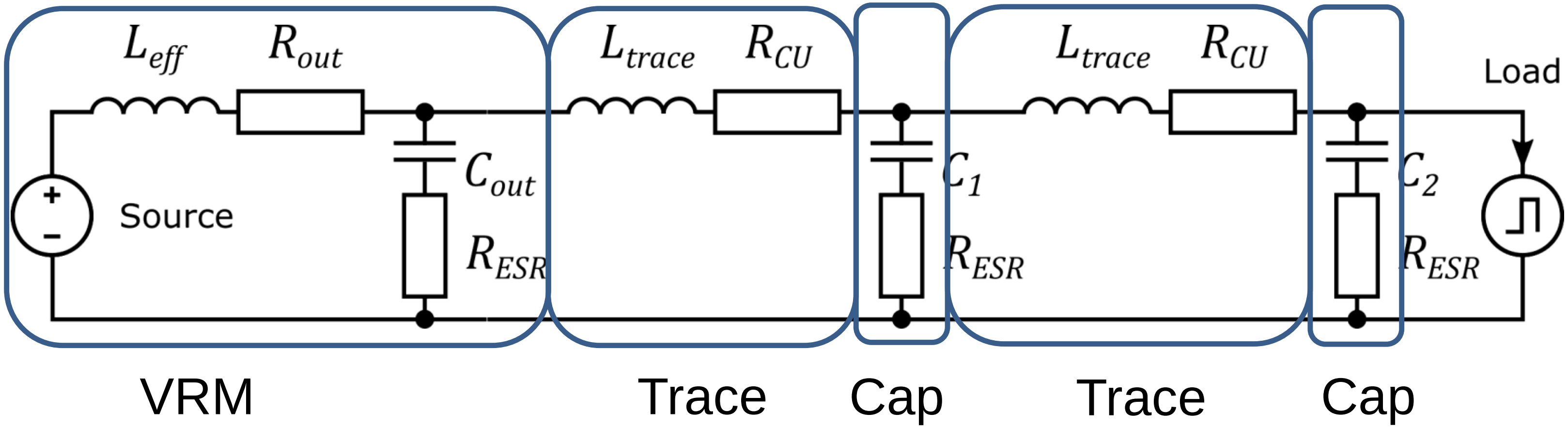
NISM (Non-Invasive Stability Measurement)

- Q correlates to Phase Margin φ_m
- Peak in Z_{out} correlates to the Q of the closed loop system



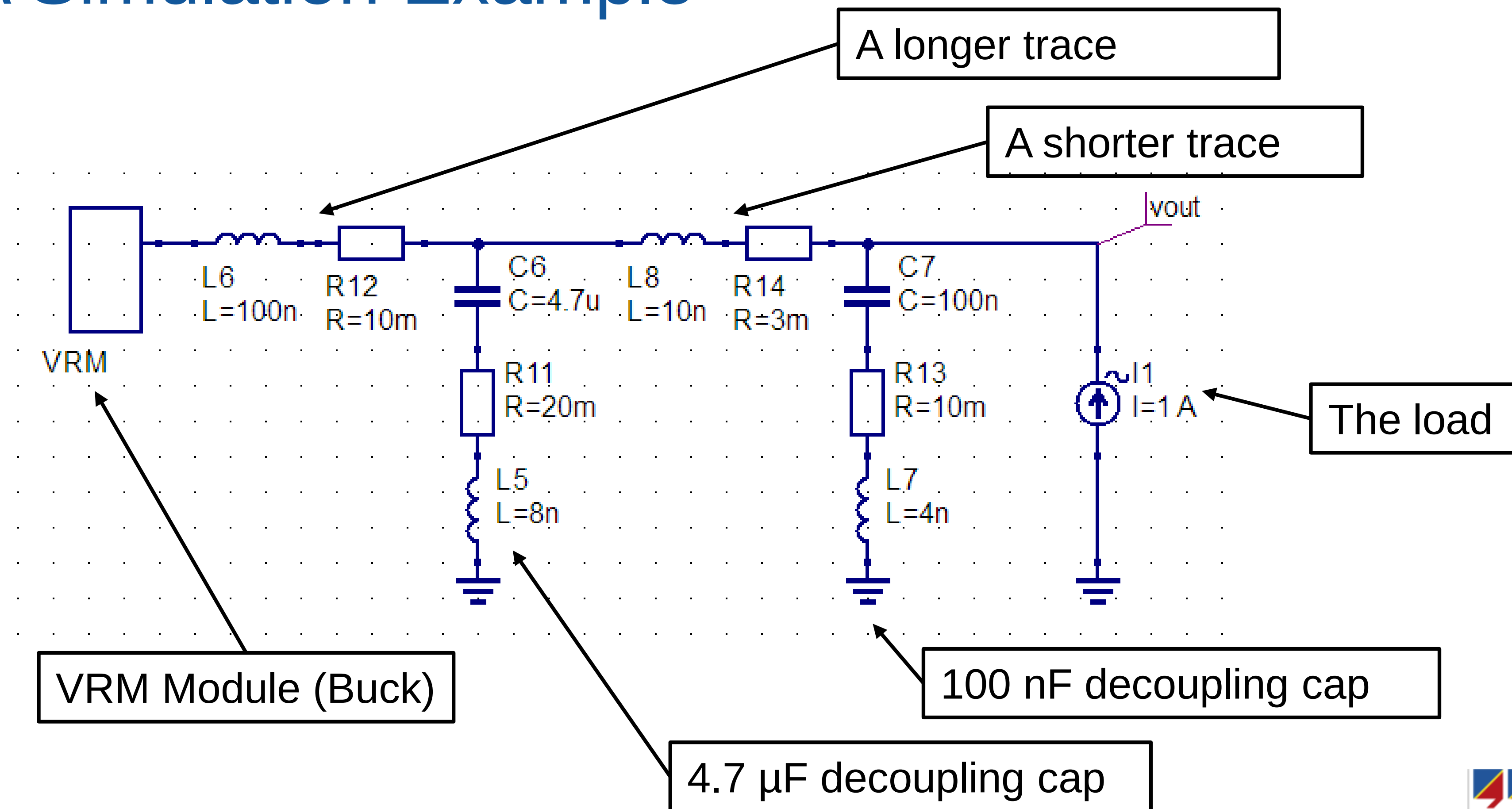
$$Q = \frac{\sqrt{\cos(\varphi_m)}}{\sin(\varphi_m)}$$

There is more from the VRM to the Load

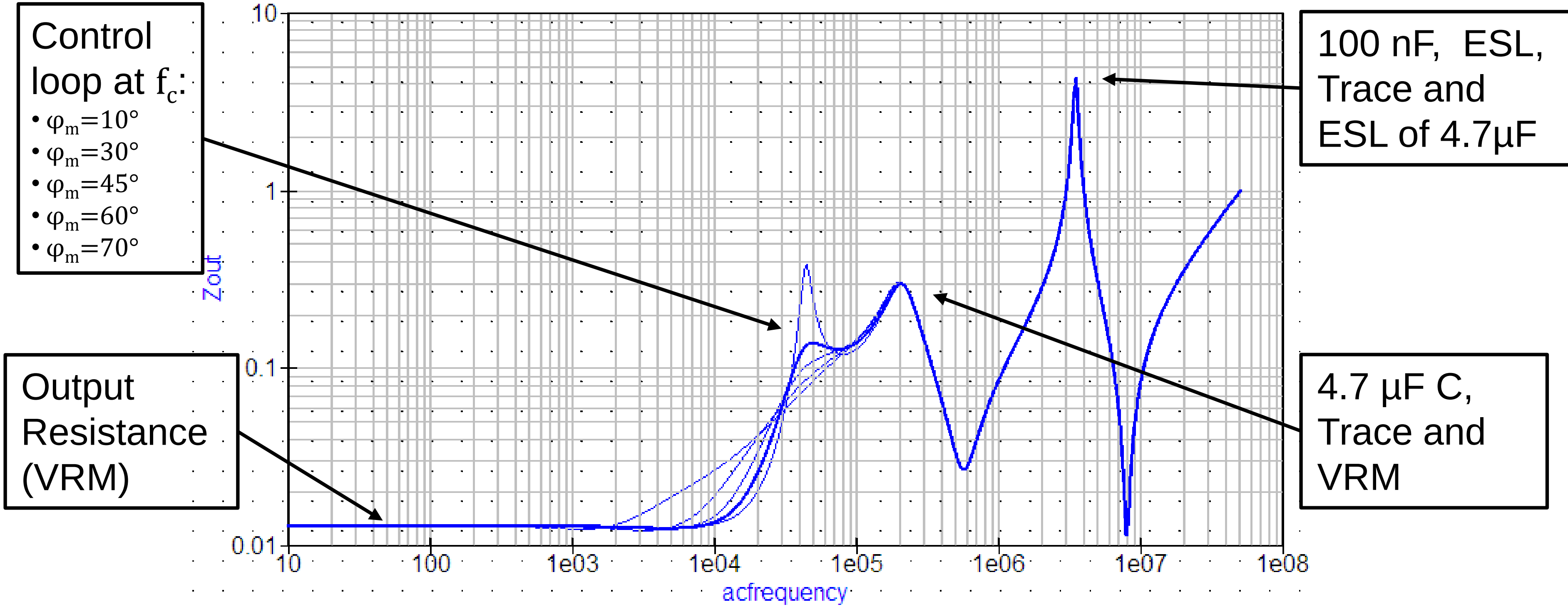


- Multiple L-C resonance circuits
  - Ceramic caps have generally very low ESR values
  - Ferrites have generally low resistance
  - The Q of the resonances can be high

A Simulation Example



This is what the load sees:



- 200 kHz load current → 300 mΩ source impedance
- 3 MHz load current → 3 Ω source impedance
- ➢ 1 A load current causes 0.3V / 3 V drop

Supply Impedance Peaks

- High impedance increases the risk of coupling noise to the supply voltage ($V = \sqrt{P \cdot R}$)
- Noise on the supply voltage can degrade performance of:
  - Oscillators (Jitter)
  - ADCs
  - Reference voltages
  - Low-Noise amplifiers
  - etc...

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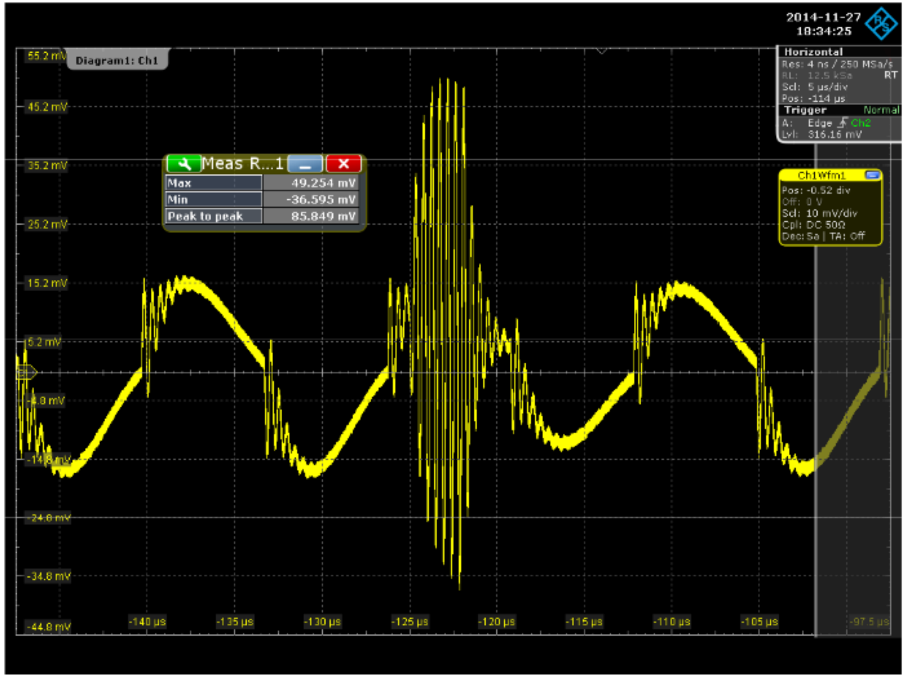
Risk of Rogue Waves

PICOTEST

- Dynamic load currents or load current patterns at multiple frequencies can superimpose
- Worst case scenario is a rogue wave



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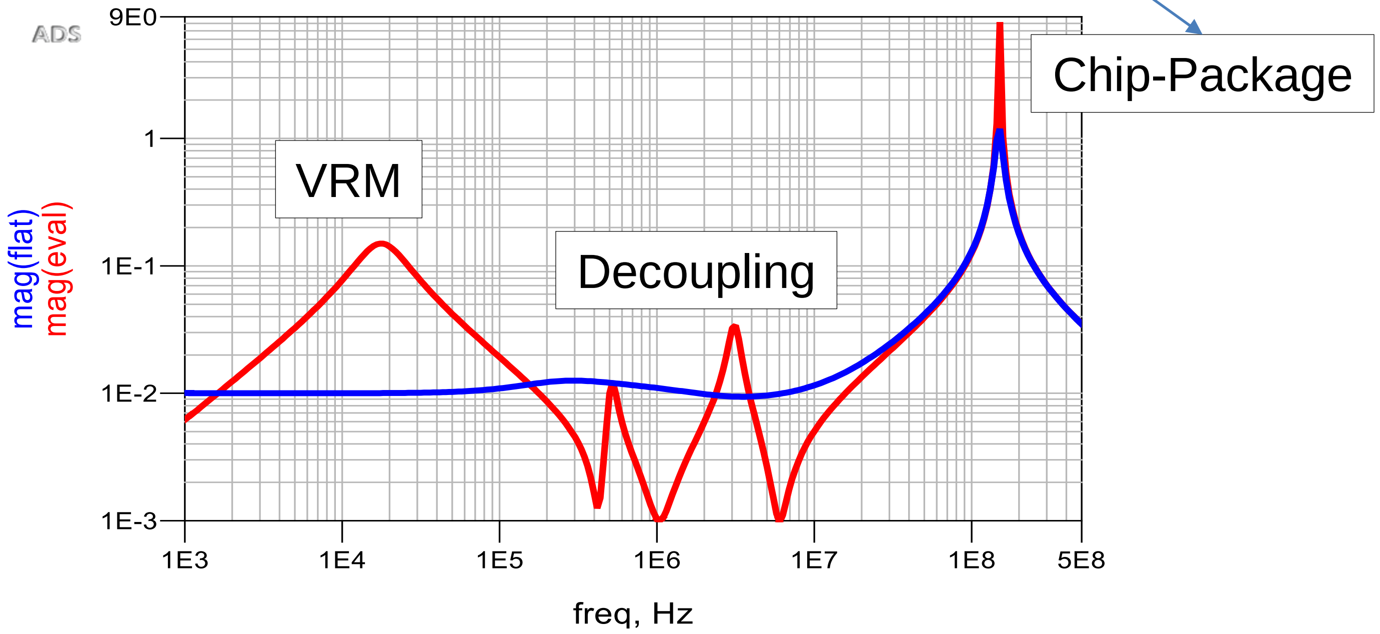
The Flat-Impedance Approach

PICOTEST

- The only reliable way to avoid resonances
- Represents a constant source resistance to the load
- Reduces the height of the “Bandini Mountain”



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The Output Impedance Plot

1. Contains information about the stability (oscillation tendency) of the voltage regulator
2. Reveals resonance frequencies of the decoupling network
3. The resonance peaks can cause performance degradation of the supplied load

➢ Let’s measure it!

(it sounds more difficult than it is)

Measuring Output Impedance ≤ 3.3VDC

- No special precautions needed. Bode 100 Signal Source and 50 Ω inputs can withstand the voltage.
- Possible Measurement Methods:
  1. One-Port impedance measurement
  2. Shunt-Thru measurement (recommended for very low Z)
  3. J2111A current injector
  4. Alternative load modulation

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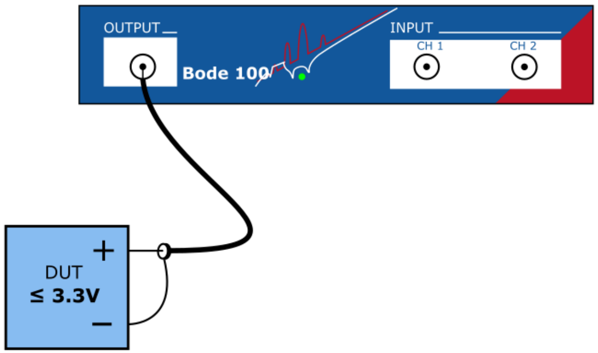
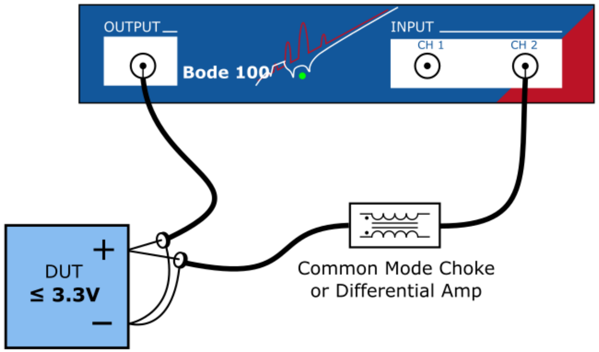
Measuring Output Impedance ≤ 3.3VDC





One-Port Method:
- Simplest setup providing quick results
- Not really suitable for mΩ measurements

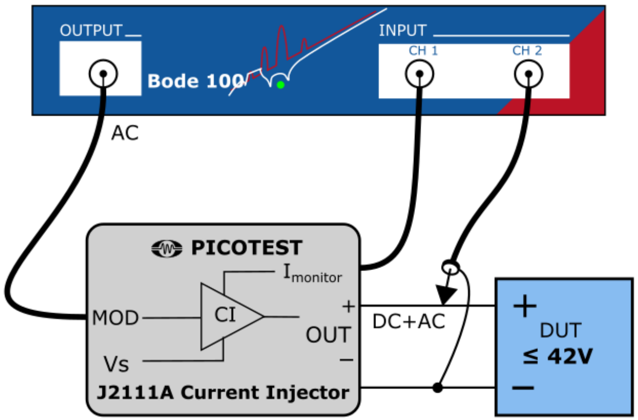
2-Port Shunt-Thru:
- Best suitable for mΩ measurements
- Take care of the GND-loop!
- Use amplifier to get more signal

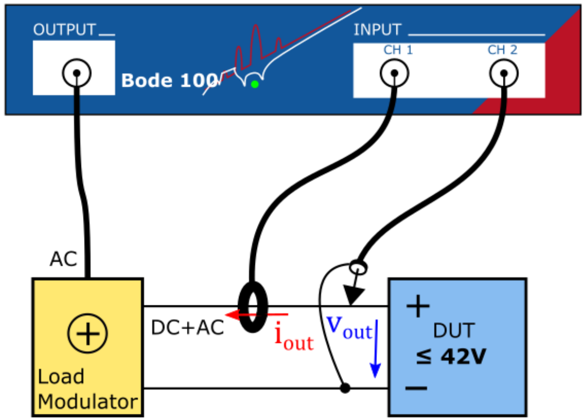
➢ Both methods can also measure OFF-State impedance

Measuring Output Impedance ≤ 42VDC

- Bode 100 Signal Source and 50 Ω must be AC coupled!
- Possible Measurement Methods:
  1. J2111A current injector
  2. One-Port impedance measurement **with DC Block**
     Note: Use calibration to remove the impedance of the DC Block
  3. Shunt-Thru measurement with **2 DC Blocks**
     Note: Use calibration to remove the impedance of the DC Block
  4. Shunt-Thru measurement with series-resistance
     Note: Use thru-calibration to remove the resistor influence
  5. Alternative load modulation

Measuring Output Impedance ≤ 42VDC





Current Injector:

- Simple setup
- Sinks 25 mA DC load current + AC current (10mA/V)

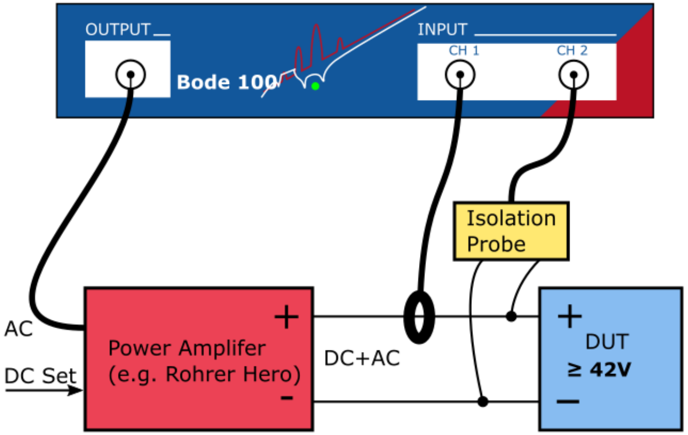
Dynamic Load:

- AC or AC+DC current
- Current probe & voltage probe

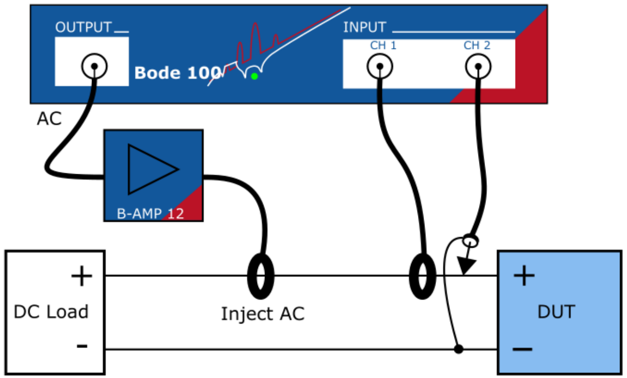
Measuring Output Impedance ≥ 42VDC

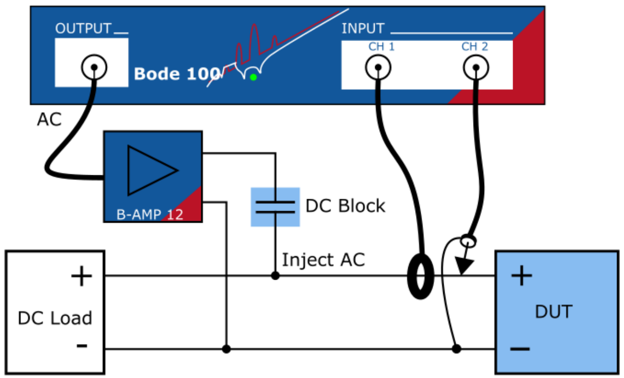
- Bode 100 must be protected from high voltages!
- Possible Measurement Methods:

Voltage/Current method using a power amplifier



Alternative Load Modulation Possibilities





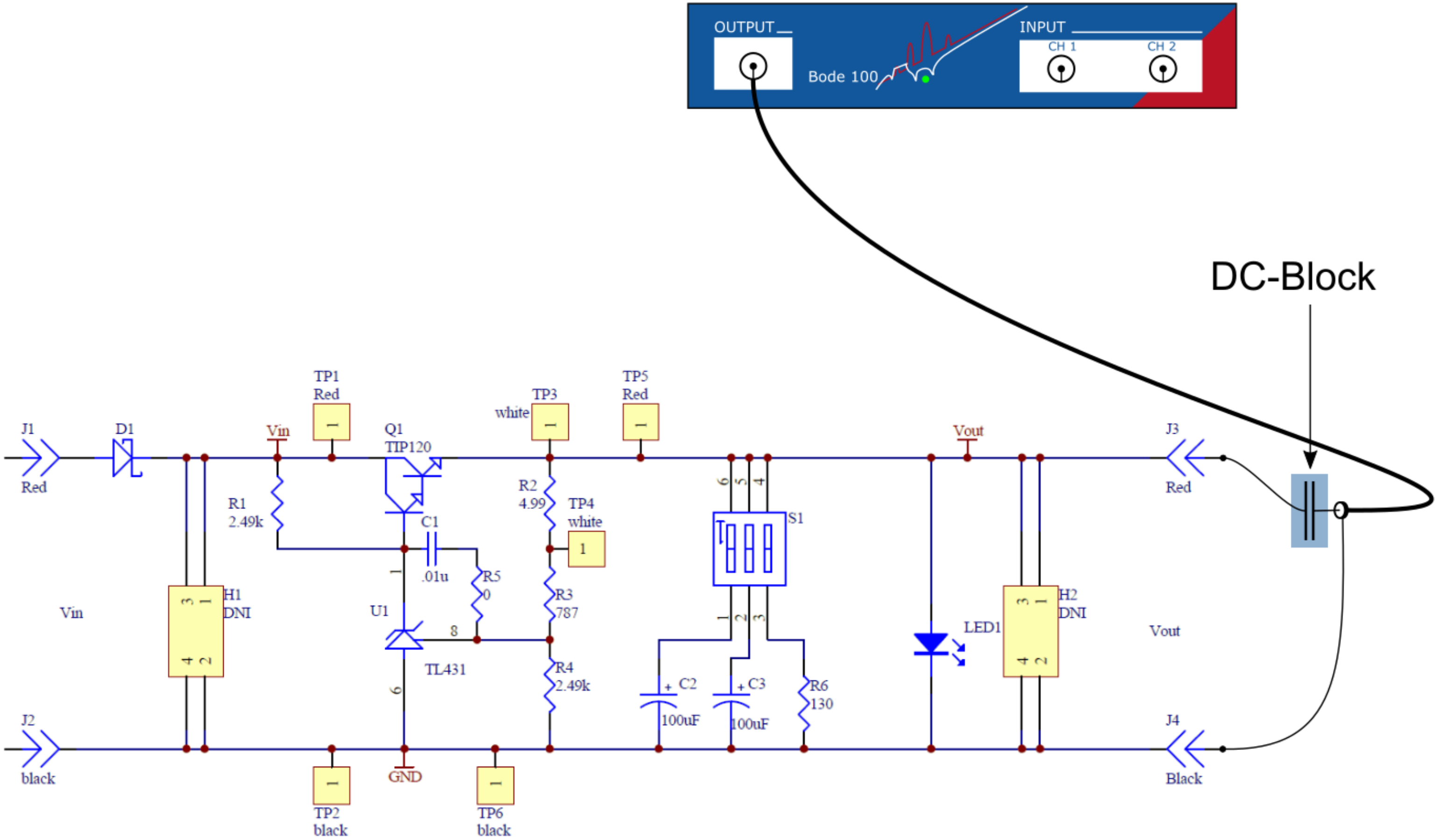
Inductive injection

- Provides galvanic isolation
- Requires big transformer that does not saturate at DC
- Use an amplifier to get more signal

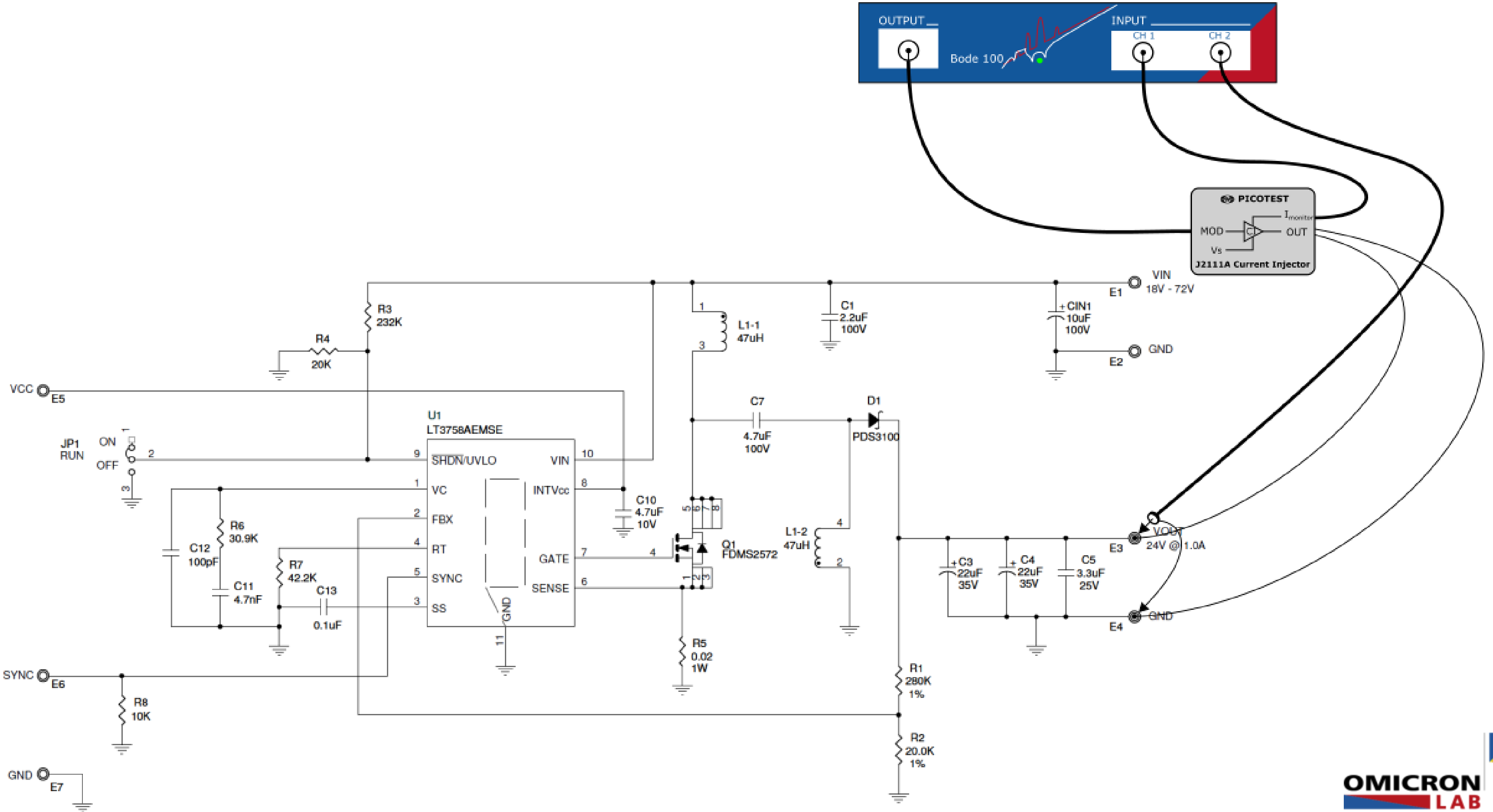
Capacitive injection

- Requires big capacitor at low frequencies
- Use amplifier to get more signal

Hands-On Example VRTS 1.5

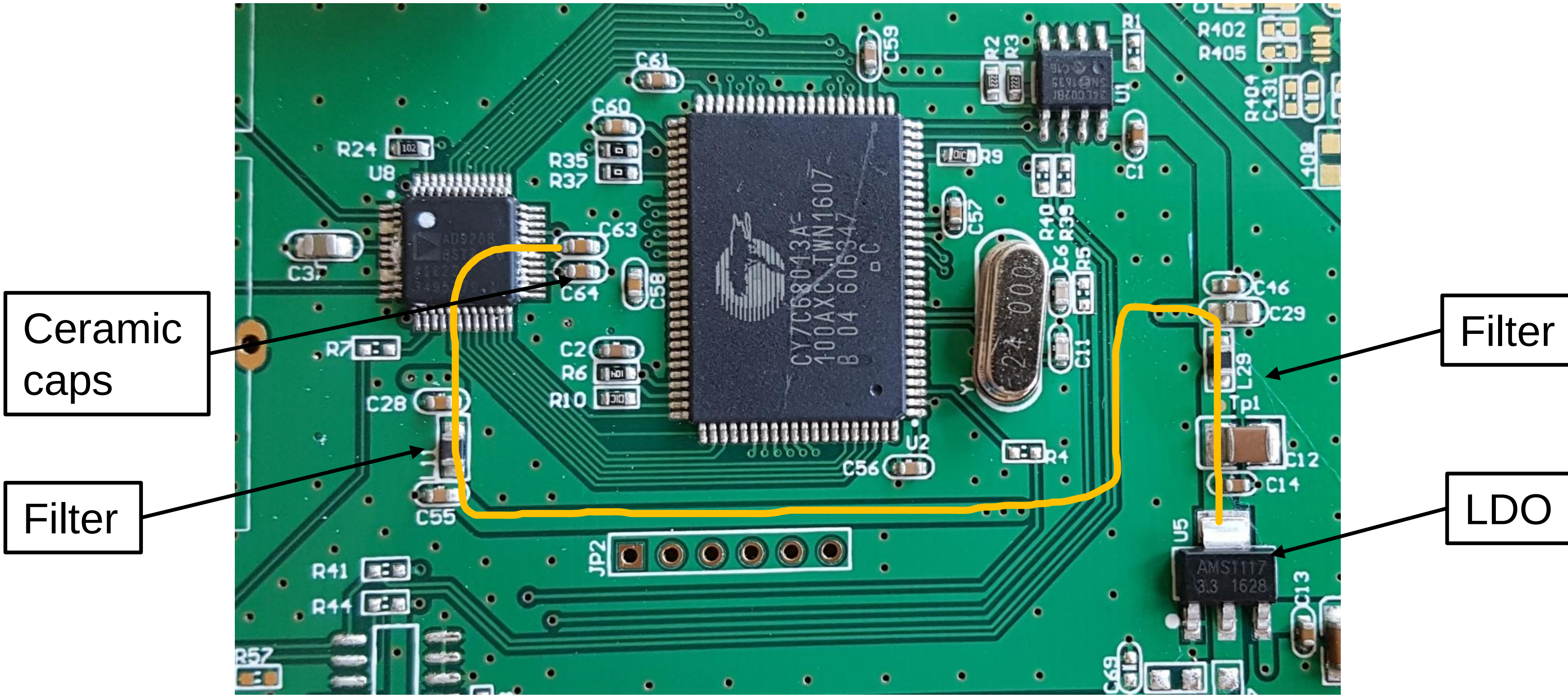


Hands-On Example SEPIC

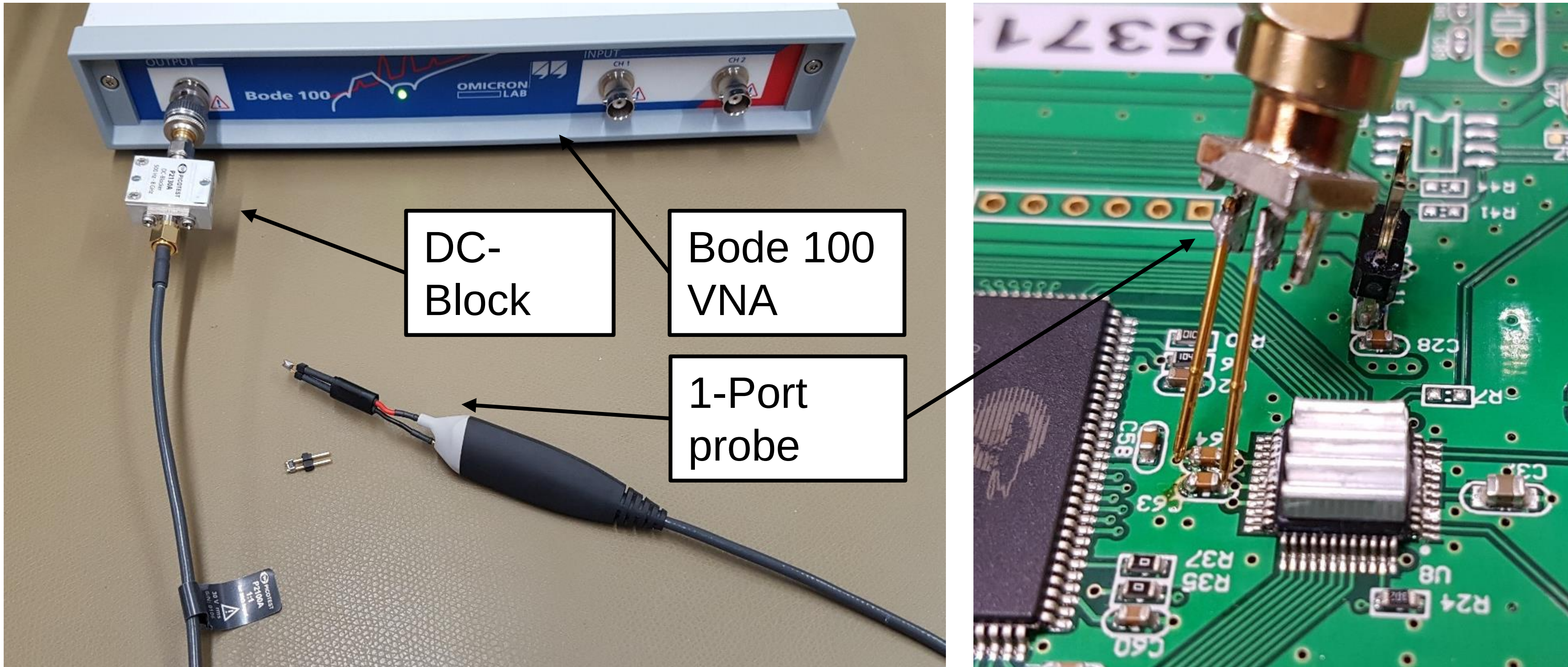


System-Example: USB Scope

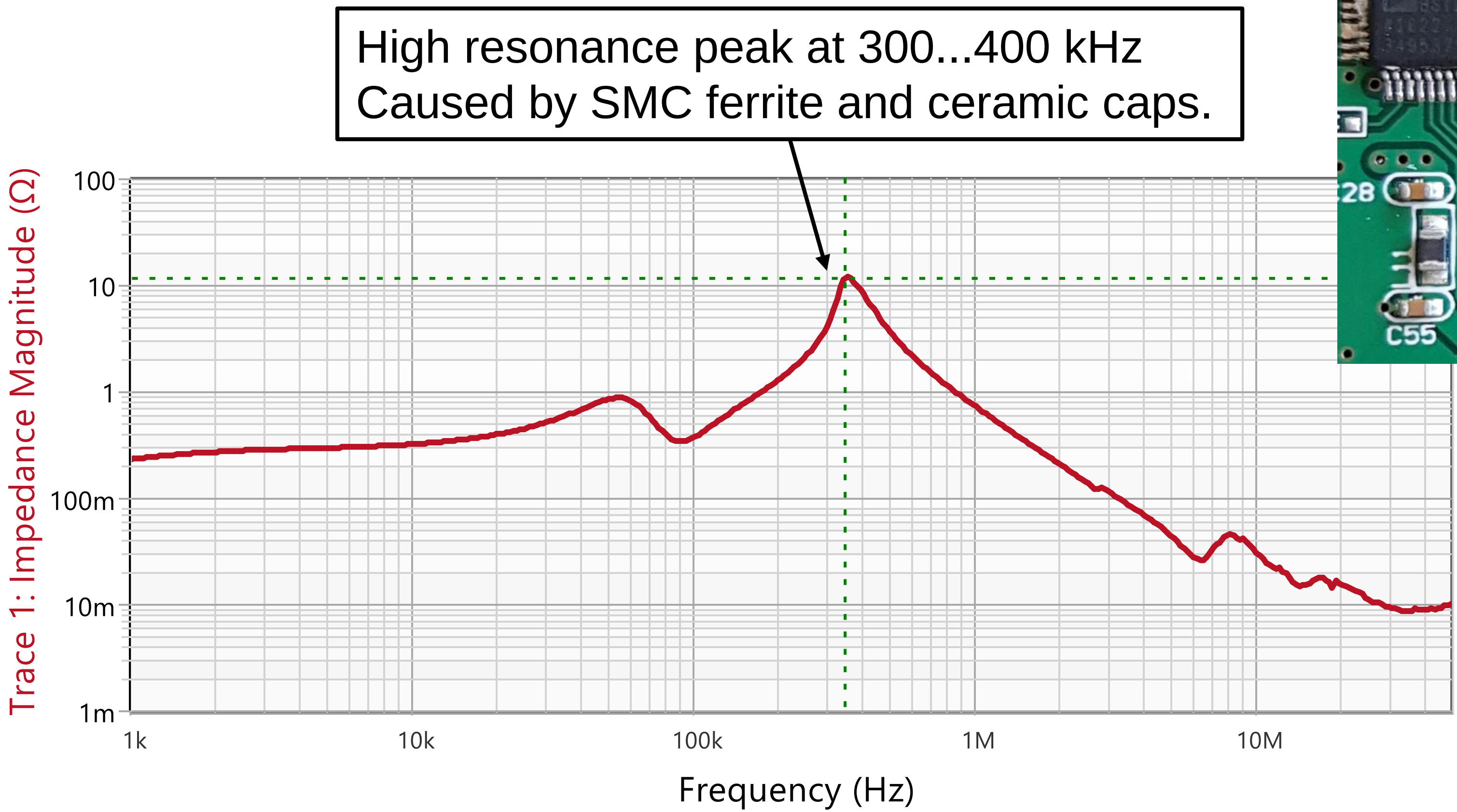
ADC Power Supply

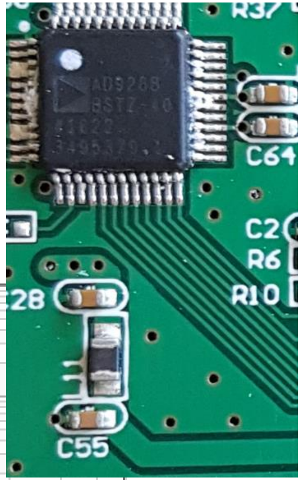


Measuring Supply Output Impedance

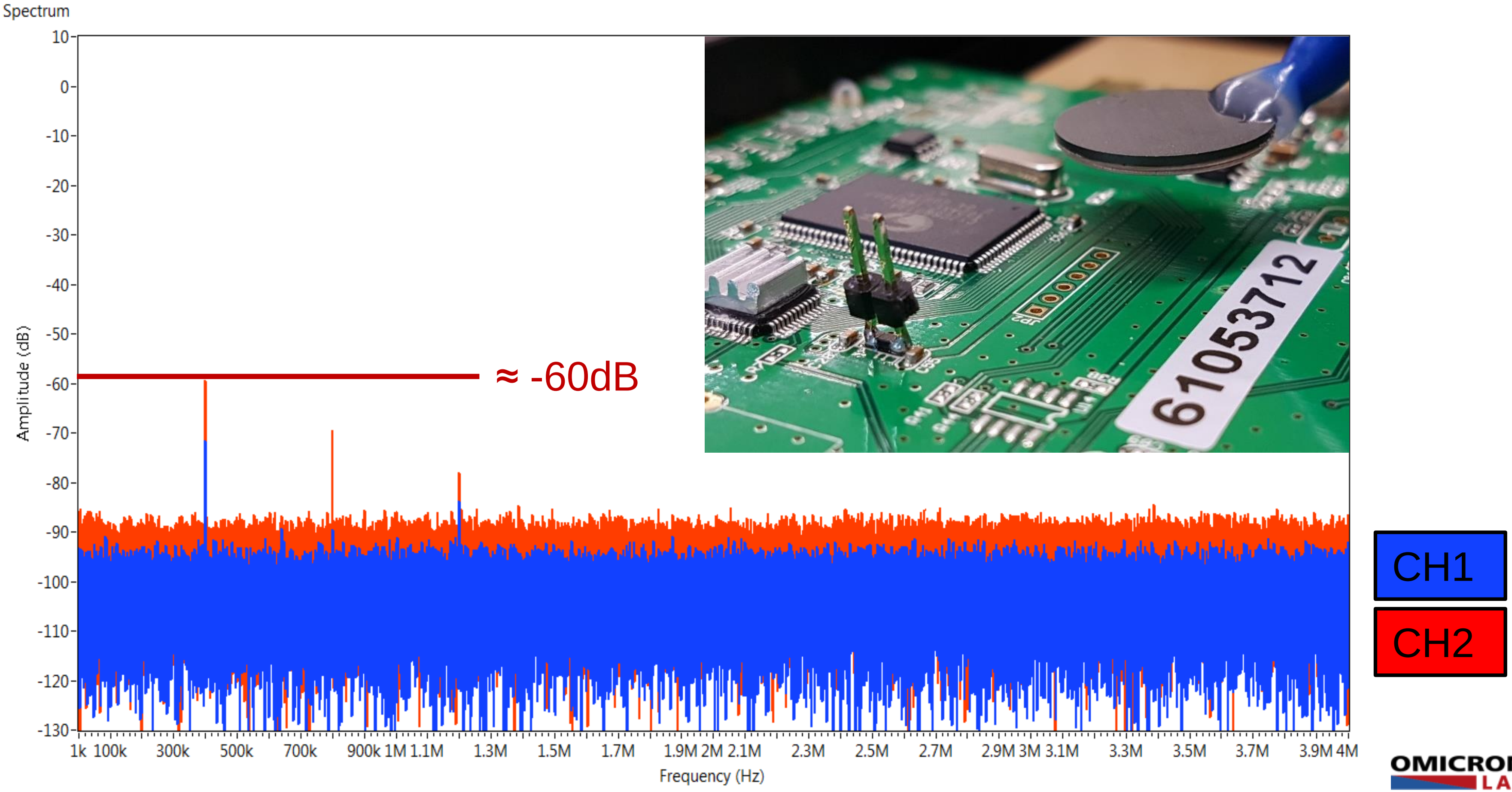


Measurement Result

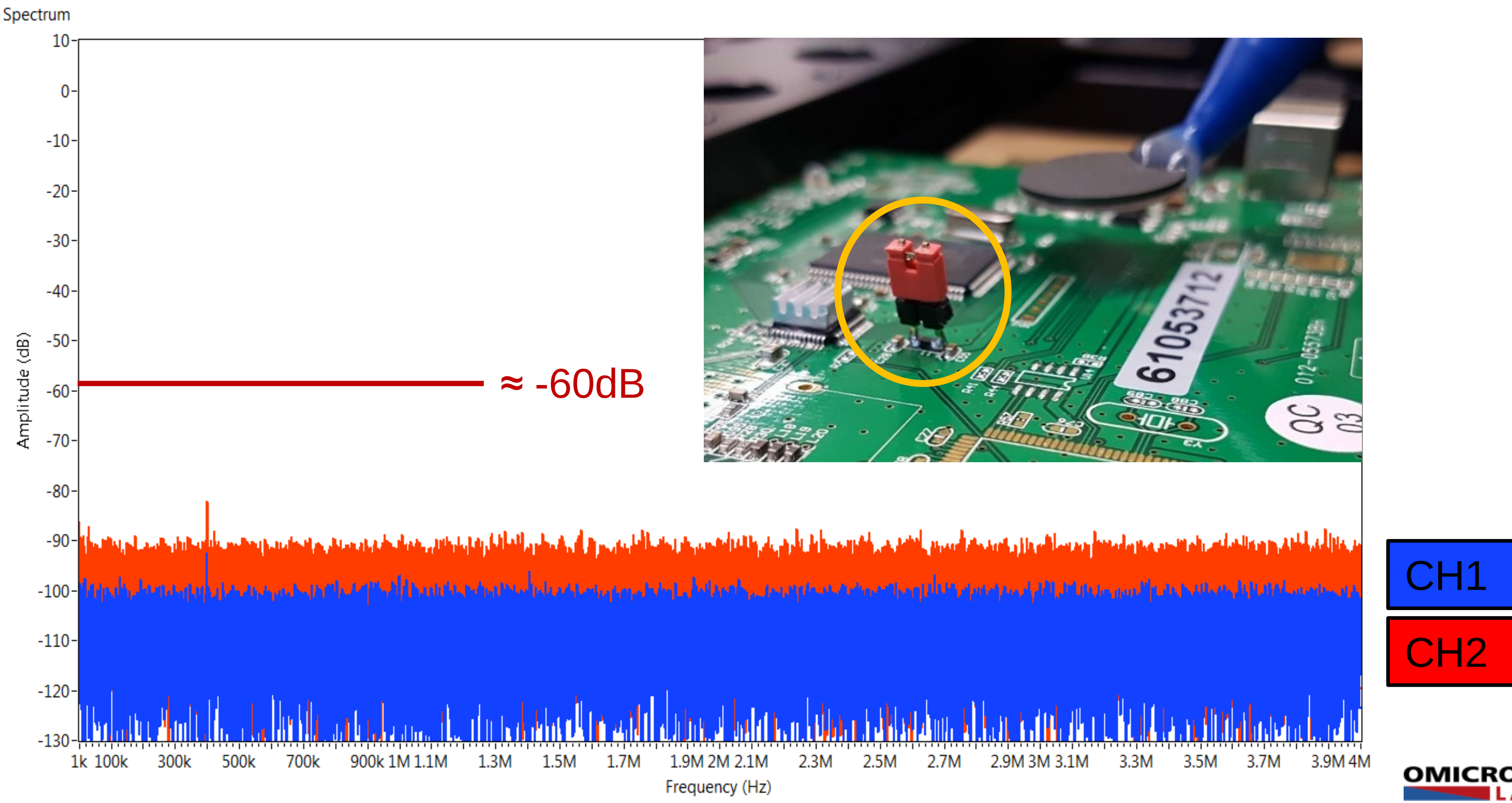




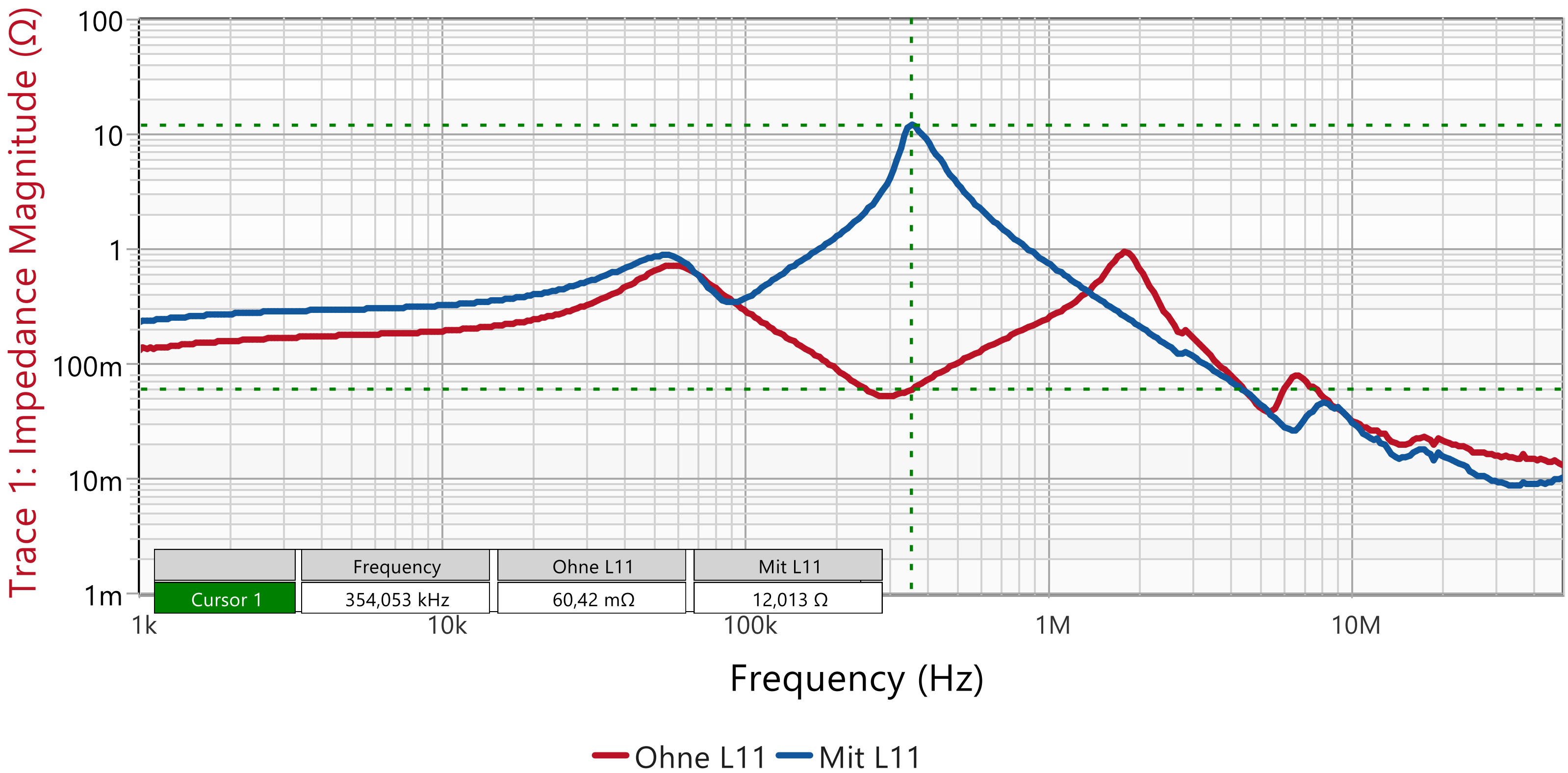
400 kHz Disturbance (inductively coupled)



Shorting the Ferrite Bead



What has Changed in Output Impedance?



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Summary

- Output impedance reveals information about
  - Control loop stability
  - Resonance frequencies in the supply line
- Measuring output impedance is simple
  - The output capacitors are nearly always accessible
  - The control loop must not be broken
- A flat impedance guarantees optimum damping at all frequencies
- Lower output impedance results in less noise

References and further information:

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. 2001. Norwell, Mass: Springer, 2001.

[2] Sandler, S., *The inductive nature of voltage-control loops,* EDN (www.edn.com), 2015.

[3] Sandler, S., *Designing Power for Sensitive Circuits, EDICon*, 2017

[4] Sandler, S., *Target Impedance and Rogue Waves, DesignCon*, 2016

[5] Sandler, S., *Power Integrity*, Mc Graw Hill Education Ltd, 2014

[6] Yuri Panov and Milan Jovanovic, Practical Issues of Input/Output Impedance Measurements in Switching Power Supplies and Application of Measured Data to Stability Analysis, Delta Power Electronics Laboratory

Feel free to ask questions via the Q&A function...

If time runs out, please send us an e-mail and we will follow up.

You can contact us at: info@omicron-lab.com

Thank you for your attention!

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