Output Impedance

OMICRON Lab Webinar Series 2020

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We will record the presentation such that you can view it again later

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Florian Hämmerle

• Studied Mechatronics at Vorarlberg University of Applied Sciences

• Working at OMICRON Lab since 2010 in:
  – Technical Support & Applications
  – Product management

• Contact:
  – florian.haemmerle@omicron-lab.com
  – https://meet-omicron.webex.com/meet/florian.haemmerle
Tobias Schuster

• Completed electrical engineering college in 2013
• Studied Industrial Engineering and Management
• Working at OMICRON Lab since 2015 focusing on:
  – Technical Support
  – Applications
  – Sales
• Contact:
  – tobias.schuster@omicron-lab.com
  – https://meet-omicron.webex.com/meet/tobias.schuster
Agenda

• DC voltage source (ideal vs. real)
• Output Impedance of VRM
• NISM (Non-Invasive Stability Measurement)
• From the power to the load
• Measuring Output Impedance
• Examples
DC Voltage Source

Two-terminal device that can maintain a fixed DC voltage.

Ideally:

\[ R_{out} = 0 \rightarrow V_{out} = V_0 \]

In reality:

\[ R_{out} \neq 0 \rightarrow V_{out} = V_0 - I_{out}R_{out} \]
Stabilizing Output via Voltage Feedback

- Closing the loop changes the output impedance to:

\[
Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)}
\]

- \(Z_{OL}(s)\)...Open-Loop Output Impedance
- \(Z_{out}(s)\)...Closed-Loop Output Impedance
- \(T(s)\)...Loop Gain

\[\text{Power stage } Z_{OL}(s)\]

\[\text{Control}\]

\[\text{Feedback}\]

\[\text{Reference}\]
Closed-Loop Output Impedance

\[ Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)} \]

• If \( T(s) \gg 1 \) then \( Z_{out}(s) \ll Z_{OL}(s) \)
• If \( T(s) \ll 1 \) then \( Z_{out}(s) = Z_{OL}(s) \)
• If \( T(s) = 1 \) then \( Z_{out}(s) = \frac{1}{2} Z_{OL}(s) \)

➢ High loop gain results in low output impedance
Loop Gain

- Loop Gain at DC is not $\infty \rightarrow R_{\text{out}} \neq 0$
- Control loop is not infinitely fast $\rightarrow$ Loop Gain reduces with $f$
- Loop Gain crosses 0 dB line at some crossover frequency $f_c$
  - Control loop affects $Z_{\text{out}}$ mainly below $f_c$
  - Above $f_c$ the feedback has nearly no effect: $Z_{\text{out}}(s) = Z_{OL}(s)$

Simulation example (Linearized Buck)
- $f_c \approx 40$ kHz
- $\phi_m \approx 30^\circ$
- DC Gain limited to roughly 70dB
Buck Output Impedance Simulation

Closed-Loop:

Open-Loop:
Output Impedance

Resonance peak at $f_c$ correlates to phase margin (here $\varphi_m \approx 30^\circ$)

$\mathbf{Output \ Impedance \ contains \ information \ about \ Loop \ Gain \ (Stability)!}$

\[
Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)} \Rightarrow T(s) = \frac{Z_{OL}(s)}{Z_{out}(s)} - 1
\]
NISM (Non-Invasive Stability Measurement)

- Q correlates to Phase Margin $\varphi_m$
- Peak in $Z_{out}$ correlates to the Q of the closed loop system

$$Q = \frac{\sqrt{\cos(\varphi_m)}}{\sin(\varphi_m)}$$
There is more from the VRM to the Load

➢ Multiple L-C resonance circuits
  - Ceramic caps have generally very low ESR values
  - Ferrites have generally low resistance
  ➢ The Q of the resonances can be high
A Simulation Example

VRM Module (Buck)

A longer trace

A shorter trace

100 nF decoupling cap

4.7 μF decoupling cap

The load
This is what the load sees:

Control loop at \( f_c \):
- \( \phi_m = 10^\circ \)
- \( \phi_m = 30^\circ \)
- \( \phi_m = 45^\circ \)
- \( \phi_m = 60^\circ \)
- \( \phi_m = 70^\circ \)

Output Resistance (VRM):

- 200 kHz load current \( \rightarrow 300 \text{ m\Omega} \) source impedance
- 3 MHz load current \( \rightarrow 3 \text{ \Omega} \) source impedance
- 1 A load current causes 0.3V / 3 V drop

4.7 \( \mu \text{F} \) C, Trace and VRM

100 nF, ESL, Trace and ESL of 4.7\( \mu \text{F} \)
Supply Impedance Peaks

• High impedance increases the risk of coupling noise to the supply voltage \( V = \sqrt{P \cdot R} \)

• Noise on the supply voltage can degrade performance of:
  − Oscillators (Jitter)
  − ADCs
  − Reference voltages
  − Low-Noise amplifiers
  − etc...
Risk of Rogue Waves

• Dynamic load currents or load current patterns at multiple frequencies can superimpose

• Worst case scenario is a rogue wave
The Flat-Impedance Approach

- The only reliable way to avoid resonances
- Represents a constant source resistance to the load
- Reduces the height of the “Bandini Mountain”
The Output Impedance Plot

1. Contains information about the stability (oscillation tendency) of the voltage regulator
2. Reveals resonance frequencies of the decoupling network
3. The resonance peaks can cause performance degradation of the supplied load

➢ Let’s measure it!
(it sounds more difficult than it is)
Measuring Output Impedance ≤ 3.3VDC

• No special precautions needed. Bode 100 Signal Source and 50 Ω inputs can withstand the voltage.

• Possible Measurement Methods:
  1. One-Port impedance measurement
  2. Shunt-Thru measurement (recommended for very low Z)
  3. J2111A current injector
  4. Alternative load modulation
Measuring Output Impedance $\leq 3.3\text{VDC}$

**One-Port Method:**
- Simplest setup providing quick results
- Not really suitable for m$\Omega$ measurements

**2-Port Shunt-Thru:**
- Best suitable for m$\Omega$ measurements
- Take care of the GND-loop!
- Use amplifier to get more signal

➢ Both methods can also measure OFF-State impedance
Measuring Output Impedance $\leq 42\text{VDC}$

- Bode 100 Signal Source and 50 $\Omega$ must be AC coupled!
- Possible Measurement Methods:
  1. J2111A current injector
  2. One-Port impedance measurement with DC Block
     **Note:** Use calibration to remove the impedance of the DC Block
  3. Shunt-Thru measurement with 2 DC Blocks
     **Note:** Use calibration to remove the impedance of the DC Block
  4. Shunt-Thru measurement with series-resistance
     **Note:** Use thru-calibration to remove the resistor influence
  5. Alternative load modulation
**Measuring Output Impedance ≤ 42VDC**

**Current Injector:**
- Simple setup
- Sinks 25 mA DC load current
  + AC current (10mA/V)

**Dynamic Load:**
- AC or AC+DC current
- Current probe & voltage probe
Measuring Output Impedance $\geq 42$VDC

- Bode 100 must be protected from high voltages!
- Possible Measurement Methods:
  Voltage/Current method using a power amplifier

![Diagram](image-url)
Alternative Load Modulation Possibilities

**Inductive injection**
- Provides galvanic isolation
- Requires big transformer that does not saturate at DC
- Use an amplifier to get more signal

**Capacitive injection**
- Requires big capacitor at low frequencies
- Use amplifier to get more signal
Hands-On Example VRTS 1.5
Hands-On Example SEPIC
System-Example: USB Scope

CH1

CH2

ADC

LDO
ADC Power Supply

- Ceramic caps
- Filter
- LDO
Measuring Supply Output Impedance

- DC-Block
- Bode 100 VNA
- 1-Port probe
Measurement Result

High resonance peak at 300...400 kHz
Caused by SMC ferrite and ceramic caps.
400 kHz Disturbance (inductively coupled)

\[ \approx -60\text{dB} \]
Shorting the Ferrite Bead

Approximately -60dB

Frequency (Hz)

Amplitude (dB)
What has Changed in Output Impedance?

![Graph showing changes in output impedance]

- **Frequency (Hz):**
  - **1k to 10M**

- **Trace 1: Impedance Magnitude (Ω):**
  - **Trace Details:**
    - **Cursor 1:** 354,053 kHz
      - **Ohne L11:** 60.42 mΩ
      - **Mit L11:** 12.013 Ω

- **Y-Axis:**
  - **1m, 10m, 100m, 1, 10, 100, 1000, 10000, 100000, 1000000**

- **Colors:**
  - **Red:** Ohne L11
  - **Blue:** Mit L11
Summary

• Output impedance reveals information about
  − Control loop stability
  − Resonance frequencies in the supply line

• Measuring output impedance is simple
  − The output capacitors are nearly always accessible
  − The control loop must not be broken

• A flat impedance guarantees optimum damping at all frequencies

• Lower output impedance results in less noise
References and further information:


Feel free to ask questions via the Q&A function...

If time runs out, please send us an e-mail and we will follow up.
You can contact us at: info@omicron-lab.com

Thank you for your attention!